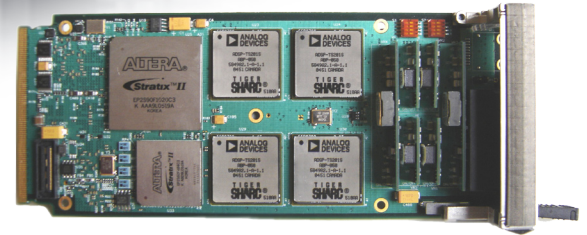


B2-AMC

Hybrid Signal Processing Advanced Mezzanine Card

Universal Baseband Processing

- 2G, 2.5G, and 3G Wireless Applications
- WiMAX PHY
- Software Defined Radio (SDR)



Programmable Baseband Processing for Wireless Communications Infrastructure

Featuring a hybrid signal processing architecture that couples an Altera® Stratix® II FPGA with four ADSP-TS2015 TigerSHARC® processors, BittWare's B2-AMC (B2AM) is an AdvancedMC that supports universal baseband processing for wireless communications infrastructure such as 2G, 2.5G, 3G, WiMAX and SDR. A full-height, single wide AMC, the B2AM attaches to AdvancedTCA (Advanced Telecom Compute Architecture) carriers or other cards equipped with AMC bays and is completely hot-swappable. The B2AM combines an Altera Stratix II FPGA, four TigerSHARCs, a variety of front and back panel I/O interfaces, and a configurable 4x network interface supporting a variety of protocols. It also provides a 10/100 Ethernet interface and a Gigabit Ethernet interface for command, control, and reprogramming, as well as Flash memory for booting the DSPs and FPGAs.

Altera Stratix II

At the heart of the B2AM is a state-of-the-art Altera Stratix II FPGA containing up to: 179,400 equivalent LEs, 9.3 Mbits of RAM, 384 embedded 18x18 multipliers, 96 DSP blocks, and 12 PLLs. The FPGA provides pre-, post-, or co-processing to complement the TigerSHARC processing cluster, while also enabling seamless routing of the TigerSHARC I/O via BittWare's ATLANTIS™ framework.

ADSP-TS2015 DSPs

The B2AM features a single cluster of four ADSP-TS2015 TigerSHARC DSPs from Analog Devices, providing a total of 14.4 GFLOPS of floating point processing power and 57.5 GOPS of 16-bit fixed point processing power. In addition to 24 Mbits of on-chip RAM, each TigerSHARC also boasts four high-speed LVDS link ports. Each full-duplex link port is comprised of a 4-bit transmit and a 4-bit receive channel, and can support up to 500 MBytes/s in each direction for a total maximum throughput of up to 1 GByte/s. Two link ports from each DSP are used to create an interprocessor communications ring, and the remaining two link ports are routed to the on-board FPGA.

Fat Pipes, Common Options, and I/O Interfaces

The Altera Stratix II FPGA facilitates off-board I/O and provides communications routing and processing. It implements eight TigerSHARC link ports and supports a variety of external I/O, flags, and interrupts. Efficient routing is achieved using BittWare's ATLANTIS architecture, which tightly integrates the DSPs with the I/O peripherals and the FPGA and allows any combination of link ports and off-board I/O interfaces to be routed together, providing nearly infinite options for configuring the I/O.

The Stratix II interfaces to four ports in the AMC fat pipes via PMC Sierra's QuadPHY SerDes. The four ports provide a network data and control switch fabric interface on the AMC connector, configurable to support PCI Express, Advanced Switching Interconnect (ASI), Serial RapidIO, GigE, or XAUI. Alternatively, a single SerDes port can be run via a front panel fiber transceiver.

BittWare's FINE Bridge provides Gigabit Ethernet via the common options region, or can be optionally configured for PCI Express. It also provides 10/100 Ethernet and RS-232 on the AMC front panel.

The Stratix II provides 11 pairs of LVDS I/O (5 Rx, 1 Rx clk, 5 Tx) for proprietary antenna or network interfaces and 24 bits of general purpose digital I/O available on the AMC front panel.

Development Support

A B2-Breakout Board (B2B0) is available as a peripheral for the B2AM. The B2B0, only compatible with the B2AM, provides a convenient way to access the boards signals for test and debug.

Features

- Full-height, single wide Advanced Mezzanine Card
- Altera® Stratix® II FPGA for I/O, routing, and processing
- ADSP-TS201 DSP cluster
 - ◆ 4 ADSP-TS2015 TigerSHARC® DSPs
 - ◆ 57.5 GOPS 16-bit fixed point, 14.4 GFLOPS floating point processing power
- ATLANTIS™ framework
- Fat Pipes and Common Options Interfaces for Data and Control
 - ◆ Network interface configurable to support:
 - Serial RapidIO™
 - PCI Express™ and ASI
 - GigE, XAUI™ (10 GigE)
 - ◆ FINE bridge providing GigE and configurable for PCI Express
 - ◆ System synchronization via AMC system clocks
- Front Panel I/O
 - ◆ 10/100 Ethernet
 - ◆ LVDS I/O
 - ◆ General Purpose Digital I/O
 - ◆ RS-232
 - ◆ Optional 1x Fiber Transceiver [replaces AMC Fat Pipes]
 - ◆ JTAG port for debug support
- Booting of DSPs and FPGA via Flash nonvolatile memory



BOARD ARCHITECTURE

FPGA

- Altera Stratix II (EP2S60, 90, 130, or 180)
- I/O routing and data processing via BittWare's ATLANTIS framework
- Up to 179,400 equivalent LEs
- Up to 9.3 Mbits of RAM
- Up to 96 DSP blocks
- Up to 384 embedded multipliers
- Up to 12 PLLs

Processors

- 4 Analog Devices ADSP-TS201S TigerSHARC DSPs
- 600 MHz, 1.67 ns instruction rate DSP core
- 3.6 GFLOPS (32-bit floating point) or 14.4 GOPS (16-bit fixed point) per DSP
- Native support for 32-bit floating point operations and for 8, 16, and 32-bit fixed point operations
- 24 Mbits of on-chip RAM per DSP
- Four LVDS link ports at up to 1 GByte/s
- Integrated I/O processor with fourteen-channel DMA controller

External Memory

- 16 MB Flash memory for booting DSPs and configuring the FPGA

Link Ports

- 8 link ports extend from the ADSP-TS201S DSPs (2 per DSP) to the Stratix II FPGA
- 8 link ports (2 per DSP) dedicated for interprocessor communication
- Each link port runs up to 1 GByte/s

Fat Pipes Interface

- Stratix II FPGA (EP2S60, 90, 130, or 180)
- Up to 18 million system gates
- BittWare's ATLANTIS architecture
- Network Interface via PMC Sierra QuadPHY SerDes configurable to support PCI Express, ASI, Serial RapidIO, GigE and XAU1

Common Options Interface

- FINE™ bridge providing Gigabit Ethernet and configurable for PCI Express
- System clocks with clock buffering and phase shifting

AMC Front Panel I/O

- 10/100 Ethernet and RS-232 via SharcFINE
- 11 pairs LVDS I/O (5 Rx, 1 Rx clk, 5 Tx)
- 24 General Purpose Digital I/O
- Optional 1x Fiber Transceiver [replaces AMC Fat Pipes]
- JTAG debug interface to all four DSPs and the FPGA

Test and Debug

- B2-Breakout (B2BO) peripheral
- User access to AMC front panel signals
- GP-DIO, LVDS, 10/100b Ethernet, RS-232, JTAG

Power

- 25 W typical

Size

- AMC full-height, single width (74 mm x 180 mm) compatible with AMC specification

SOFTWARE SUPPORT

Host Interface

- BittWare's software development kit for Windows® and Linux contains C-callable libraries for board control and communications routines
- Porting kit available for other operating system platforms

Development Tools

- Altera's Quartus® II software
- Analog Devices' VisualDSP tools: kernel (VDK), C compiler, assembler, linker, simulator, and debugger
- BittWare's VisualDSP Target for on-board debugging from host without an ICE
- BittWare's TS-Lib optimized function libraries
- Analog Devices' wireless processing libraries for ADSP-TS201S TigerSHARC
- Analog Devices ICE emulators
- Enea's OSEck RTOS

Ordering Information

B2AM-XYX-ZZA-BCDE

X: DSPs

4 = 4 DSPs

E: Flash size

5 = 64 MB

YY: Processor Speed

50 = 500 MHz*

60 = 600 MHz†

ZZ: FPGA Size

09 = EP2S90

D: Front Panel Fiber

0 = Not populated*

1 = Populated†

C: SerDes Speed

0 = None

2 = 2.5 GHz

3 = 3.125 GHz*

B: Switch Fabric

N = None*

R = Serial Rapid I/O

A: FPGA Speed

3 = Altera speed grade 3

* Default

† Contact BittWare. Special order only.

