

S4-AMC

Altera® Stratix® IV GX Reconfigurable AMC



FPGA-Computing Advanced Mezzanine Card

Based on Altera's Stratix IV GX FPGA, BittWare's S4-AMC (S4AM) is a mid-size, single wide AdvancedMC that can be attached to AdvancedTCA (Advanced Telecom Compute Architecture) carriers or other cards equipped with AMC bays, and used in MicroTCA systems. The S4AM features a high-density, low-power Altera Stratix IV GX FPGA designed specifically for serial I/O-based applications, creating a completely flexible, reconfigurable AMC. BittWare's ATLANTIS FrameWork, in conjunction with the FINE Host/Control Bridge, greatly simplifies application development and integration of this powerful board. The board also provides an IPMI system management interface, a configurable 15 port AMC SerDes interface supporting a variety of protocols, and a front panel 4x SerDes interface supporting CPRI and OBSAI. Additionally, the board features 10/100 Ethernet, Gigabit Ethernet, two banks of DDR3 SDRAM, two banks of QDRII+ SRAM, and Flash memory for booting the FPGAs and FINE. Providing enhanced flexibility is the VITA 57-compliant FMC site which has an additional eight SerDes, 60 LVDS pairs, and six clocks.

Altera Stratix IV GX FPGA

The Altera Stratix IV GX was specifically designed for serial I/O-based applications requiring high-density, reconfigurable logic. The Stratix IV GX provides 27 full-duplex, multi-gigabit transceivers, 24 of which are high-performance supporting PCI Express (Rev 1.0/2.0), 10GigE, Gigabit Ethernet, Serial RapidIO (Rev 1.0/2.0), and SerialLite II standards. It contains up to 530k equivalent LEs, over 20 Mbits of embedded memory, and 1,024 embedded 18x18 multipliers. The FPGA implements BittWare's ATLANTIS FrameWork and provides seamless routing of all on-board data, I/O, and memory.

Fat Pipes, Common Options, and I/O Interfaces

The Stratix IV GX FPGA interfaces to three ports (1, 2, & 3) in the AMC common options region, and 16 ports in the AMC fat pipes region (4 - 15, 17 - 20). These 19 ports provide a network data and control switch fabric interface on the AMC connector, with 12 supporting up to 6.25 GHz, three supporting up to 3.125 GHz, and the remaining four providing LVDS rear-panel I/O.

All AMC clocks are also connected to the Stratix IV GX.

The front panel provides an additional four SerDes via an Infiniband-type connector, along with 10/100 Ethernet, two RS-232 ports, and a JTAG port for debug support.

VITA 57 FMC Site for Processing and I/O Expansion

The FMC site provides eight high-performance SerDes and 60 LVDS pairs, along with six clocks. The connector is compliant with the VITA-57 mezzanine standard for FPGA IO, enabling the S4AM to be customized to individual needs.

ATLANTIS™ FrameWork

BittWare's ATLANTIS FrameWork (AFW) provides reconfigurable FPGA components, along with the infrastructure necessary to implement, simulate, synthesize, validate, and deploy a complete FPGA application on the Stratix IV GX. AFW delivers fully validated FPGA physical interfaces for all board-level I/O and communications, including high speed SerDes and external memory control, along with resource management components such as buffering, DMA engines, and arbitration. Each component can be easily monitored and controlled via an addressed path implemented using Altera's open standard Avalon Memory Mapped Interface. Similarly, Altera's open standard Avalon Streaming Interface is used to implement point to point data transport between ATLANTIS components. A set of reconfigurable fabric components such as multiplexers, switches, decoders, and FIFOs expand the interconnect options for both memory mapped and streaming interfaces. AFW removes the burden of reinventing low-level IP for the FPGA, thus freeing developers to focus on unique value-added development.

FINE™ Host/Control Bridge

BittWare's FINE Host/Control Bridge implements a complete control plane interface for the S4AM, facilitating separate control and data planes, and greatly simplifying the development of data plane I/O and processing. Extensive software support is provided via BittWare's BittWorks Toolkit including a Host Interface Library (HIL) which supports run-time command and control, and the DSP21K Toolkit for development and debugging.

The FINE provides Gigabit Ethernet via the common options region, along with 10/100 Ethernet and an RS232 monitor port on the AMC front panel, and is connected to the FPGA via a local control bus.

Features

- High-density Altera® Stratix® IV GX FPGA implementing BittWare's ATLANTIS™ FrameWork for control of I/O, routing, and processing
 - ◆ 27 full-duplex, multi-gigabit SerDes transceivers
 - ◆ up to 530k equivalent LEs
 - ◆ up to 1,024 embedded 18x18 multipliers
 - ◆ over 20 Mbits of RAM
 - ◆ IP available for: Serial RapidIO™, PCI Express™, GigE, 10 GigE/XAUI, CPRI, and OBSAI
- BittWare's FINE™ Host/Control Bridge provides control plane processing and interface via GigE, 10/100 Ethernet, and RS-232
- Over 2 GBytes of memory
 - ◆ Two banks of DDR3 SDRAM @ up to 1 GByte each
 - ◆ Two banks of QDRII+ SRAM @ up to 9 MBytes each
- Mid-size or full-size, single wide, fully-connected AMC
 - ◆ Common Options region has four ports
 - ◆ Fat Pipes region has 16 ports
 - ◆ System synchronization via AMC system clocks
 - ◆ Module Management Control (MMC) implementing IPMI
- Front panel I/O
 - ◆ 4x SerDes via Infiniband-type connector
 - ◆ 10/100 Ethernet
 - ◆ RS-232 via Stratix IV GX
 - ◆ RS-232 via FINE
 - ◆ JTAG port for debug support
- Connectorless footprint for Agilent / Tektronix logic analyzers
- VITA 57 FMC site for processing and I/O expansion
 - ◆ Compliant with VITA 57 mezzanine standard for FPGA IO
 - ◆ 8x high-performance SerDes
 - ◆ 60 LVDS pairs
 - ◆ Six clocks



BOARD ARCHITECTURE

FPGA

- Altera® Stratix® IV GX FPGA (4SGX230/530)
- BittWare's ATLANTIS™ FrameWork
- 24 full-duplex, high-performance, multi-gigabit SerDes transceivers @ 6.25 GHz
- Three full-duplex, multi-gigabit SerDes transceivers @ 3.125 GHz
- Over 530k equivalent LEs
- Over 20 Mbits of RAM
- Over 1,024 embedded multipliers

External Memory

- Two banks of up to 1 GByte DDR3 SDRAM configured as x32
- Two banks of up to 9 MBytes QDRII+ SRAM configured as x18
- 64 MBytes of Flash memory for booting FPGA and FINE

Fat Pipes Interface

- 12 ports (4 - 11, 20 - 17) @ up to 6.25 GHz via ATLANTIS™ FrameWork, configurable to support PCI Express (Rev 1.0/2.0), Serial RapidIO (Rev 1.0/2.0), GigE, 10GigE/XAUI
- Four ports (12 - 15) of LVDS I/O (4 In, 4 Out)

Common Options Interface

- BittWare's FINE™ Host/Control Bridge providing Gigabit Ethernet on port 0

- Ports 1, 2 & 3 via ATLANTIS™ FrameWork, configurable to support PCI Express, Serial RapidIO, and GigE

Other AMC Edge Connections

- All AMC clocks brought to ATLANTIS
- Module Management Control (MMC) Interface implementing IPMI for temperature monitoring and hot-swap support
- Connectorless footprint for Agilent / Tektronix logic analyzers

AMC Front Panel I/O

- 4x SerDes via Infiniband-type connector
- 10/100 Ethernet to FINE
- RS-232 port to Stratix IV GX
- RS-232 port to FINE
- JTAG debug interface to the Stratix IV GX

VITA 57 FMC Site

- VITA 57-compliant
- 8x high-performance SerDes
- 60 LVDS pairs
- Six clocks

Size

- AMC mid-size or full-size, single width format compatible with AMC.0 specification R2.0

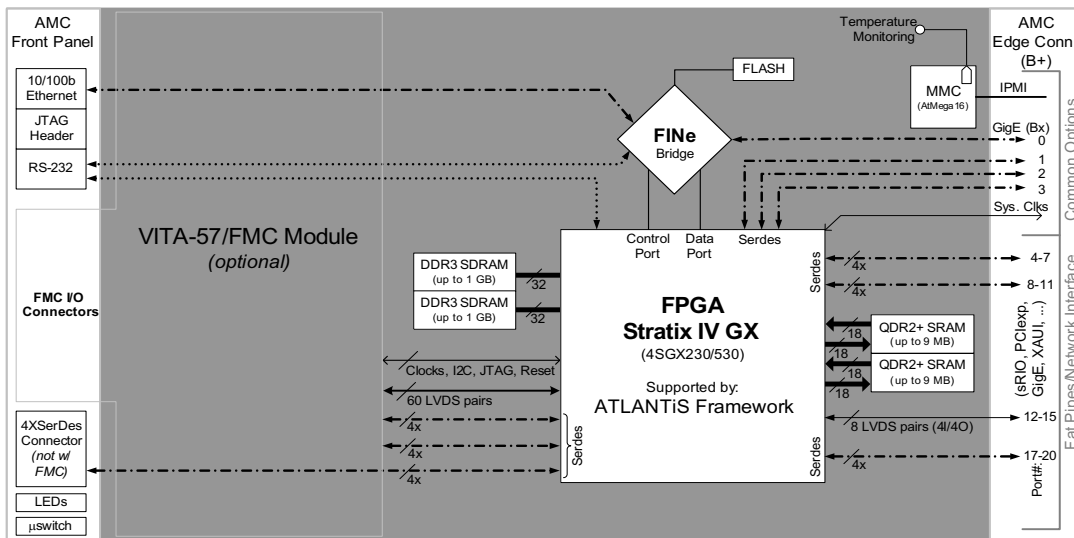
SOFTWARE SUPPORT

Host Interface

- BittWare software development kit for Windows® and Linux containing C-callable libraries for board control and communications routines
- Porting kit available for other operating system platforms

Development Tools

- Altera Quartus® II software



Ordering Information

S4AM-RW-AABB-CDEFG-HHIJK

RW: Ruggedization

0U = Commercial (0C to 50 C)*

AA: FPGA Size

23 = Altera Stratix IV GX 230 FPGA*

53 - Altera Stratix IV GX 530 FPGA†

BB: FPGA Speed Grade

C2 = Commercial Speed Grade 2

C3 = Commercial Speed Grade 3*

C4 = Commercial Speed Grade 4

I3 = Industrial Speed Grade 3

I4 = Industrial Speed Grade 4

C: DDR3 Bank A Size

0 = None

7 = 256 MB*

8 = 512 MB

9 = 1 GB

D: DDR3 Bank B Size

0 = None

7 = 256 MB*

8 = 512 MB

9 = 1 GB

E: QDRII+ Bank A Size

0 = None*

2 = 9 MB†

F: QDRII+ Bank B Size

0 = None*

2 = 9 MB†

G: FINE Flash Size

5 = 64 MB

6 = 128 MB*

HH: Front Panel

00 = No Front Panel

F1 = Full Size - VITA 57 Cutout

F2 = Full Size - SerDes Cutout*

M1 = Mid Size - VITA 57 Cutout

M2 = Mid Size - SerDes Cutout

I: Front Panel SerDes Connector

0 = Not Populated

1 = Populated*

J: VITA-57 Banks LA/HA I/O Voltage

0 = Any Vadj but 3.3V*

1 = Vadj of 2.5V or 3.3V

K: VITA-57 Bank HB I/O Voltage

0 = Any Vio-b but 3.3V*

1 = Vio-b of 2.5V or 3.3V (VITA-57 required)

* Default

† Contact BittWare for availability