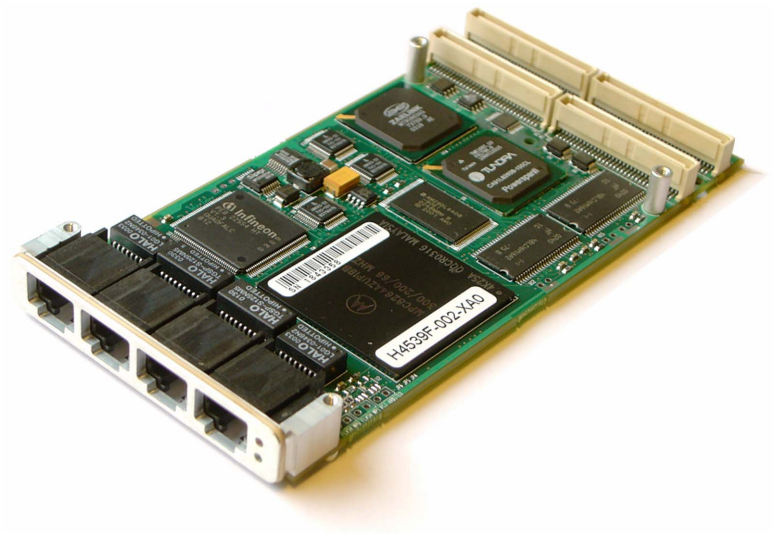
*i*SPAN® 4539F PMC T1/E1/J1 Communications Controller

Technical Product Brief



Overview

As a new generation of high-availability embedded systems emerges, the demand for robust, high-performance communications I/O modules increases. The Interphase ***i***SPAN® 4539F T1/E1/J1 Communications Controller sets the standard for high-performance as the industry's most advanced T1/E1/J1 controller for next-generation telecommunication solutions.

The ***i***SPAN 4539F Communications Controller outshines its competition with the industry's best performance, four T1/E1/J1 ports on a single card, a comprehensive array of protocol and operating system support, and robust development tools to simplify the integration process. A variety of telecommunications applications ranging from 3rd Generation Wireless to Broadband Internet Access to AIN can realize the immediate advantages of the ***i***SPAN 4539F easy integration and carrier-class features.

Main Features

The Interphase ***i***SPAN 4539F Communications Controller is a single-slot PMC network interface card equipped with four software-selectable T1/E1/J1 interfaces The controller is intended for 2G and 3G wireless networks, Internet access, and Advanced Intelligent Network (AIN) applications in a number of access arrangements, including:

- ISDN Primary Rate Interface (PRI)
- ATM AAL0, 2 and 5 over T1/E1/J1 or fractional T1/E1/J1 lines
- Frame Relay, X.25, or PPP over T1/E1/J1 or fractional T1/E1/J1 lines
- HDLC or transparent over T1/E1/J1 or fractional T1/E1/J1 lines
- Q.SAAL (SSCOP and SSCF) over ATM AAL5
- PICMG® 2.15 Configuration 0 (PMC), Configuration 2 (PT2MC) and Configuration 3 (PT3MC) compliant
- SS7 MTP1 and MTP2 LSL processing on multiple DS0 channels or HSL over full T1/E1/J1 lines
- Smart communications card, featuring the Motorola MPC8264A 32-bit RISC processor operating at 300 MHz clock speed
- Four shielded or unshielded ports, software programmable as T1, E1, or J1
- Four DSX1 ports on the front panel
- 64 MB of SDRAM memory upgradeable to 128 MB, 16 MB of flash EPROM
- 32-bit 33/66 MHz PCI Bus Interface
- "Pass through" capability (Line 1 to (or from) line 2, line 3 to (or from) line 4) for snooping applications
- PCI 2.2 master/target bus interface, high performance transfers via four DMA channels
- Comprehensive hardware Board Development Kit (BDK)
- Software Development Suites for Sun™ Solaris™ 8 and 9 (SPARC®) and Linux® 2.4.x

Configuration Options

The following configurations are currently available. Each configuration is equipped with four front-access T1/E1/J1 ports (shielded or unshielded) as indicated), interface as indicated, a Motorola 8264A (HiP 4) processor, up to 128 MB main system memory, 4 MB Boot Memory, TTY port, and JTAG port as indicated:

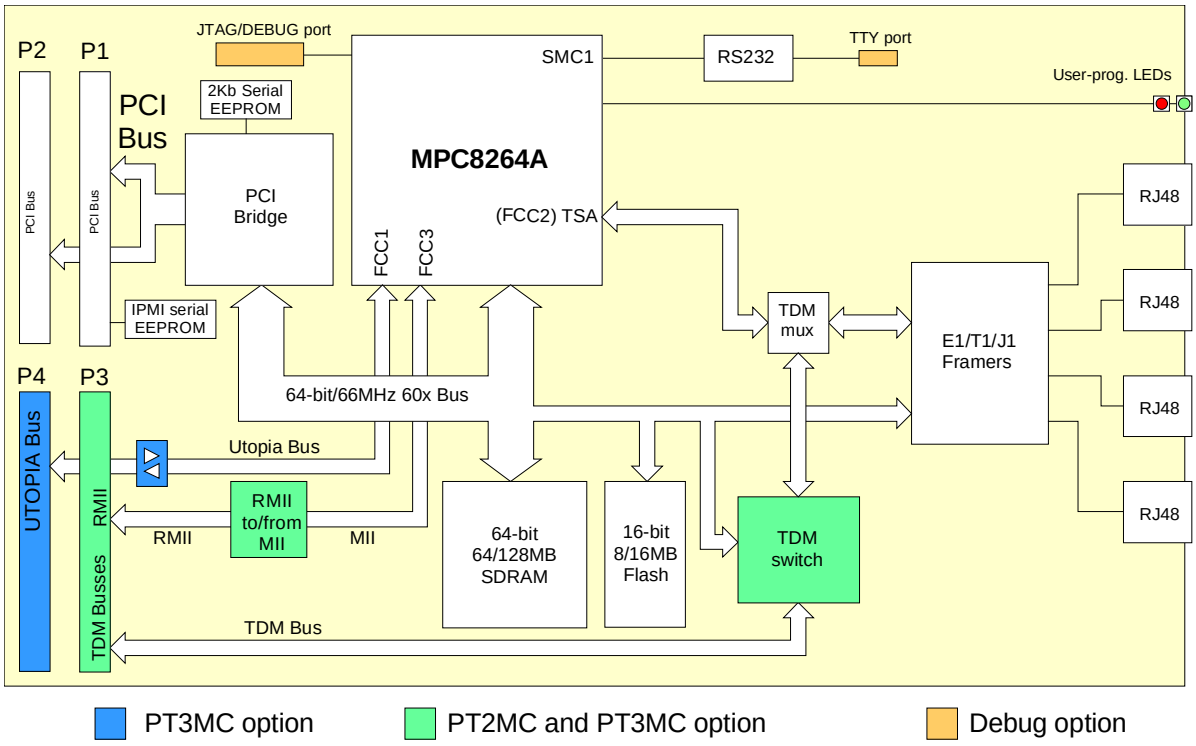
Configuration	PTMC PMC	Shielded	Debug Port
4539F-000	PT2MC	No	No
4539F-001	PT2MC	No	JTAG
4539F-002	PT2MC	Yes	No
4539F-003	PT2MC	Yes	JTAG
4539F-004	PT3MC	No	No
4539F-005	PT3MC	No	JTAG
4539F-006	PT3MC	Yes	No
4539F-007	PT3MC	Yes	JTAG
4539F-008	PMC	No	No
4539F-009	PMC	No	JTAG
4539F-010	PMC	Yes	No
4539F-011	PMC	Yes	JTAG

Professional Services

Custom software development, integration, and consulting services are also available via the Interphase Professional Services Group.With over 100 man years of development experienced amassed, the professional services team offers everything from completely custom development to merely customizing standard Interphase products to meet your specific needs.

Hardware Description

Block Diagram



On-Board Processor, Memory

The 4539F is equipped with a powerful on-board communications processor, the Motorola MPC8264A. This networking processor is made of three major parts: an MPC603e RISC core running at 300 MHz, a System Interface Unit (SIU), and a Communication Processor Module (CPM) operating at 200 MHz. The CPM co-processor can implement a variety of communications protocols at aggregate speeds of up to 700 Mbps.

The MPC603e core is derived from the PowerPC™ 603e core and includes mainly the integer core and the 16 KB data and 16 KB instruction caches.

The System Interface Unit includes a memory management unit and enables the control of the 64-bit wide local bus. On this local bus are tied the PCI bridge, the main SDRAM memory (up to 128 MB), the Flash EEPROM memory, and the line framer.

The communication processor (CPM) features:

- Two Multi-channel Communications Controllers (MCCs) handling up to 256 HDLC/transparent channels at 64 Kbps each, multiplexed on up to eight TDM busses.
- Three full-duplex fast serial communications controllers (FCCs). On the 4539F, an FCC is used to control the Fast Ethernet port.
- Four Serial Communication Controllers (SCCs)
- Two Serial Management Controllers; one used as UART for a TTY connection.
- A Time-Slot Assigner (TSA) for multiplexing data from any of the SCCs, FCCs, SMCs, and MCCs onto four Time-Division Multiplexed (TDM) interfaces. The 4539F can terminate all four T1/E1 or J1 channels into the TSA.
- A debug serial port
- Four timers and an interrupt controller

The 4539F is equipped with 64 MB of SDRAM main memory, and 16 MB of field-programmable Flash EPROM.

System Bus Interface

A dedicated PCI bridge, the Tundra PowerSpan, controls the interface between the 32-bit PCI bus and the 64-bit local processor 60x bus on the 4539F. The PowerSpan implements all the registers specified by the PCI 2.2 standard. The chip supports “Target” and “Master” accesses between the PCI bus and the local 60x bus.

The bridge chip implements windows as well as other mechanisms to interface between the PCI host and the 4539F controller. Exchanges between the two can use any of the following mechanisms available from the PowerSpan:

- Runtime registers (mailboxes, doorbells)
- Memory windows between the Local space and the PCI space
- Four independent bi-directional DMA engines with linked-list capability
- An I²O messaging unit

T1/E1/J1 Line Interfaces and Framers

One Infineon QuadFALC chip controls the four E1/T1/J1 line interfaces. The QuadFALC supports long haul or short haul interface, AMI, HDB3, or B8ZS line coding and various Super-Frame Formats (SFFs), allowing the 4539F to be software configurable in T1, E1, or J1 mode. Each line is also individually software configurable in "Line Termination" mode (LT: clock slave) or "Network Termination" mode (NT: clock master).

Four line interfaces are provided on the front with standard RJ48C connectors, or four line interfaces are provided on PMC connector P4, for connection to a rear I/O card. When using the rear access, the interfaces include the line protection to comply with ETS300 046-3, UL1459, FCC68, and Bellcore TR-NWT-001089.

Telecom Clock Management

The 4539F can select a synchronization source from any T1/E1/J1 line. Each line can also be configured as the master of its clock rhythm or as a clock slave.

The 4539F can support any mix of clock slave or clock master line configuration and support four independent line clocks.

The 4539F can provide its own fixed frequency clock rhythm or the rhythm can come from the carrier card through the PMC P4 connector, or the rhythm can be derived from the one of the four lines receive signal.

When the card uses the line receive clock rhythm, it de-jitters it to generate the transmit clock rhythm. The card will provide this received line rhythm to the carrier card through the PMC P4 connector

I/0 and Connectors

PMC connectors P1 and P2 support the 32-bit PCI bus as defined by the PMC standards.

Connector P3 is used for local CT (TDM), with pin-outs per PICMG 2.15 R 1.0 as required for PT2MC and PT3MC, depending on configuration.

P4 is used for user-defined I/O and UTOPIA bus (8-bit data path interface and multi-PHY) as required per configuration.

Environmental and Mechanical

The 4539F is powered by +3.3V available from the PMC PCI connectors.

The 4539F complies with the following standards:

- FCC part 15 class A
- CE class A
- EN 55022
- EN 60950
- FCC part 68
- CS03

4539F Software Development Support

The 4539F is available with two levels of software support:

- The first level is intended for software developers building their own embedded firmware on the 4539F processor, and their own 4539F drivers and APIs on the host CPU. To these customers, Interphase offers the Board Development Kit (BDK), an OS-independent hardware development tool.
- The second level of custom support is targeted for developers that intend to use the Interphase-embedded firmware protocol stacks under the APIs provided by Interphase. The tool is called a Software Development Suite (SDS), and it provides a complete set of software solutions, including onboard software, drivers for different operating systems, and several software utilities and sample programs with sources.

4539F Board Development Kit

The 4539F Board Development Kit includes a set of documents which provide valuable information, hardware description, and software implementation directives, as well as source examples. They describe the specification of the Interphase 4539F boot code provided in the FLASH memory. All the sources as well as the compilation environment for this boot code are also provided as an example for custom development. The 4539F BDK is specific to the 4539F hardware, but it is not tied to a particular operating system environment. The documentation set is composed of the following documents:

- Board Installation and Maintenance Manual: Provides procedures for installing and maintaining the module.
- Hardware Reference Manual: Provides 4539F hardware description and information for developing embedded software and/or host drivers for the module.
- Built-in Self Test and Monitor Manual: Provides high-level information for using the Boot Firmware.

A set of utilities running under several standard operating systems (Solaris, Linux, and VxWorks) are also provided. These utilities can be used to modify the content of the various programmable elements of the board, especially the FLASH EEPROM memory and to get access to the boot firmware console through the PCI bus and to get access to boot firmware configuration and self-test diagnostics.

4539F Software Development Suite

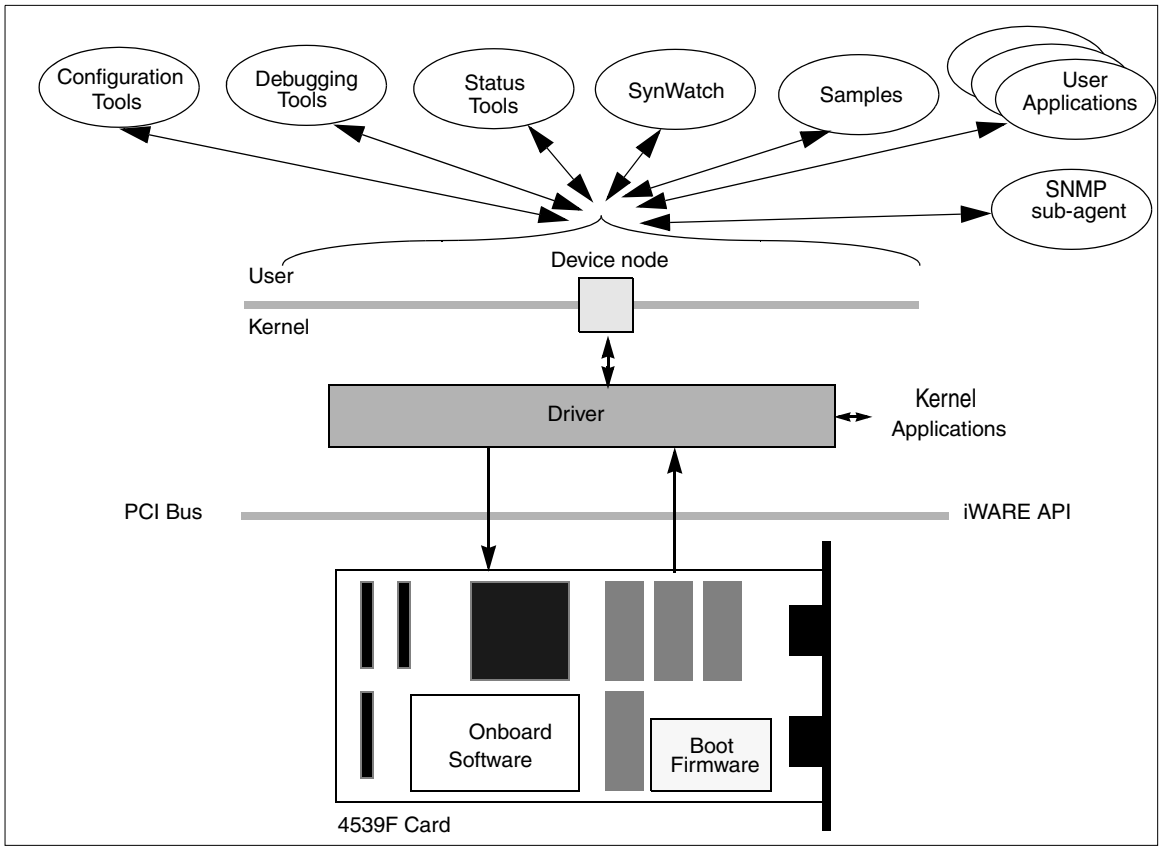
The 4539F Software Development Suite (SDS) available from Interphase consists of software programs and utilities running on the host CPU, and embedded software (“firmware”) which runs on the on-board networking processor. 4539F SDSs are available for Solaris SPARC and for Linux PowerPC and Intel x86 processors.

The 4539F Software Developers Suite includes the following:

- User and Kernel API
- Onboard Software file to be loaded on the cards

- A configuration tool to dynamically set up the cards
- Tools to flash an Onboard Software and its initial software configuration in the card memory
- The SynWatch™ WAN protocol analyzer
- Tools to monitor line status
- Tools to monitor and log card/port status
- A SNMP sub-agent.
- Debugging tools
- PCI console application to run tests on the cards
- Several application samples

The following figure presents a general view of the 4539F SDS software package architecture:



4539F Software Development Suite Software Package Architecture

The Onboard Software handles the communications on the controller. The Onboard Software and its initial software configuration can be either dynamically loaded from the host or they can be stored in the Flash EEPROM so that the card boots and configures itself automatically, without any host action.

The driver runs in kernel space and provides either a User Application Programming Interface (API) (through `open/close/ioctl/select` standard UNIX functions) or a Kernel API (through `iph_kernel_open/iph_kernel_close/iph_kernel_ioctl` kernel entry points).

The device nodes are special files used by the user applications to dialog with the cards. The device driver automatically creates one `/dev/iph_wan_x` device node per card.

Several tools are provided with the 4539F SDS:

- A configuration tool that can be used to download and configure an Onboard Software on a communications controller.
- The `iphDumpCardList` utility that displays all the available device nodes.
- The `iphMonitor` PCI console application is provided to communicate with the Boot Firmware and run some of the Power-On Self Tests (POST) at card boot time. This can be used to diagnose any hardware problem.
- SynWatch is a WAN protocol analyzer used to dump in a file and interpret all the exchanges on the physical line.
- `iphlinestat` is a tool used to monitor activity on a physical T1/E1/J1 line. `iphlinetest` is a utility used to test a physical T1/E1/J1 line.
- `iphPortStatd` is a daemon that monitors all the T1/E1/J1 Interphase Communication Controllers found in the local machine and logs and displays all of their status changes.
- Other tools are supplied to help developers debug their software applications running over Interphase Communication Controllers.

Samples illustrate the dialog with the cards through the device driver. Both user and kernel API samples are provided. Samples are provided in both binary and source formats

A complete documentation set is also provided with the Software Development Suite. The documentation describes the Interphase ***i***WARE API (***i***WARE Application Programmer's Interface) with the onboard software, the Driver API, and sample programs and tools users guides.

Driver

The driver is dynamically loadable and un-loadable.

The driver is multi-communications controller, multi-application. It can support:

- Up to four communications controllers
- Up to 256 concurrent applications per device, this limit can be changed in the configuration file
- Up to 1024 concurrent applications for all communications controllers
- Up to 4096 concurrent sessions per application, this limit can be changed in the configuration file

The driver performs DMA transfers with the cards for large data exchanges.

Configuration Tool

The configuration utility (`iphConfigure`) is used to set up driver parameters, dynamically load an onboard software on a card, and set up the initial software configuration of the onboard software. The initial configuration must be done each time a card is reset in order to give the onboard software information about the type of line used to connect to the WAN.

The parameters used to configure the driver and the card are specified in a configuration file.

Debugging Tools

The 4539F SDS is provided with several dump utilities to use for monitoring the card. These utilities can be used to view:

- A list of available 4539F controllers in the system and a list of the applications that use them.
- The 4539F onboard memory and host driver memory usage information.
- The driver or onboard software debug traces.
- The onboard software configuration.
- The 4539F CPU performance usage.
- The 4539F PCI registers.

Status Tools

Line Status utility

`iphlinestat` enables the user to watch the status of the lines handled by one or several communications controllers, that is, to see what is wrong when a problem occurs with one or the other communications controller.

This status is made of:

- The *loopback* state.
- The *alarms* state: Connecting problems may result from line failures, known as DS1 alarms, like LOS, LOF, AIS, or RAI.
- *Errors* counters, like BPV, PCV, or CS.

Each time one of the above states changes on a line, a new line of text is displayed for that port.

Line Test Utility

`iphlinetest` enables the user to test a line connected on any port of a 4539F by activating a low-level loop back mode (at line or payload level) or a PRBS (Pseudo-Random Bit Sequences) test.

Line Status Daemon

The Status Monitor Daemon is an application that continuously polls all the cards found in the local machine in order to monitor and log any status changes of these cards. All the messages logged by the Status Monitor Daemon are time stamped. They are logged in a text file and can simultaneously (if enabled) be displayed on the console. The information logged is:

- Card status
- List of available ports and list of configured channels
- Alarms
- Errors

Synwatch

SynWatch: This is a protocol analyzer, that can display the frames exchanged on the line and analyze their contents. Frame Relay, SS7 MTP2, ATM, SSCOP, and HDLC protocols can be interpreted. Data can be displayed in real time or stored in a file for off-line analysis.

SNMP Sub-Agent

The 4539F SDS includes a SNMP sub-agent which is tied to the host's system master agent, allowing any SNMP client access to onboard software internal statistics variables. The sub-agent converts the requests received from the system SNMP master agent into ***i***WARE requests to get the information from the 4539F onboard software and interprets the response before replying to the master agent.

Each protocol layer in the onboard software maintains SNMP Management Information Bases (MIBs). The statistic parts of the following MIBs are supported:

- DS1 MIB (RFC 1406)
- FR MIB (RFC 2115)
- SS7 MTP2 MIB
- ATM MIB (RFC 1695)
- SSCF and SSCOP MIBs
- Private enterprise MIB

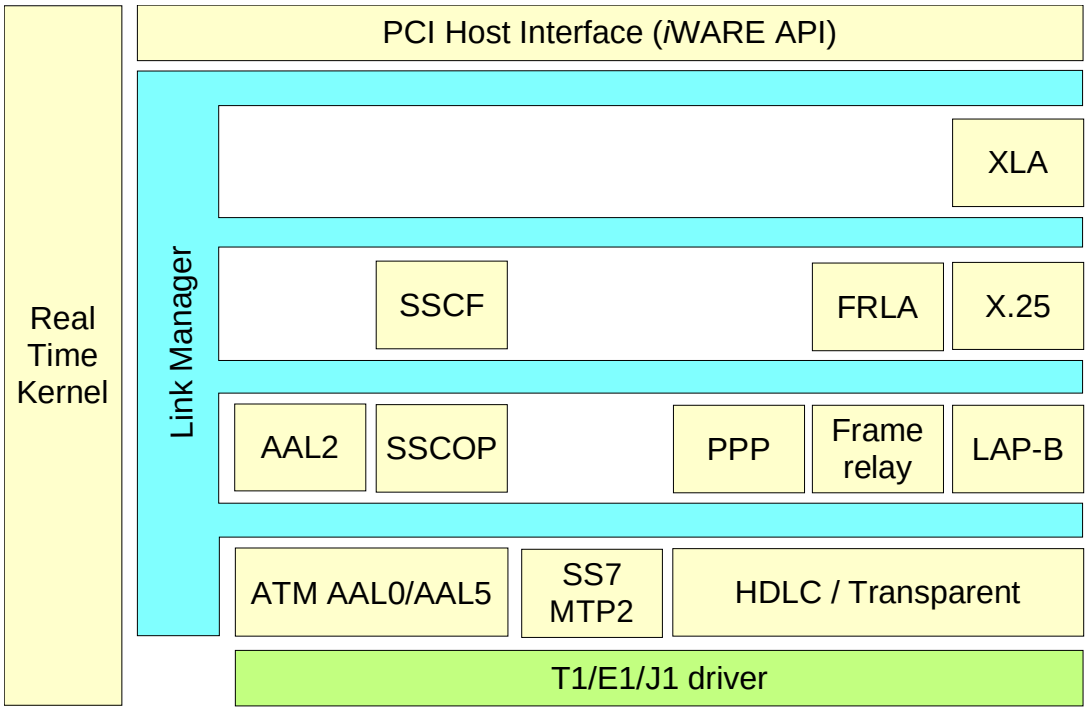
All these MIBs appear in the Interphase private branch. The 4539F MIB files are provided in the 4539F SDS package.

Samples

The 4539F SDS provides several samples that can be done as a way to better understand the ***i***WARE API and as a base for the development of a new application. The samples demonstrate both the User API and Kernel API, use almost all the protocol layers provided in the 4539F onboard software, and is provided both in binary and source format.

4539F Onboard Software

The following is a block diagram of the onboard software running on the 4539F 8264A processor:



4539F Onboard Software Block Diagram

The onboard software consists of various communications protocol stacks, a link manager, and a constant, unified interface to the host (*i*WARE API). All the onboard software supplied by Interphase runs under the control of a small, proprietary real-time kernel. Interphase software is packaged as a Software Development Suite.

The 4539F Software Development Suite integrates the following protocols:

- SS7 MTP2 and MTP1, both LSL and HSL
- HDLC/Transparent
- ATM AAL0, AAL2, and AAL5
- Q.SAAL (SSCOP, SSCF)
- Frame Relay

The following protocols are available for integration from Interphase Professional Services:

- PPP
- X.25
- ISDN

HDLC/Transparent Protocol

The HDLC and transparent protocol can be implemented on each individual DS0 channel of the 4539F, or on any aggregation of DS0s when the 4539F is connected to channelized, unchannelized, or fractional T1/E1/J1 lines. Up to 248 (a full eight E1, T1, or J1 lines) HDLC or transparent channels can be activated simultaneously.

SS7 MTP2

The 4539F Communications Controller supports multi-channel SS7 connections over multiple channelized T1, E1, or J1 lines. An Interphase implementation of SS7 MTP1 and MTP2 is included with the Interphase embedded firmware running on the on-board processor.

Interphase MTP2 implements the entire layer 2 functionality, including FISUs stuffing/elimination, Link Synchronization, and error management. MSUs and OAM services are relayed to layer 3 MTP3, normally run on the host CPU. The SS7 embedded firmware is able to handle up to 128 simultaneous MTP2 sessions.

Interphase implementation of SS7 MTP2 conforms to ITU-T, ANSI, and TTC standards.

ATM

The 4539F onboard software includes an ATM layer, which implements the following sub-layers:

- ATM protocol sub-layer, including cell delineation, VPI/VCI translation, handling of alarm and loopback OAM cells, traffic shaping
- The AAL0 null adaptation layer
- The AAL2 common part and service specific convergence sub-layers (CPS and SSSAR)
- The AAL5 Segmentation And Reassembly protocol sub-layer (SAR)

The Interphase ATM provides support of CBR, UBR, rt-VBR, rnt-VBR, ABR, and GFR Quality of Service classes.

Interphase implementation of ATM conforms to the following standards:

- I.361 B-ISDN ATM layer specification, ITU-T 1996
- I.362 B-ISDN ATM adaptation layer (AAL) functional description, ITU-T 1996
- I.363.2 B-ISDN ATM Adaptation Layer specification : Type 2 AAL, ITU-T 1996
- I.363.5 B-ISDN ATM Adaptation Layer specification : Type 5 AAL, ITU-T 1996

Q.SAAL

The 4539F Communications Controller onboard software provides Q.SAAL support, to transport Signaling over ATM AAL5 links. The Q.SAAL support is a set of the two following protocol layers:

- SSCOP
- SSCF at NNI

Interphase implementation of Q.SAAL conforms to the following standards:

- ITU-T Q.2110 (07/94) B-ISDN ATM Adaptation layer – Service Specific Connection Oriented Protocol (SSCOP)
- ITU-T Q.2140 (02/95) B-ISDN ATM Adaptation layer – Service Specific Coordination Function for Signaling at the Network Node Interface (SSCF at NNI)

Frame Relay

The 4539F Communications Controller supports an embedded frame relay stack that is compliant with ITU-T Q.933 and ITU-T Q.922. The Interphase implementation includes:

- DLCI management (user defined, automatic)
- Frame size up to 4096 bytes
- Quality of Service management (CIR, Bc, Be, T)
- Congestion management (BECN, FECN, DE)
- User side of the User to Network interface
- Unicast only
- PVC only (up to 976 user's DLCI)

PPP

The 4539F Communications Controller supports a Point-to-Point Protocol (PPP) stack, which provides a standard method to transport multi-protocol datagrams over point-to-point links. Interphase PPP implementation complies with the following RFCs:

- 1661 (Point-to Point Protocol)
- 1662 (PPP in HDLC-like Framing)
- 1570 (PPP LCP Extensions)
- 1333 (PPP Link Quality Monitoring)
- 1334 (PPP Authentication Protocols)
- 1717 (PPP Multilink Protocol)

The 4539F supports encapsulation of TCP/IP via RFC 1332 (PPP Internet Protocol Control Protocol) and of IPX via RFC 1552 (the PPP Internetwork Packet Exchange Control Protocol).

X.25

The X.25 protocol is used to connect Data Terminal Equipment (DTE) to Packet Switched Data Networks. The 4539F module can be equipped with software providing Layers 2 and 3 of X.25 in compliance with ISO8208, ISO7776, and ITU-T X.25. The Interphase X.25 implementation includes:

- Frame size up to 4096 bytes
- Up to 256 CVs
- IP and IPX over X.25 (RFC 1356)
- Modulo 8 and modulo 128 numbering
- IP and IPX over Frame Relay (RFC 1490)

ISDN Signaling

The Interphase-supplied signaling stack is compliant with all major national ISDN standards, specifically EuroISDN and CE (with French and German complementary approvals), NI-1, NI-2 (Lucent Technologies 5ESS® and Nortel Networks DMS 100), Austel (Australia), NTT (Japan), plus numerous other country-specific approvals.

Management

The 4539F onboard software provides the two different management mechanisms, SNMP and Supervision.

Each protocol layer in the firmware maintains a set of variables that can be accessed through a specific API. The Software Development Suite SNMP sub-agent uses these variable SNMPs to maintain the MIB.

The supervision is a proprietary API that can be used by application and Interphase tools to access internal variables or to get status information about the onboard software.

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