# *i*SPAN™ 4539 PMC T1/E1/J1 Communications Controller

*Technical Product Brief*

## Overview

As a new generation of high-availability embedded systems emerge, the demand for robust, high-performance communications I/O modules increases. The Interphase ***i***SPAN 4539 PMC T1/E1/J1 Communications Controller sets the standard for high-performance as the industry's most advanced T1/E1/J1 controller for next-generation telecommunication solutions.

The ***i***SPAN 4539 Communications Controller outshines its competition with the industry's best performance, a comprehensive array of protocol and operating system support, and robust development tools to simplify the integration process. A variety of telecommunications applications ranging from 3rd Generation Wireless to Broadband Internet Access to AIN can realize the immediate advantages of the 4539 easy integration and carrier-class features.

# Main Features

The Interphase ***i***SPAN 4539 Communications Controller is a single-slot PMC network interface card equipped with rear access (using a Rear Transition Module) for four software-selectable T1/E1/J1 interfaces, and a fast Ethernet interface for remote boot or LAN capability with support of 10BaseT/100BaseT auto-negotiation and parallel detection. The controller is intended for 2G and 3G wireless networks, Internet access, and Advanced Intelligent Network (AIN) applications in a number of access arrangements, including:

- ISDN Primary Rate Interface (PRI)
- Frame Relay, X.25, or PPP over T1/E1/J1 lines
- ATM over T1 with Inverse Multiplexing for ATM (IMA)
- SS7 MTP1 and MTP2 processing on multiple DS0 channels
- Smart communications card, featuring the Motorola® MPC8264A PowerQUICC II™ 32-bit RISC processor operating at 300 MHz clock speed
- Four ports, software programmable as T1, E1, or J1
- Integrated CSU (with Rear Transition Module)
- Four DS1 interfaces
- 64 MB of SDRAM memory, 4 MB of flash EEPROM
- 8 MB of connection memory for storage of ATM connection parameters
- 16K x 64 Content Addressable Memory (CAM)
- 32-bit 33 MHz PCI Bus Interface
- UTOPIA bus on PMC connector P3 (PTMC configuration 1)
- Local TDM busses provided on PMC connector P4 for time slot switching on the carrier card
- “Pass through” capability (Line 1 to (or from) line 2, line 3 to (or from) line 4) for snooping applications
- PCI 2.2 master/target bus interface, high performance transfers via four DMA channels
- Ethernet 10/100BaseT port on front panel
- RS232 TTY port on front panel
- Comprehensive hardware Board Development Kit (BDK)
- VxWorks® Board Support Package (BSP) for custom protocol or applications development

# Configuration Options

The following configurations are currently available:

**4539-006:** PMC Quad E1/T1/J1 IMA Communications Controller, MPC8264A processor @ 300 MHz, 64 MB SDRAM, 16 K CAM

**4539-007:** PMC Quad E1/T1/J1 IMA Communications Controller, MPC8264A processor @ 300 MHz, 64 MB SDRAM, 16 K CAM, JTAG connector

**6435-009:** Rear Transition Module 4 port T1/E1, Keyed (keyed connectors) (see **Note**) (used when the 4539 is in a PMC site connected to J5 (upper))

**6435-010:** Rear Transition Module 8 port T1/E1, Keyed (keyed connectors) (see **Note**)

**6435-011:** Rear Transition Module 4 port T1/E1, Non-Keyed (non-keyed connectors) (see **Note**) (used when the 4539 is in a PMC site connected to J5 (upper))

**6435-012:** Rear Transition Module 8 port T1/E1, Non-Keyed (non-keyed connectors) (see **Note**)

**3039-000:** Rear Transition PIM Module, 4 port T1/E1, Unshielded

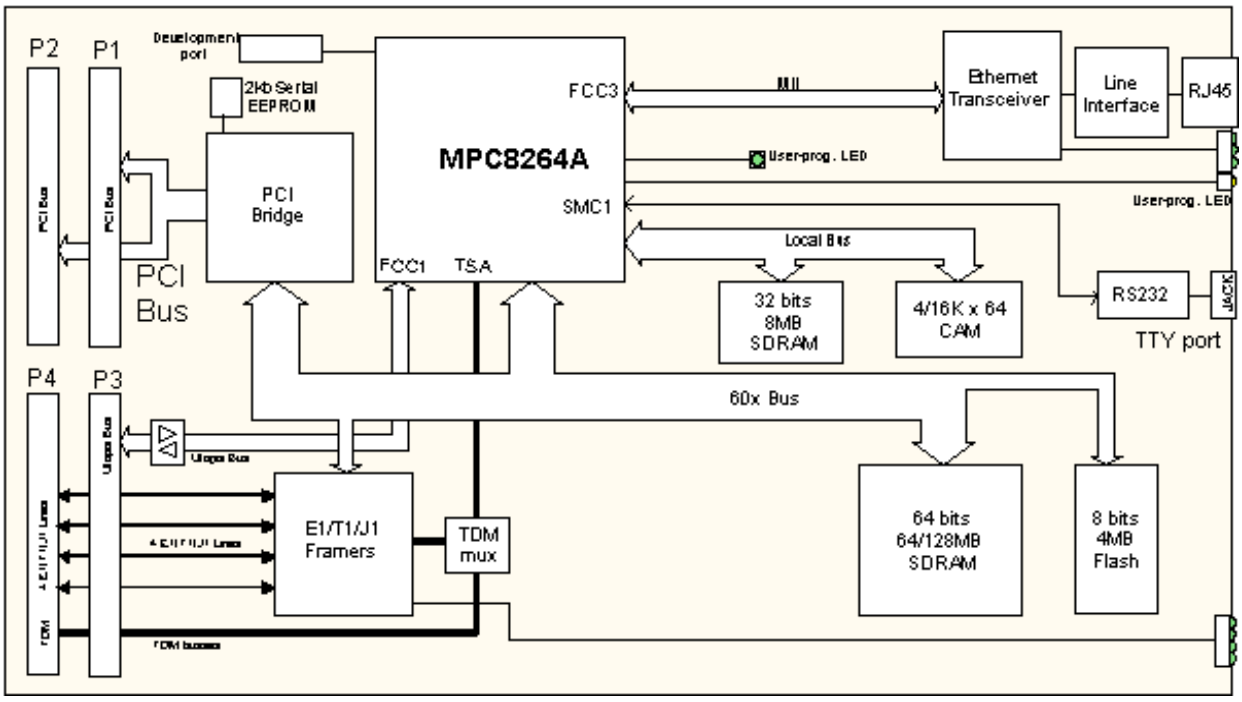
**3039-001:** Rear Transition PIM Module, 4 port T1/E1, Shielded

## *NOTE*

**Keyed connectors refers to Reference Designator J3 and J5 on the Rear Transition Module only. In the 6435-011 and -012, J3 and J5 are populated with non-keyed connectors; in the 6435-009, and -010, J3 and J5 are populated with keyed connectors.**
**Keyed connectors have an alignment tab in the connector that helps align the pins in the connector with the pins of the chassis backplane. The tabs on the connectors mate with slots in the backplane connectors to prevent connector/chassis pins from being bent.**

# Hardware Description

## Block Diagram




## On-Board Processor, Memory

The ***i***SPAN 4539 is equipped with a powerful on-board communications processor, the Motorola MPC8264A. This networking processor is made of three major parts: an MPC603e RISC core running at 300 MHz, a System Interface Unit (SIU), and a Communication Processor Module (CPM) operating at 200 MHz. The CPM co-processor can implement a variety of communications protocols at aggregate speeds of up to 700 Mbps.

The MPC603e core is derived from the PowerPC™ 603e core and includes mainly the integer core and the 16 KB data and 16 KB instruction caches.

The SIU includes a memory management unit and enables the control of the 64-bit wide local bus. On this local bus are tied the PCI bridge, the main SDRAM memory (up to 128 MB), the Flash EEPROM memory, and the line framer.

The CPM features:

- Two Multi-channel Communications Controllers (MCCs) handling up to 256 HDLC/transparent channels at 64 Kbps each, multiplexed on up to eight TDM busses.
- Three full-duplex Fast serial Communications Controllers (FCCs). On the 4539, an FCC is used to control the Fast Ethernet port.

- Four Serial Communication Controllers (SCCs)
- Two Serial Management Controllers; one used as UART for a TTY connection.
- A Time-Slot Assigner (TSA) for multiplexing data from any of the SCCs, FCCs, SMCs, and MCCs onto four Time-Division Multiplexed (TDM) interfaces. The 4539 can terminate all four T1, E1, or J1 channels into the TSA.
- A debug serial port
- Four timers and an interrupt controller

The 4539 is equipped with 64 MB of SDRAM main memory and 4 MB of field-programmable Flash EEPROM.

## System Bus Interface

A dedicated PCI bridge, the Tundra® PowerSpan™, controls the interface between the 32-bit PCI bus and the 64-bit local processor 60x bus on the 4539. The PowerSpan implements all the registers specified by the PCI 2.2 standard. The chip supports “Target” and “Master” accesses between the PCI bus and the local 60x bus.

The bridge chip implements windows as well as other mechanisms to interface between the PCI host and the 4539 controller. Exchanges between the two can use any of the following mechanisms available from the PowerSpan:

- Runtime registers (mailboxes, doorbells)
- Memory windows between the Local space and the PCI space
- Four independent bi-directional DMA engines with linked-list capability
- An I²O messaging unit

## T1/E1/J1 Line Interfaces and Framers

One Infineon QuadFALC™ chip controls the four E1/T1/J1 line interfaces. The QuadFALC chip supports long haul or short haul interface, AMI, HDB3, or B8ZS line coding and various Super-Frame Formats (SFFs), allowing the 4539 to be software configurable in T1, E1, or J1 mode. Each line is also individually software configurable in “Line Termination” mode (LT: clock slave) or “Network Termination” mode (NT: clock master).

Four line interfaces are provided on PMC connector P4, for connection to a rear I/O card. The interfaces include line protection to comply with ETS300 046-3, UL1459, FCC68, and Bellcore TR-NWT-001089.

## Telecom Clock Management

The 4539 can select a synchronization source from any T1/E1/J1 line. Each line can also be configured as the master of its clock rhythm or as a clock slave.

The 4539 can support any mix of clock slave or clock master line configuration. The four lines can have independent clock rhythms.

The 4539 can provide its own fixed frequency clock rhythm or the rhythm can come from the carrier card through the PMC P4 connector, or the rhythm can be derived from the one of the four lines receive signal.

When the card uses the line receive clock rhythm, it de-jitters it to generate the transmit clock rhythm. The card will provide this received line rhythm to the carrier card through the PMC P4 connector

## I/0 and Connectors

PMC connectors P1 and P2 support the 32-bit PCI bus as defined by the PMC standards.

P3 and P4 connectors are used according with the PICMG 2.15
"PCI Telecom Mezzanine Card" (PTMC) standard R1.0, configuration 1:

- On P3 there is an ATM UTOPIA bus, connected to FCC1 of the PowerQUICC II. FCC1 can appear as a "PHY" (UTOPIA slave) or as an ATM layer (UTOPIA master).
- PMC connector P4 supports the four E1/T1/J1 lines and the two TDM busses with clocks and synchronization signals.
- One Ethernet 10/100 RJ45 connector on the front panel.
- One TTY jack connector on the front panel

## Environmental and Mechanical

### Power

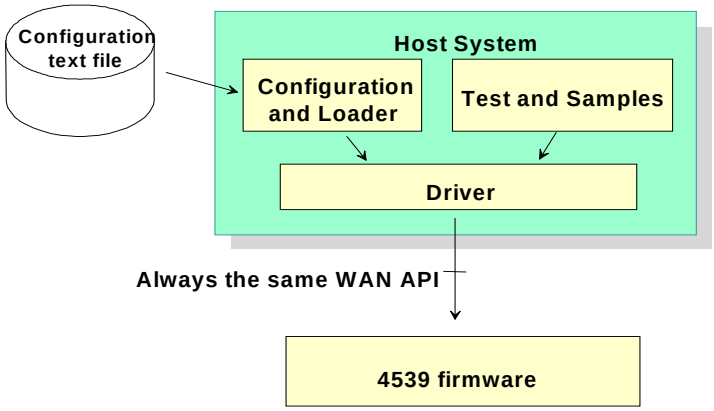
- **3.3 V:** 8.1 W maximum
- **5 V:** Less than 50 mW

The 4539 complies with the following standards:

- FCC part 15 class A
- CE class A
- EN 55022
- EN 60950
- FCC part 68
- CS03

# 4539 Software Architecture

The software supplied with the 4539 module consists of software programs and utilities running on the host CPU, and embedded software ("firmware") that runs on the 4539 on-board 8264A networking processor. A common ***i***WARE WAN API is defined at the interface between the embedded firmware and the various drivers. See the following block diagram:




**4539 Software Block Diagram**

## Base Driver

The base driver running on the host CPU, is responsible for exchanging data between the 4539 local memory and host memory. Those transfers take advantage of the Master DMA capabilities of the 4539 PCI bridge.

## Installation/Configuration

This module is responsible for the field downloading/upgrading of the embedded firmware into the 4539 resident SDRAM memory. The module also updates the 4539 configuration database defined by the host CPU.

## Diagnostics/Utilities

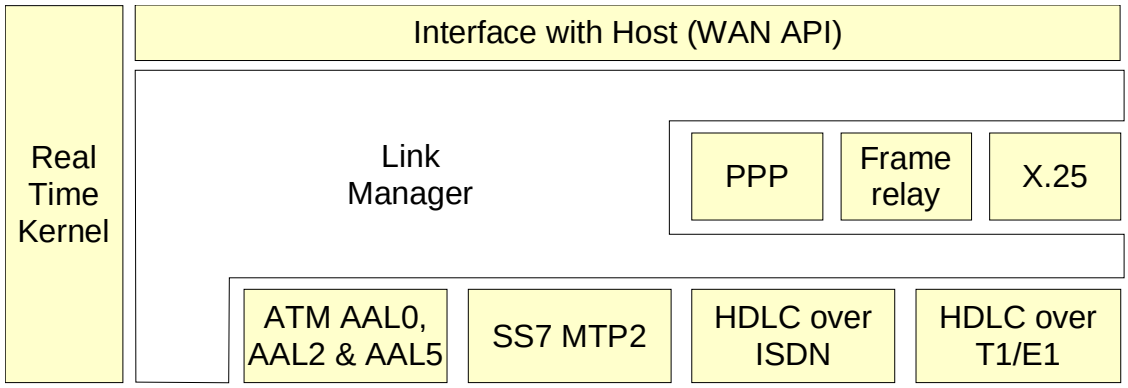
Depending on the embedded protocol stacks, various utility software modules are available, such as:

- SynWatch: This is a protocol analyzer, that can display the frames exchanged on the line and analyze their contents. PPP, X.25, Frame Relay, SS7 MTP2, ATM, SDLC, and QLLC protocols can be interpreted. Data can be displayed in real time or stored in a file for off-line analysis.

- Dump and trace utilities: Various utilities are provided to dump the board's SDRAM memory, PCI registers, and get firmware traces to help developers debug their application.

## 4539 Embedded Firmware Block Diagram

The following is a diagram of the software running on the module's 8264A processor:




The software consists of various communications protocol stacks, a link manager, and a constant, unified interface to the host. All the embedded software supplied by Interphase runs under the control of a small, proprietary real time kernel. Alternatively, when there is a need for a full-featured OS running on the 8264A processor, the kernel can be replaced with an embedded Real Time OS (VxWorks). For this case Interphase offers a Board Support Package.

The following protocols are available from Interphase Professional Services. Brief descriptions of each can be found in subsequent paragraphs:

- ATM AAL0, AAL2 and AAL5
- SS7 MTP2 and MTP1
- ISDN
- HDLC/Transparent
- PPP, X.25, and Frame Relay
- SNMP

## ATM

When connecting the 4539 module to ATM based networks through T1/E1/J1 lines (ATM over T1/E1/J1), the 4539 makes extensive use of the 8264A CPM integrated ATM SAR. The Interphase 4539 ATM protocol support covers AAL0, AAL2, and AAL5 Common Part Convergence Sublayer (CPCS) APIs.

Restricted allocation of up to 64K VPI/VCI numbers is supported via an internal Address Compression Mechanism. The 4539 ATM firmware offers the following additional features:

- AAL5, AAL2 and AAL0 interface
- OAM support

- CBR, VBR, ABR (ATM Forum UNI 4.0), and UBR service classes
- ATM MIB (RFC 1695) support

## SS7 MTP2

The 4539 Communications Controller supports multi-channel SS7 connections over multiple channelized T1, E1, or J1 lines. An Interphase implementation of SS7 MTP1 and MTP2 is included with the Interphase embedded firmware running on the on-board processor.

Interphase MTP2 implements the entire layer 2 functionality, including FISUs stuffing/elimination, Link Synchronization, and error management. MSUs and OAM services are relayed to layer 3 MTP3, normally run on the host CPU. The SS7 embedded firmware is able to handle up to 128 simultaneous MTP2 sessions.

Interphase implementation of SS7 MTP2 conforms to ITU-T, ANSI, and TTC standards.

## ISDN Signaling

The Interphase-supplied signalling stack is compliant with all major national ISDN standards, specifically EuroISDN and CE (with French and German complementary approvals), NI-1, NI-2 (Lucent Technologies 5ESS® and Nortel Networks® DMS™ 100), Austel (Australia), NTT (Japan), plus numerous other country-specific approvals.

## HDLC Protocol /Transparent Mode

The HDLC/transparent mode can be implemented on each individual DS0 channel of the 4539, or on any aggregation of DS0s when the 4539 is connected to ISDN PRI lines, or to channelized, unchannelized, or fractional T1/E1/J1 lines. Up to 248 (a full eight E1, T1, or J1 lines) HDLC/Transparent channels can be activated simultaneously.

## PPP

The Point-to-Point Protocol (PPP) provides a standard method to transport multi-protocol datagrams over point-to-point links. Interphase PPP implementation complies with the following RFCs:

- 1661 (Point-to Point Protocol)
- 1662 (PPP in HDLC-like Framing)
- 1618 (PPP over ISDN)
- 1570 (PPP LCP Extensions)
- 1333 (PPP Link Quality Monitoring)
- 1334 (PPP Authentication Protocols)
- 1717 (PPP Multilink Protocol).

The 4539 supports encapsulation of TCP/IP via RFC 1332 (PPP Internet Protocol Control Protocol) and of IPX via RFC 1552 (The PPP Internetwork Packet Exchange Control Protocol).

## X.25

X.25 protocol is used to connect Data Terminal Equipment (DTE) to Packet Switched Data Networks. The 4539 module can be equipped with software providing Layers 2 and 3 of X.25 in compliance with ISO8208, ISO7776, and ITU-T X.25. The Interphase X.25 implementation includes:

- Frame size up to 4096 bytes
- Up to 256 CVs
- IP and IPX over X.25 (RFC 1356)
- Mod 8 and mod 128 numbering

## Frame Relay

The 4539 module supports an embedded frame relay stack that is compliant with ITU-T Q.933 and ITU-T Q.922. The Interphase implementation includes:

- DLCI management (user defined, automatic)
- Frame size up to 4096 bytes
- Quality of Service management (CIR, Bc, Be, T)
- Congestion management (BECN, FECN, DE)
- User side of the User to Network interface
- Unicast only
- PVC only (up to 976 user's DLCI)
- IP and IPX over Frame Relay (RFC 1490)

## SNMP

Each protocol layer in the firmware maintains SNMP Management Information Bases (MIBs). The following MIBs are supported:

- DS1 MIB (RFC 1406)
- PPP MIB (RFC 1471, RFC 1473)
- FR MIB (RFC 1604)
- X.25 MIB ( RFC 1381, RFC 1382)
- ATM MIB (RFC 1695)
- Private enterprise MIB

# 4539 Software Development Support

The 4539 is available with three levels of software support:

- The first level is intended for software developers building their own embedded firmware on the 4539 processor, and their own 4539 drivers and APIs on the host CPU. To these customers, Interphase offers the Board Development Kit (BDK), an OS-independent hardware development tool.
- The second level of software support is targeted as well to customers developing their own embedded firmware for the 4539 controller, running under a standard Real Time Operating System (RTOS). To these customers, Interphase offers the Board Support Package (BSP). A 4539 BSP is specifically tailored for an RTOS.
- The third level of custom support is targeted for developers that intend to use the Interphase-embedded firmware protocol stacks under the APIs provided by Interphase. The tool is called an ***i***WARE Software Development Suite, and it provides a complete set of software solutions, including embedded firmware, drivers for different operating systems, and several software utilities and sample programs with sources. All these elements are provided in a single CD available through Interphase Professional Services.

## 4539 Board Development Kit

The 4539 Board Development Kit (BDK) includes an *Installation and Maintenance Manual*, a *Hardware Reference Manual*, and a *Built-In Self Test and Monitor Manual*. These documents provide installation instructions, hardware information, software implementation directives, as well as source examples. They describe the specification of the Interphase 4539 boot code provided in the FLASH memory. All the sources as well as the compilation environment for this boot code are also provided as an example for custom developments.

Two DOS® utilities are provided with the BDK. A setup utility permits modifying the content of the various programmable elements of the board, especially the FLASH EEPROM memory. Also included is an interactive utility that allows management of the card such as reset/run action, memory and registers dump, memory and DMA tests, and line parameters manipulation.

## 4539 VxWorks Board Support Package

The 4539 VxWorks Board Support Package consists of documentation compiled as a *Board Support Package Guide*. This document provides valuable information on how to configure and install VxWorks on the 4539. Once the BSP is installed, the 4539 can be connected to an Ethernet network and development can be done directly from VxWorks.

The 4539 Board Support Package (BSP) includes the files required to make VxWorks run on the 4539. The package provides source files for:

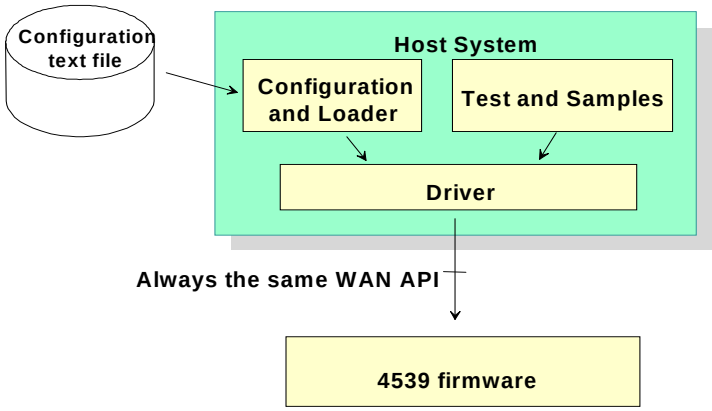
- TTY driver
- Ethernet driver (broadcast and multicast support)
- Interrupt controller
- Timestamp driver

- Auxiliary timer support
- Flash Memory Management
- True Flash File system (TFFS) support
- MMU support

## *i*WARE Software Development Suites

Interphase offers its customers a full suite of software utilities to provide driver software that uniquely fits the target application.

A typical custom ***i***WARE Software Development Suite available from Interphase Professional Services consists of software programs and utilities running on the host CPU, and embedded software ("firmware") which runs on the on-board networking processor. See the following block diagram:




**Typical *i*WARE Software Development Suite Block Diagram**

The software elements included in the Interphase ***i***WARE Software Development Suite are separated into four modules:

- The base drivers for each supported Operating System (executed by the host processor)
- The configuration and diagnostic utilities
- Sample programs
- The embedded firmware executed by the 8264A on the 4539 board

These modules interact with each other through well-defined and documented interfaces. A common WAN API is defined at the interface between the embedded firmware and the various drivers. The software modules provided are organized as shown in the block diagram shown above.

A complete documentation set is also provided with the Software Development Kit. The documentation describes the Interphase ***i***WARE WAN API (WAN Application Programmer's Interface with the embedded firmware), the Base Driver API, and sample programs and a tools users guides.

Interphase offers custom ***i***WARE Software Development Suites for Solaris®, VxWorks®, Chorus®, and LynxOS®, as well as several other operating systems.

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