
TIP111

Motion Controller with Absolute Encoder Interface (SSI)

Version 1.1

User Manual

Issue 1.4

September 2005

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TIP111-1x

1 axis motion controller with absolute encoder interface (SSI)

TIP111-2x

2 axes motion controller with absolute encoder interface (SSI)

TIP111-TM-10

Transition Module for TIP111-1x
Isolated 24V digital I/O

TIP111-TM-11

Transition Module for TIP111-1x
Isolated 24V digital I/O, encoder

TIP111-TM-12

Transition Module for TIP111-1x
Isolated 24V digital I/O, encoder, analog out

TIP111-TM-13

Transition Module for TIP111-1x
Isolated 24V digital I/O, encoder, analog in & out

TIP111-TM-20

Transition Module for TIP111-2x
Isolated 24V digital I/O

TIP111-TM-21

Transition Module for TIP111-2x
Isolated 24V digital I/O, encoder

TIP111-TM-22

Transition Module for TIP111-2x
Isolated 24V digital I/O, encoder, analog out

TIP111-TM-23

Transition Module for TIP111-2x
Isolated 24V digital I/O, encoder, analog in & out

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an 'Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W Write Only
R Read Only
R/W Read/Write
R/C Read/Clear
R/S Read/Set

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1.0	First Issue	June 1995
1.1	I/O Connector Input pol.	April 1996
1.2	General Revision	May 2003
1.3	Additional note for ADC conversion	October 2004
1.4	More detailed description of the various I/O signals	September 2005

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1 Product Description

The TIP111 family are IndustryPack® compatible modules for motion control applications using absolute encoder with a serial interface (SSI) as position feedback.

There are two versions available: The TIP111-1x provides a one axis controller and the TIP111-2x provides a two axes controller on a single size IP. The transition module TIP111-TM-xx is required for the signal conditioning and optional galvanically isolation of the various input and output signals.

The position feedback is provided by an absolute encoder with a synchronous serial interface (SSI) and a corresponding 32 bit shift register at the IP. The level of the encoder signals can be TTL or RS422. Optionally the encoder signals can be isolated on the transition module by high speed optocoupler. The TIP111 can handle data streams encoded in Binary or in Gray Code.

Two isolated 24V DC digital inputs have limit switch functionality. Each of these inputs drives a floating optocoupler output as hardware feedback. These outputs can be used to disable the power on the motor power amplifier, dependent on the actual direction. Two additional isolated 24V digital inputs are for free use by the software, for example as emergency stop input. A floating optical output can be controlled by software, for example as enable signal for the motor power amplifier.

A 16 bit digital to analog converter (DAC) produces a +/-10V controller output signal which can be used as speed or torque source for the power amplifier of the motor drive system. A galvanically isolation of this signal is available as a transition module option. A 12 bit analog to digital converter (ADC) with a configurable input voltage range is also available.

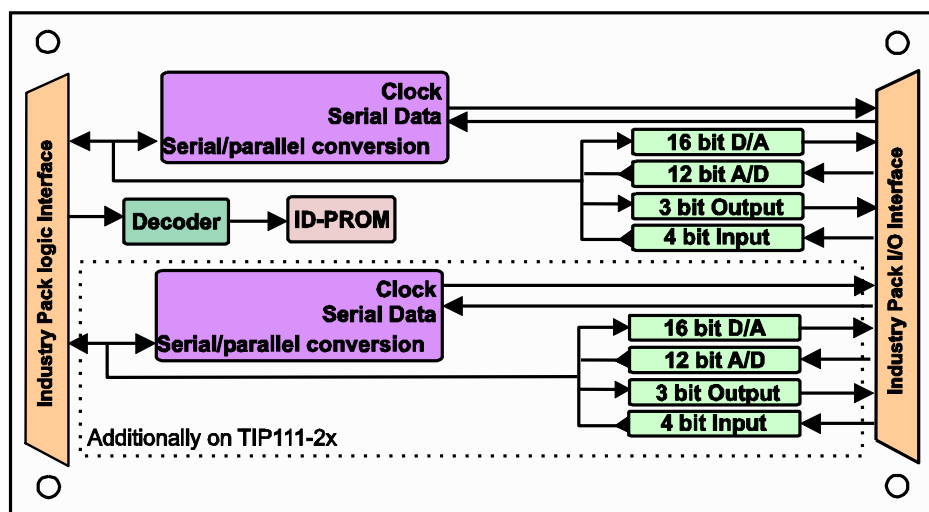


Figure 1-1 : Block Diagram TIP111-xx

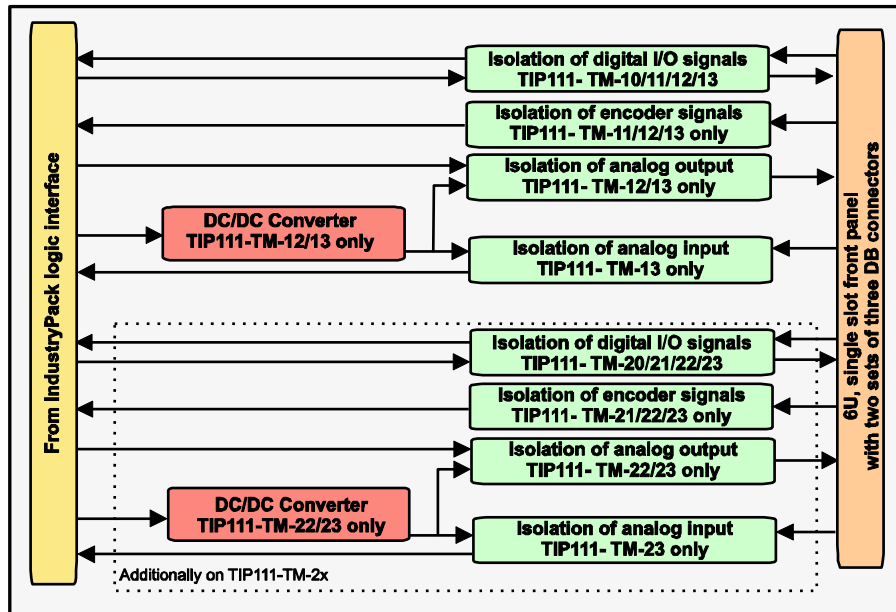


Figure 1-2 : Block Diagram TIP111-TM-xx

2 Technical Specification

2.1 IP Module TIP111-xx

IP Interface	
Interface	Single Size IndustryPack® Logic Interface (8 MHz) compliant to ANSI/VITA 4-1995
Wait States	IDPROM: no wait states All registers except accesses to ADC and DAC: no wait states Accesses to ADC: 1 wait state Accesses to DAC: 2 wait states
I/O Interface	
Transition Module	TIP111-TM-xx required, provides signal conditioning and optional isolation of digital and analog I/O signals
Number of Axes	TIP111-1x: 1 TIP111-2x: 2
Encoder Interface	Absolute encoder with a synchronous serial interface (SSI) 32 bit shift register, binary or gray programmable number of data bits, programmable from 1 to 32 clock rate, programmable 1µs to 15µs in steps of 1µs.
Analog Input	1 ADC per axis, 12 bit, 10µs, input voltage +/-10V
Analog Input Overvoltage	Input overvoltage protection up to 25Vpp
Analog Output	1 DAC per axis, output voltage +/-10V
Analog Output Current	+/-5mA
Digital Inputs	5 inputs per axis (TTL level)
Digital Outputs	2 outputs per axis (TTL level)
External Trigger I/O	TTL input, TTL output
Physical Data	
Power Requirements	50mA typical @ +5V DC
Temperature Range	Operating 0 °C to +70 °C Storage -45°C to +125°C
MTBF	TIP111-1x: 1126126 h TIP111-2x: 932836 h
Humidity	5 – 95 % non-condensing

Figure 2-1 : Technical Specification TIP111-xx

2.2 Transition Module TIP111-TM-xx

Board Data	
Board Size	1 VME slot (6 U)
Number of Axes	1 axis for TIP111-1x 2 axes for TIP111-2x
Encoder Interface	Signal level TTL or RS422 optional galvanically isolated
Analog Input	1 input per axis, input voltage +/-10V optional isolated (ADC device is located on TIP111)
Analog Input Overvoltage	Input overvoltage protection up to 100Vpp with galvanic isolation and up to 12Vpp without galvanic isolation
Analog Output	1 output per axis, output voltage +/-10V optional isolated (DAC device is located on TIP111)
Analog Output Current	+/-5mA maximum
Digital Inputs per Axis (isolated)	General purpose input 24V DC Reference switch input 24V DC Limit switch 1 control input 24V DC Limit switch 2 control input 24V DC Encoder error input TTL (low active)
Digital Outputs per Axis (isolated)	Enable output 24V DC (+ "in position" LED indication)
Digital Outputs directly driven from Inputs per Axis (isolated)	Limit_Switch_1 Output 24V DC Limit_Switch_2 Output 24V DC
External Trigger I/O per Axis	1 isolated TTL I/O per axis (jumper selectable input or output)
24V Output Load	1000 ohm maximum
Physical Data	
Power Requirements	TIP111-TM-1x : 100mA typical @ +5V DC (without load), <60mA typical @ ±12V DC (without load) TIP111-TM-2x : 180mA typical @ +5V DC (without load), <90mA typical @ ±12V DC (without load)
Temperature Range	Operating 0 °C to +70 °C Storage -45°C to +125°C
MTBF	TIP111-TM-10: 622277 h, TIP111-TM-11: 613120 h TIP111-TM-12: 540832 h, TIP111-TM-13: 511508 h TIP111-TM-20: 920810 h, TIP111-TM-21: 386996 h TIP111-TM-22: 331125 h, TIP111-TM-23: 309023 h
Humidity	5 – 95 % non-condensing

Figure 2-2 : Technical Specification TIP111-TM-xx

3 ID PROM

Offset	Function	Content
0x01	ASCII 'I'	0x49
0x03	ASCII 'P'	0x50
0x05	ASCII 'A'	0x41
0x07	ASCII 'C'	0x43
0x09	Manufacturer ID	0xB3
0x0B	Model Number	0x0C (TIP111-1x) 0x0F (TIP111-2x)
0x0D	Revision	0x11
0x0F	Reserved	0x00
0x11	Driver-ID Low - Byte	0x00
0x13	Driver-ID High - Byte	0x00
0x15	Number of bytes used	0x0C
0x17	CRC	0xBB (TIP111-1x) 0x39 (TIP111-2x)

Figure 3-1 : ID PROM

4 IP Addressing

4.1 I/O Addressing

The complete register set of the TIP111 is accessible in the IP I/O space.

Offset	Symbol	Description	Size (Bit)
0x01	INPSR1	Input and Status Register	8
0x03	OUTCR1	Output Control Register	8
0x05	BITCCR1	Bit Count Control Register	8
0x07	CLKCR1	Clock Control Register	8
0x09	DATBY0_1	Encoder Data Byte 0	8
0x0B	DATBY1_1	Encoder Data Byte 1	8
0x0D	DATBY2_1	Encoder Data Byte 2	8
0x0F	DATBY3_1	Encoder Data Byte 3	8
0x10	DACDA1	DAC Data Register	16
0x13	ADCCS1	ADC Control and Status Register	8
0x14	ADCDA1	ADC Data Register	16
0x17	ENAIN1	Interrupt Enable Register	8
0x19	INTVEC	Interrupt Vector Register	8

Figure 4-1 : Register Set TIP111-1x

On the TIP111-2x two axes motion controller the second axis is accessed through a second set of control and status registers. The INTVEC (Interrupt Vector Register) is shared between both axes.

Offset	Symbol	Description	Size (Bit)
0x21	INPSR2	Input and Status Register	8
0x23	OUTCR2	Output Control Register	8
0x25	BITCCR2	Bit Count Control Register	8
0x27	CLKCR2	Clock Control Register	8
0x29	DATBY0_2	Encoder Data Byte 0	8
0x2B	DATBY1_2	Encoder Data Byte 1	8
0x2D	DATBY2_2	Encoder Data Byte 2	8
0x2F	DATBY3_2	Encoder Data Byte 3	8
0x30	DACDA2	DAC Data Register	16
0x33	ADCCS2	ADC Control and Status Register	8
0x34	ADCDA2	ADC Data Register	16
0x37	ENAIN2	Interrupt Enable Register	8

Figure 4-2 : Additional Register Set TIP111-2x

4.2 Input and Status Register (INPSR)

The Input and Status Register (INPSR1 / INPSR2) provides the actual status of all digital input lines and the status of the internal control logic.

Bit	Symbol	Description	Access
7		Not used	
6	Data valid	Data Valid Indicates that the data transfer between the encoder is completed and the position data can be read. This bit is '0' during data transmission.	R
5	Parity Error	Parity Error 1 = parity error 0 = no parity error Bit is updated only if bit 4 in the CLKCR (Encoder with Parity) is set. Otherwise this bit is always read as '0'.	R
4	General Input	General Purpose Input 1 = input is active 0 = input is not active This status bit corresponds to the General_Purpose input (Pin 5) on the X102/202 connector of the TIP111-TM transition module.	R
3	Trigger Input	External Trigger Input 1 = trigger input is active 0 = trigger input is not active This bit reflects the state of the external Trigger output switch (Pins 6 & 14) on the X102/202 connector of the TIP111-TM transition module. The bidirectional Trigger I/O signal must be configured as input when this bit is going to be used. The transition module TIP111-TM-xx has one set of isolated trigger I/O signals, which are jumper configurable as trigger input or trigger output (see chapter "Trigger I/O Jumper Configuration").	R
2	Reference Input	Reference Input (could also be used as another general purpose input) 1 = input is active 0 = input is not active This status bit corresponds to the Reference input (Pin 12) on the X102/202 connector of the TIP111-TM transition module.	R
1	High Limit Input	High Limit Switch Control Input 1 = switch is activated 0 = switch is not activated This status bit corresponds to the Limit_Switch_2_Control input (Pin 4) on the X102/202 connector of the TIP111-TM transition module.	R

Bit	Symbol	Description	Access
0	Low Limit Input	Low Limit Switch Control Input 1 = switch is activated 0 = switch is not activated This status bit corresponds to the Limit_Switch_1_Control input (Pin 11) on the X102/202 connector of the TIP111-TM transition module.	R

Figure 4-3 : Input and Status Register (INPSR)

4.3 Output Control Register (OUTCR)

The Output Control Register (OUTCR1 / OUTCR2) controls the status of some output signals. Bits 0:2 can be read and written by software and are automatically cleared with the IP_RESET# signal.

Bit	Symbol	Description	Access
7:3		Not used	
2	Trigger Output	External Trigger Output 1 = trigger output switch activated 0 = trigger output switch not activated This bit controls the state of the external Trigger output switch (Pins 6 & 14) on the X102/202 connector of the TIP111-TM transition module. The Trigger output switch is a floating optocoupler output. The bidirectional Trigger I/O signal must be configured as output when this bit is going to be used. The transition module TIP111-TM-xx provides one isolated trigger I/O signal per axis, jumper configurable as input or output (see also chapter "Jumper Configuration").	R/W
1	Status LED	Status LED 1 = status LED on 0 = status LED off This bit controls the state of a LED located on the transition module.	R/W
0	Ampl. Enable	Servo Amplifier Enable Output 1 = enable output switch activated 0 = enable output switch not activated This bit controls the state of the Enable output switch (Pins 3 & 8) on the X103/203 connector of the TIP111-TM transition module. The Enable output switch is a floating optocoupler output which is normally connected to the enable input of the servo amplifier of the drive system.	R/W

Figure 4-4 : Output Control Register (OUTCR)

4.4 Bit Count Control Register (BITCCR)

The Bit Count Control Register (BITCCR1 / BITCCR2) is used to program the number of data bits of the serial absolute encoder. It can be read and written by software.

Bit	Symbol	Description	Access
7:6		Not used	
5	BC5	Number of absolute encoder data bits The data bit count can be programmed in the range from 1 to 32. Other programming values lead to wrong results.	R/W
4	BC4		
3	BC3		
2	BC2		
1	BC1		
0	BC0		

Figure 4-5 : Bit Count Control Register (BITCCR)

4.5 Clock Control Register (CLKCR)

The Clock Control Register (CLKCR1 / CLKCR2) is used to define the clock speed, parity, and data encoding of the SSI encoder. It can be read and written by software and are automatically cleared with the IP_RESET# signal.

Bit	Symbol	Description	Access
7		Not used	
6	Gray Code	Gray Code Control for data transmission 1 = Gray code 0 = Binary mode	R/W
5		Not used	
4	With Parity	Encoder with Parity Control 1 = encoder provides a parity bit to detect a parity error 0 = provides no parity bit	R/W
3	CR3	Clock Rate Bits used to program the encoder serial clock speed in steps of 1µs in the range of 1 to 15. A value of '0' is not allowed and will stop the operation of the SSI interface.	R/W
2	CR2		
1	CR1		
0	CR0		

Figure 4-6 : Clock Control Register (CLKCR)

4.6 Data Register (DATBYx)

The serial data of the encoder is shifted into four byte wide data register DATBY0_1, DATBY1_1, DATBY2_1, and DATBY3_1 (DATBY0_2, DATBY1_2, DATBY2_2, and DATBY3_2).

Register DATBY0 holds the least significant byte and DATBY3 the most significant byte of the 32 bit shift register.

The data transfer from the encoder is initiated by a write with any value to register DATBY0.

Bit	Symbol	Description	Access
7:0		8 bit Data Register	

Figure 4-7 : Data Register (DATBYx)

4.7 DAC Data Register (DACDA)

The DAC Data Register (DACDA1 / DACDA2) is the write only data register for the +/-10V controller output signal of the TIP111. The 2's complement value is converted to the corresponding output voltage with a range of +/-10V.

Bit	Symbol	Description	Access
15	S	16 bit DAC data in 2's complement	W
14:0		Only 16 bit access is supported for this register. A read to this register will return random data.	

Figure 4-8 : DAC Data Register (DACDA)

4.8 ADC Control and Status Register (ADCCS)

The ADC Control and Status Register (ADCCS1 / ADCCS2) controls the function of the 12 bit ADC.

A data conversion is started by a write cycle to the ADCCS (Write data value is don't care).

Bit	Symbol	Description	Access
7:1		These unused bits may be in a random state when reading this register.	
0	ADC Busy	ADC Busy 1 = ADC is busy	R/W*

Figure 4-9 : ADC Control and Status Register (ADCCS)

After power up the ADC is in a random state and requires two dummy conversions before operating correctly. This is based on the chip design of the ADC. All drivers from TEWS TECHNOLOGIES already include these two dummy conversions.

4.9 ADC Data Register (ADCDA)

The ADC Data Register (ADCDA1 / ADCDA2) holds the conversion result of the 12 bit ADC.

The 12 bit conversion data is left shifted by hardware so that the software reads a 16 bit 2's complement value.

Bit	Symbol	Description	Access
15	Sign	12 bit ADC Data in 2's complement, shifted to register bits 16:4. Bits 3:0 are always read as 0. Only 16 bit access is supported for this register.	R
14:4			
3:0			

Figure 4-10 : ADC Data Register (ADCDA)

4.10 Interrupt Enable Register (ENAINT)

Bit	Symbol	Description	Access
7	Int. Enable	Interrupt Enable Bit controls the interrupt enable for the external trigger input and can be read and written by software. 1 = enables interrupt 0 = disables interrupt Bit is also automatically cleared with the IP_RESET# signal.	R/W
6:0		These unused bits may be in a random state when reading this register.	

Figure 4-11 : Interrupt Enable Register (ENAINT)

4.11 Interrupt Vector Register (INTVEC)

The Interrupt Vector Register is a byte wide read/write register and is shared between both axes. Each axis will create an individual interrupt.

Bit	Symbol	Description	Access
7:1		Interrupt Vector loaded by software	R/W
0		Interrupt from Axes 1 or 2 1 = interrupt from axis 2 0 = interrupt from axis 1 Example: If this register loaded with 0x60, axis 1 will create an interrupt at vector 0x60 and axis 2 will create an interrupt at vector 0x61. Axis 1 is using the INTREQ0# and axis 2 is using INTREQ1# interrupt request line of the IP bus.	R/W

Figure 4-12 : Interrupt Vector Register (INTVEC)

5 Jumper Configurations

5.1 Transition Module TIP111-TM-xx

5.1.1 Trigger I/O Jumper Configuration

The trigger I/O signals at connector X102 (X202) of the transition module must be configured as input or output by the jumper J1 (J200) on the TIP111-TM transition module.

J1 selects the trigger signal direction for axis 1, J200 selects the trigger I/O direction for axis 2.



Figure 5-1 : Jumper J1 (J200) configuration for trigger input



Figure 5-2 : Jumper J1 (J200) configuration for trigger output

5.1.2 Jumper Layout TIP111-TM-xx

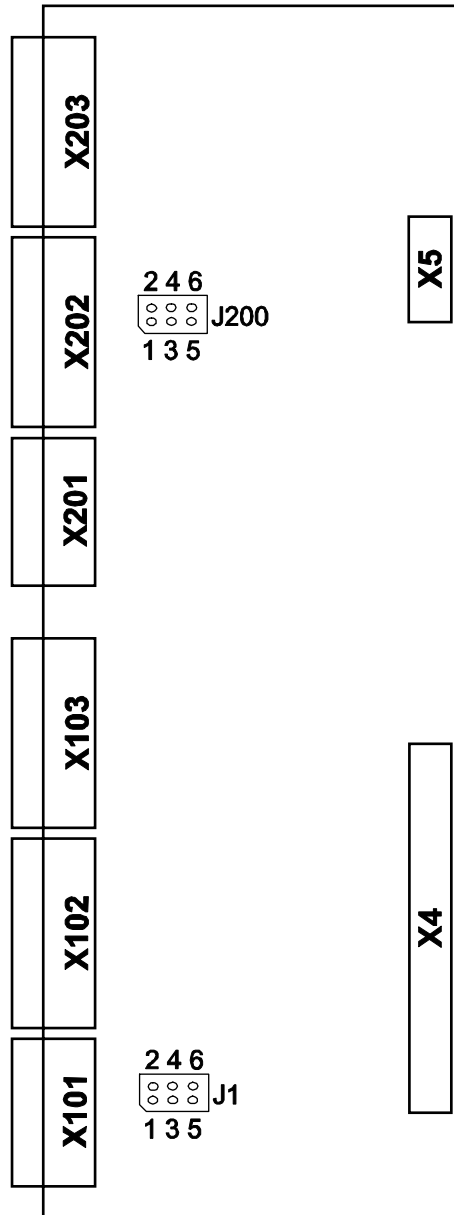


Figure 5-3 : Jumper Layout TIP111-TM-xx

6 Pin Assignment

6.1 I/O Connection of TIP111-xx

6.1.1 50 pin IP I/O Connector

Pin	Function	Pin	Function
1	+5V VCC	26	NC
2	+5V VCC	27	NC
3	GND	28	ENC SSI DATA axis 1 (TTL input)
4	GND	29	Status LED axis 2 (TTL output)
5	+12V	30	Servo Ampl. Enable axis 2 (TTL output)
6	-12V	31	GND
7	Status LED axis 1 (TTL output)	32	DAC output axis 2 (+/-10V)
8	Servo Ampl. Enable axis 1 (TTL output)	33	DAC ground axis 2
9	GND	34	ADC input axis 2 (+/-10V)
10	DAC output axis 1 (+/-10V)	35	ADC ground axis 2
11	DAC ground axis 1	36	GND
12	ADC input axis 1 (+/-10V)	37	Trigger_Input# axis 2 (TTL input)
13	ADC ground axis 1	38	Trigger_Output# axis 2 (TTL output)
14	GND	39	General_Input# axis 2 (TTL input)
15	Trigger_Input# axis 1 (TTL input)	40	Reference_Input# axis 2 (TTL input)
16	Trigger_Output# axis 1 (TTL output)	41	High_Limit_Switch# axis 2 (TTL input)
17	General_Input# axis 1 (TTL input)	42	Low_Limit_Switch# axis 2 (TTL input)
18	Reference_Input# axis 1 (TTL input)	43	NC
19	High_Limit_Switch# axis 1 (TTL input)	44	ENC SSI Clock axis 2 (TTL output)
20	Low_Limit_Switch# axis 1 (TTL input)	45	NC
21	NC	46	NC
22	ENC SSI Clock axis 1 (TTL output)	47	NC
23	NC	48	NC
24	NC	49	NC
25	NC	50	ENC SSI DATA axis 2 (TTL input)

Figure 6-1 : IP Module I/O Connector (TIP111-xx)

6.2 Transition Module I/O Connectors (TIP111-TM-xx)

6.2.1 X101/201 - DB9 Female - Servo Amplifier Signals

Pin	Function	Signal Level	Comment
1	Current_Limit_Switch_1+		Current Limit Switch 1 (floating optocoupler output transistor collector pin) See also pin 6. The switch state is controlled by the matching control input on X102/202 (Pin 11).
2	Current_Limit_Switch_2+		Current Limit Switch 2 (floating optocoupler output transistor collector pin) See also pin 7 The switch state is controlled by the matching control input on X102/202 (Pin 4).
3	Enable_Switch+		Enable Switch (floating optocoupler output transistor collector pin) See also pin 8. The switch state is controlled by OUTCR register bit 0.
4	Shield		
5	DAC_GND		Analog output ground reference See also pin 9.
6	Current_Limit_Switch_1-		Current Limit Switch 1 (floating optocoupler output transistor emitter pin) See also pin 1. The switch state is controlled by the matching control input on X102/202 (Pin 11).
7	Current_Limit_Switch_2-		Current Limit Switch 1 (floating optocoupler output transistor emitter pin) See also pin 2. The switch state is controlled by the matching control input on X102/202 (Pin 4).
8	Enable_Switch-		Enable Switch (floating optocoupler output transistor emitter pin) See also pin 3. The switch state is controlled by OUTCR register bit 0.
9	DAC_Output	+/-10V	Analog output See also pin 5.

Figure 6-2 : X101/201 - DB9 Female - Servo Amplifier Signals (TIP111-TM-xx)

6.2.2 X102/202 - DB15 Male - Power and I/O Signals

Pin	Function	Signal Level	Comment
1	ENC_VCC		Encoder power supply (source) Direct onboard connection to X103/203 pins 1 & 9. Connect to power supply.
2	ENC_VCC_SENSE		Encoder power supply sense (source) Direct onboard connection to X103/203 pin 3. Connect to power supply sense input (if applicable).
3	Shield		
4	Limit_Switch_2_Control Input	24V	24V control input to activate the Current_Limit_Switch_2 on X101/201. State readable in INPSR register bit 1.
5	General_Purpose Input	24V	General purpose 24V input State readable in INPSR register bit 4
6	Trigger I/O+	Input Configuration: TTL	Bidirectional Trigger I/O signal Direction is configured by jumper. See also pin 14. TTL Input configuration: Anode of photodiode. When configured as input, the status of this input is reflected by INSPR register bit 3. Output switch configuration: Floating optocoupler output transistor collector pin. When configured as output, this switch is controlled by OUTCR register bit 2.
7	Shield		
8	ADC_GND		Analog input ground reference See also pin 15.
9	ENC_GND		Encoder power supply ground (source) Direct onboard connection to X103/203 pins 2 & 10 Connect to power supply ground.
10	ENC_GND_SENSE		Encoder power supply sense ground (source) Direct onboard connection to X103/203 pin 11 Connect to power supply sense ground input (if applicable).
11	Limit_Switch_1_Control Input	24V	24V control input to activate the Current_Limit_Switch_1 on X101/201. State readable in INPSR register bit 0
12	Reference Input	24V	Reference 24V Input State readable in INPSR register bit 2

Pin	Function	Signal Level	Comment
13	Common Return of Input Signals	24V Common Return	Common Return Signal of the following 24V Inputs : General Purpose Input 1 (Pin 12) General Purpose Input 2 (Pin 5) Limit_Switch_1_Control_Input (Pin 11) Limit_Switch_2_Control_Input (Pin 4)
14	Trigger I/O–	Input Configuration: TTL	Bidirectional Trigger I/O signal Direction is configured by jumper. See also pin 6. TTL Input configuration: Anode of photodiode When configured as input, the status of this input is reflected by INSPR register bit 3. Output switch configuration : Floating optocoupler output transistor collector pin. When configured as output, this switch is controlled by OUTCR register bit 2.
15	ADC Input	+/-10V	Analog Input See also Pin 8

Figure 6-3 : X102/202 - DB15 Male - Power and I/O Signals (TIP111-TM-xx)

6.2.3 X103/203 - DB15 Female - Encoder Signals

Pin	Function	Signal Level	Comment
1	ENC_VCC		Encoder Power Supply Connect to Encoder
2	ENC_GND		Encoder Power Supply Ground Connect to Encoder
3	ENC_VCC_SENSE		Encoder Power Supply Sense Connect to Encoder (if applicable)
4	NC		
5	NC		
6	SSI_CLOCK#	TTL or RS422 -	SSI Encoder Clock Line (inverted) Connect to Encoder
7	SSI_DATA#	TTL or RS422 -	SSI Encoder Data Line (inverted) Connect to Encoder
8	Shield		
9	ENC_VCC	Same as pin1	Encoder Power Supply Connect to Encoder
10	ENC_GND	Same as pin 2	Encoder Power Supply Ground Connect to Encoder
11	ENC_GND_SENSE		Encoder Power Supply Sense Ground Connect to Encoder (if applicable)
12	NC		
13	NC		
14	SSI_CLOCK	TTL or RS422 +	SSI Encoder Clock Line Connect to Encoder
15	SSI_DATA	TTL or RS422 +	SSI Encoder Data Line Connect to Encoder

Figure 6-4 : X103/203 - DB15 Female - Encoder Signals (TIP111-TM-xx)