
TIP675

48 TTL I/O Lines with Interrupts

Version 1.0

User Manual

Issue 1.2

February 2003

TIP675-10

48 TTL I/O Lines with Interrupts

This document contains information, which is proprietary to TEWS TECHNOLOGIES GmbH. Any reproduction without written permission is forbidden.

TEWS TECHNOLOGIES GmbH has made any effort to ensure that this manual is accurate and complete. However TEWS TECHNOLOGIES GmbH reserves the right to change the product described in this document at any time without notice.

TEWS TECHNOLOGIES GmbH is not liable for any damage arising out of the application or use of the device described herein.

Style Conventions

Hexadecimal characters are specified with prefix 0x: i.e. 0x029E (hexadecimal value 029E).

Access terms are described as:

W Write Only

R Read Only

R/W Read/Write

R/C Read/Clear

R/S Read/Set

© 2002-2003 by TEWS TECHNOLOGIES GmbH

IndustryPack® is a registered trademark of SBS Technologies, Inc

Issue	Description	Date
1.0	First Issue	September 2002
1.1	Correction I/O Pin Assignment	January 2003
1.2	Completion of technical Information and new Hardware Revision	February 2003

Table of Contents

1	PRODUCT DESCRIPTION	5
2	TECHNICAL SPECIFICATION	6
3	ID PROM CONTENT	7
4	ADDRESS MAP	8
	4.1 IP Bus Address Map	8
	4.1.1 Word access to TIP675 registers	8
	4.1.2 Byte access to TIP675 registers.....	9
5	REGISTER DESCRIPTION	11
	5.1 Line Output Registers	11
	5.2 Line Input Registers	13
	5.3 Line Direction Registers	15
	5.4 Rising Edge Interrupt Status Registers	17
	5.5 Rising Edge Interrupt Enable Registers	19
	5.6 Falling Edge Interrupt Status Registers	21
	5.7 Falling Edge Interrupt Enable Registers	23
	5.8 Control Register	25
	5.8.1 Interrupt Vector Register	27
6	INSTALLATION TIP675	28
	6.1 Pull Up Resistors	28
	6.2 Pull Up Voltage	29
	6.3 TTL I/O Interface	30
7	I/O PIN ASSIGNMENT	31

Table of Figures

FIGURE 1-1 : BLOCK DIAGRAM	5
FIGURE 2-1 : TECHNICAL SPECIFICATION	6
FIGURE 3-1 : ID PROM CONTENT	7
FIGURE 4-1 : I/O SPACE REGISTER / WORD ACCESS.....	8
FIGURE 4-2 : I/O SPACE REGISTER / WORD ACCESS.....	9
FIGURE 5-1 : LINE OUTPUT REGISTER / WORD ACCESS (IP BASE ADDRESS + 0X00 / 0X02 / 0X04)	11
FIGURE 5-2 : LINE OUTPUT REGISTER PART 1 / BYTE ACCESS (IP BASE ADDRESS + 0X00 / 0X01 / 0X02).....	12
FIGURE 5-3 : LINE OUTPUT REGISTER PART 2 / BYTE ACCESS (IP BASE ADDRESS + 0X03 / 0X04 / 0X05).....	12
FIGURE 5-4 : LINE INPUT REGISTER / WORD ACCESS (IP BASE ADDRESS + 0X06 / 0X08 / 0X0A).....	13
FIGURE 5-5 : LINE INPUT REGISTER PART 1 / BYTE ACCESS (IP BASE ADDRESS + 0X06 / 0X07 / 0X08).....	14
FIGURE 5-6 : LINE INPUT REGISTER PART 2 / BYTE ACCESS (IP BASE ADDRESS + 0X09 / 0X0A / 0X0B).....	14
FIGURE 5-7 : LINE DIRECTION REGISTER / WORD ACCESS (IP BASE ADDRESS + 0X0C / 0X0E / 0X10)	15
FIGURE 5-8 : LINE DIRECTION REGISTER PART 1 / BYTE ACCESS (IP BASE ADDRESS + 0X0C / 0X0D / 0X0E)	16
FIGURE 5-9 : LINE DIRECTION REGISTER PART 2 / BYTE ACCESS (IP BASE ADDRESS + 0X0F / 0X10 / 0X11).....	16
FIGURE 5-10: RISING EDGE INTERRUPT STATUS REGISTER/WORD ACCESS (ADDR. +0X12/0X14/0X16)	17
FIGURE 5-11: RISING EDGE INTERRUPT STATUS REGISTER PART 1/BYTE ACCESS (ADDR. +0X12/0X13/0X14).....	18
FIGURE 5-12: RISING EDGE INTERRUPT STATUS REGISTER PART 2/BYTE ACCESS (ADDR. +0X15/0X16/0X17).....	18
FIGURE 5-13: RISING EDGE INTERRUPT ENABLE REGISTER/WORD ACCESS 8 (ADDR. +0X18/0X1A/0X1C)	19
FIGURE 5-14: RISING EDGE INTERRUPT ENABLE REGISTER PART 1/BYTE ACCESS (ADDR. +0X18/0X19/0X1A)	20
FIGURE 5-15: RISING EDGE INTERRUPT ENABLE REGISTER PART 2/BYTE ACCESS (ADDR. +0X1B/0X1C/0X1D) ...	20
FIGURE 5-16: FALLING EDGE INTERRUPT STATUS REGISTER/WORD ACCESS (ADDR. +0X1E/0X20/0X22)	21
FIGURE 5-17: FALLING EDGE INTERRUPT STATUS REGISTER PART 1/BYTE ACCESS (ADDR. +0X1E/0X1F/0X20) .	22
FIGURE 5-18: FALLING EDGE INTERRUPT STATUS REGISTER PART 2/BYTE ACCESS (ADDR. +0X21/0X22/0X23) ..	22
FIGURE 5-19: FALLING EDGE INTERRUPT ENABLE REGISTER/WORD ACCESS (ADDR. +0X24/0X26/0X28)	23
FIGURE 5-20: FALLING EDGE INTERRUPT ENABLE REGISTER PART 1/BYTE ACCESS (ADDR. +0X24/0X25/0X26) ..	24
FIGURE 5-21: FALLING EDGE INTERRUPT ENABLE REGISTER PART 2/BYTE ACCESS (ADDR. +0X27/0X28/0X29) ..	24
FIGURE 5-22 : CONTROL REGISTER (IP BASE ADDRESS + 0X2B).....	25
FIGURE 5-23 : MAXIMUM FREQUENCY OF EXTERNAL CLOCK	25
FIGURE 5-24 : INTERRUPT VECTOR REGISTER (IP BASE ADDRESS + 0X2D).....	27
FIGURE 6-1 : LOCATION OF PULL UP RESISTORS	28
FIGURE 6-2 : PINING OF PULL UP RESISTORS	29
FIGURE 6-3 : TTL I/O INTERFACE	30
FIGURE 7-1 : I/O PIN ASSIGNMENT	32

1 Product Description

The TIP675 is an IndustryPack® compatible module providing 48 digital TTL tri-state I/O lines with pull up resistors. Each of the 48 I/O lines is ESD protected and protected against overvoltage.

The line inputs are always enabled, allows determining the state of the I/O line at any time. This can be used as read back function for lines configured as outputs.

All 48 input lines can generate an interrupt. Each input interrupt can individually be enabled and cleared. Interrupts for negative and positive transitions could be used together with separate interrupt pending registers.

All interrupt inputs have an electronic debounce circuit to prevent short spikes on input lines to cause an IP interrupt.

Optional the I/O lines can be configured for simultaneous update internally and across several IP's by an external clock source. The polarity of the external clock source is programmable.

6 resistor networks mounted in sockets are used to pull the tri-state I/O lines to a logic high value. The resistor networks can be removed or changed in value.

After power-on or reset all I/O lines are configured as input and all pending interrupts are cleared.

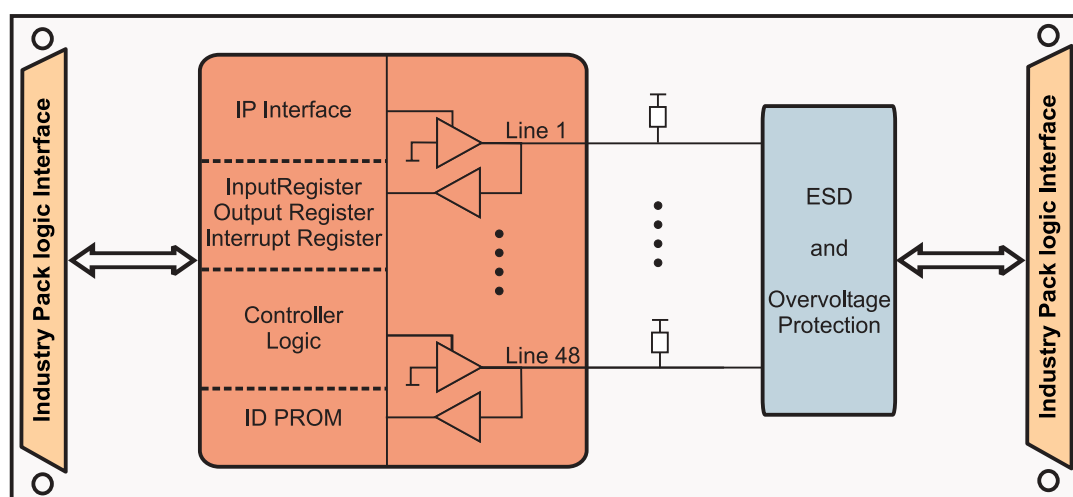


Figure 1-1 : Block Diagram

2 Technical Specification

IP Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995	
ID ROM Data	Format I	
I/O Space	Used with no wait states	
Memory Space	Not used	
DMA	Not supported	
Clock Rate	8 MHz	
Module Type	Type I	
Wait States	No wait states	
I/O Interface		
Number of TTL I/O Lines	48 lines	
Termination	4.7k ohms resistor network as pull up for each tri-state I/O line; Changeable and removable in groups of eight resistors	
Output 'Low' Current	-12mA maximum	
Output 'High' Current	Limited by 4k7 pull up to 1mA	
TTL Input / External Clock	Programmable simultaneous update feature by external clock	
External Clock Frequency	8MHz	
Interrupts	IP interrupt 0 for all 48 I/O lines; 4 registers for individual interrupt handling	
Interface Connector	50-conductor flat cable	
Physical Data		
Power Requirements	40mA typical @+5V DC all lines are inputs	
Temperature Range	Operating	-40 °C to +85 °C
	Storage	-65°C to +150°C
MTBF	191859 h	
Humidity	5 – 95 % non-condensing	

Figure 2-1 : Technical Specification

3 ID PROM Content

Address	Function	Content
0x01	ASCII 'I'	0x49
0x03	ASCII 'P'	0x50
0x05	ASCII 'A'	0x41
0x07	ASCII 'C'	0x43
0x09	Manufacturer ID	0xB3
0x0B	Model Number	0x36
0x0D	Revision	0x10
0x0F	Reserved	0x00
0x11	Driver-ID Low-Byte	0x00
0x13	Driver-ID High-Byte	0x00
0x15	Number of bytes used	0x0C
0x17	CRC	0xD8
0x19 to 0x3F	Reserved	0x00

Figure 3-1 : ID PROM Content

4 Address Map

4.1 IP Bus Address Map

The TIP675 is accessed in the I/O space through the following set of direct accessible registers.

All register of the TIP675 can be read/write by word (16bit) or byte (8bit) accesses.

4.1.1 Word access to TIP675 registers

Register Name	I/O lines	Register Symbol	Size	Address
Line Output Register	1 – 16	OUT_REG	16bit	0x00
	17 – 32		16bit	0x02
	33 – 48		16bit	0x04
Line Input Register	1 – 16	IN_REG	16bit	0x06
	17 – 32		16bit	0x08
	33 – 48		16bit	0x0A
Line Direction Register	1 – 16	DIR_REG	16bit	0x0C
	17 – 32		16bit	0x0E
	33 – 48		16bit	0x10
Interrupt Status Register for positive Transitions	1 – 16	IP_STA_REG	16bit	0x12
	17 – 32		16bit	0x14
	33 – 48		16bit	0x16
Interrupt Enable Register for positive Transitions	1 – 16	IP_ENA_REG	16bit	0x18
	17 – 32		16bit	0x1A
	33 – 48		16bit	0x1C
Interrupt Status Register for negative Transitions	1 – 16	IN_STA_REG	16bit	0x1E
	17 – 32		16bit	0x20
	33 – 48		16bit	0x22
Interrupt Enable Register for negative Transitions	1 – 16	IN_ENA_REG	16bit	0x24
	17 – 32		16bit	0x26
	33 – 48		16bit	0x28
Control Register		CNT_REG	16bit	0x2A
Interrupt Vector Register		VEC_REG	16bit	0x2C

Figure 4-1 : I/O Space Register / word access

4.1.2 Byte access to TIP675 registers

Register Name	I/O lines	Register Symbol	Size	Address
Line Output Register	9 – 16	OUT_REG	8bit	0x00
	1 – 8		8bit	0x01
	25 – 32		8bit	0x02
	17 – 24		8bit	0x03
	41 – 48		8bit	0x04
	33 – 40		8bit	0x05
Line Input Register	9 – 16	IN_REG	8bit	0x06
	1 – 8		8bit	0x07
	25 – 32		8bit	0x08
	17 – 24		8bit	0x09
	41 – 48		8bit	0x0A
	33 – 40		8bit	0x0B
Line Direction Register	9 – 16	DIR_REG	8bit	0x0C
	1 – 8		8bit	0x0D
	25 – 32		8bit	0x0E
	17 – 24		8bit	0x0F
	41 – 48		8bit	0x10
	33 – 40		8bit	0x11
Interrupt Status Register for positive Transitions	9 – 16	IP_STA_REG	8bit	0x12
	1 – 8		8bit	0x13
	25 – 32		8bit	0x14
	17 – 24		8bit	0x15
	41 – 48		8bit	0x16
	33 – 40		8bit	0x17
Interrupt Enable Register for positive Transitions	9 – 16	IP_ENA_REG	8bit	0x18
	1 – 8		8bit	0x19
	25 – 32		8bit	0x1A
	17 – 24		8bit	0x1B
	41 – 48		8bit	0x1C
	33 – 40		8bit	0x1D
Interrupt Status Register for negative Transitions	9 – 16	IN_STA_REG	8bit	0x1E
	1 – 8		8bit	0x1F
	25 – 32		8bit	0x20
	17 – 24		8bit	0x21
	41 – 48		8bit	0x22
	33 – 40		8bit	0x23
Interrupt Enable Register for negative Transitions	9 – 16	IN_ENA_REG	8bit	0x24
	1 – 8		8bit	0x25
	25 – 32		8bit	0x26
	17 – 24		8bit	0x27
	41 – 48		8bit	0x28
	33 – 40		8bit	0x29
Control Register		CNT_REG	8bit	0x2B
Interrupt Vector Register		VEC_REG	8bit	0x2D

Figure 4-2 : I/O Space Register / word access

To process all 24 bit of one register, at least two 16 bit or three 8 bit accesses are necessary.

All registers are cleared and set each bit to default value after IP reset. All bits of Line Output Register are set to '1'. All other registers set to '0'.

5 Register Description

5.1 Line Output Registers

The Line Output Register is subdivided into three word wide read/write registers. The status of the digital output channels can be set or reset directly by writing to the Line Output Register.

Bit Number	0x00	0x02	0x04	Access	Description
15 (MSB)	OUTPUT 16	OUTPUT 32	OUTPUT 48	R/W	To set an output channel active that means set to tri-state level, write '1' to the corresponding bit. For the inactive state write '0' to the corresponding bit. 0 : inactive 1 : active / tri-state
14	OUTPUT 15	OUTPUT 31	OUTPUT 47		
13	OUTPUT 14	OUTPUT 30	OUTPUT 46		
12	OUTPUT 13	OUTPUT 29	OUTPUT 45		
11	OUTPUT 12	OUTPUT 28	OUTPUT 44		
10	OUTPUT 11	OUTPUT 27	OUTPUT 43		
9	OUTPUT 10	OUTPUT 26	OUTPUT 42		
8	OUTPUT 9	OUTPUT 25	OUTPUT 41		
7	OUTPUT 8	OUTPUT 24	OUTPUT 40		
6	OUTPUT 7	OUTPUT 23	OUTPUT 39		
5	OUTPUT 6	OUTPUT 22	OUTPUT 38		
4	OUTPUT 5	OUTPUT 21	OUTPUT 37		
3	OUTPUT 4	OUTPUT 20	OUTPUT 36		
2	OUTPUT 3	OUTPUT 19	OUTPUT 35		
1	OUTPUT 2	OUTPUT 18	OUTPUT 34		
0 (LSB)	OUTPUT 1	OUTPUT 17	OUTPUT 33		

Figure 5-1 : Line Output Register / word access (IP Base Address + 0x00 / 0x02 / 0x04)

After power-on and reset all bits of Line Output Register are set to active / tri-state value.

Bit Number	0x00	0x01	0x02	Access	Description
7 (MSB)	OUTPUT 16	OUTPUT 8	OUTPUT 32	R/W	To set an output channel active that means set to tri-state level, write '1' to the corresponding bit. For the inactive state write '0' to the corresponding bit. 0 : inactive 1 : active / tri-state
6	OUTPUT 15	OUTPUT 7	OUTPUT 31		
5	OUTPUT 14	OUTPUT 6	OUTPUT 30		
4	OUTPUT 13	OUTPUT 5	OUTPUT 29		
3	OUTPUT 12	OUTPUT 4	OUTPUT 28		
2	OUTPUT 11	OUTPUT 3	OUTPUT 27		
1	OUTPUT 10	OUTPUT 2	OUTPUT 26		
0 (LSB)	OUTPUT 9	OUTPUT 1	OUTPUT 25		

Figure 5-2 : Line Output Register Part 1 / byte access (IP Base Address + 0x00 / 0x01 / 0x02)

Bit Number	0x03	0x04	0x05	Access	Description
7 (MSB)	OUTPUT 24	OUTPUT 48	OUTPUT 40	R/W	To set an output channel active that means set to tri-state level, write '1' to the corresponding bit. For the inactive state write '0' to the corresponding bit. 0 : inactive 1 : active / tri-state
6	OUTPUT 23	OUTPUT 47	OUTPUT 39		
5	OUTPUT 22	OUTPUT 46	OUTPUT 38		
4	OUTPUT 21	OUTPUT 45	OUTPUT 37		
3	OUTPUT 20	OUTPUT 44	OUTPUT 36		
2	OUTPUT 19	OUTPUT 43	OUTPUT 35		
1	OUTPUT 18	OUTPUT 42	OUTPUT 34		
0 (LSB)	OUTPUT 17	OUTPUT 41	OUTPUT 33		

Figure 5-3 : Line Output Register Part 2 / byte access (IP Base Address + 0x03 / 0x04 / 0x05)

Normally the output line is loaded with Line Output Register value direct after IP write access. This process is controlled by 8MHz IP clock.

With the simultaneous update feature the user is able to control the output switch moment by external clock. For more information please refer to chapter "Control Register".

To set a TTL line as output, the corresponding bit in the Line Direction Register must be set to '1'.

5.2 Line Input Registers

The Line Input Register is subdivided into three word wide read only registers that reflects the actual state of all 48 digital TTL I/O lines.

Bit Number	0x06	0x08	0x0A	Access	Description
15 (MSB)	INPUT 16	INPUT 32	INPUT 48	R	0 : TTL I/O line logic low 1 : TTL I/O line logic high
14	INPUT 15	INPUT 31	INPUT 47		
13	INPUT 14	INPUT 30	INPUT 46		
12	INPUT 13	INPUT 29	INPUT 45		
11	INPUT 12	INPUT 28	INPUT 44		
10	INPUT 11	INPUT 27	INPUT 43		
9	INPUT 10	INPUT 26	INPUT 42		
8	INPUT 9	INPUT 25	INPUT 41		
7	INPUT 8	INPUT 24	INPUT 40		
6	INPUT 7	INPUT 23	INPUT 39		
5	INPUT 6	INPUT 22	INPUT 38		
4	INPUT 5	INPUT 21	INPUT 37		
3	INPUT 4	INPUT 20	INPUT 36		
2	INPUT 3	INPUT 19	INPUT 35		
1	INPUT 2	INPUT 18	INPUT 34		
0 (LSB)	INPUT 1	INPUT 17	INPUT 33		

Figure 5-4 : Line Input Register / word access (IP Base Address + 0x06 / 0x08 / 0x0A)

Bit Number	0x06	0x07	0x08	Access	Description
7 (MSB)	INPUT 16	INPUT 8	INPUT 32	R	0 : TTL I/O line logic low 1 : TTL I/O line logic high
6	INPUT 15	INPUT 7	INPUT 31		
5	INPUT 14	INPUT 6	INPUT 30		
4	INPUT 13	INPUT 5	INPUT 29		
3	INPUT 12	INPUT 4	INPUT 28		
2	INPUT 11	INPUT 3	INPUT 27		
1	INPUT 10	INPUT 2	INPUT 26		
0 (LSB)	INPUT 9	INPUT 1	INPUT 25		

Figure 5-5 : Line Input Register Part 1 / byte access (IP Base Address + 0x06 / 0x07 / 0x08)

Bit Number	0x09	0x0A	0x0B	Access	Description
7 (MSB)	INPUT 24	INPUT 48	INPUT 40	R	0 : TTL I/O line logic low 1 : TTL I/O line logic high
6	INPUT 23	INPUT 47	INPUT 39		
5	INPUT 22	INPUT 46	INPUT 38		
4	INPUT 21	INPUT 45	INPUT 37		
3	INPUT 20	INPUT 44	INPUT 36		
2	INPUT 19	INPUT 43	INPUT 35		
1	INPUT 18	INPUT 42	INPUT 34		
0 (LSB)	INPUT 17	INPUT 41	INPUT 33		

Figure 5-6 : Line Input Register Part 2 / byte access (IP Base Address + 0x09 / 0x0A / 0x0B)

Normally the input lines are latched into Line Input Register every rising edge of the IP 8MHz clock.

With the simultaneous update feature the user is able to control this latch moment by external clock. After enable the external clock the Input Register contains undefined values. These values are undefined until next external clock edge latches the I/O lines. For more information please refer to chapter "Control Register".

5.3 Line Direction Registers

The Line Direction Register is subdivided into three word read/write registers. To enable the output lines the corresponding bit of the Line Direction Register must be set to logic level '1'. To disable the output lines and switch to an only input line the logic level '0' has to be written into the Line Direction Register.

Bit Number	0x0C	0x0E	0x10	Access	Description
15 (MSB)	DIR 16	DIR 32	DIR 48	R/W	0 : TTL I/O line as Input 1 : TTL I/O line as Output
14	DIR 15	DIR 31	DIR 47		
13	DIR 14	DIR 30	DIR 46		
12	DIR 13	DIR 29	DIR 45		
11	DIR 12	DIR 28	DIR 44		
10	DIR 11	DIR 27	DIR 43		
9	DIR 10	DIR 26	DIR 42		
8	DIR 9	DIR 25	DIR 41		
7	DIR 8	DIR 24	DIR 40		
6	DIR 7	DIR 23	DIR 39		
5	DIR 6	DIR 22	DIR 38		
4	DIR 5	DIR 21	DIR 37		
3	DIR 4	DIR 20	DIR 36		
2	DIR 3	DIR 19	DIR 35		
1	DIR 2	DIR 18	DIR 34		
0 (LSB)	DIR 1	DIR 17	DIR 33		

Figure 5-7 : Line Direction Register / word access (IP Base Address + 0x0C / 0x0E / 0x10)

Bit Number	0x0C	0x0D	0x0E	Access	Description
7 (MSB)	DIR 16	DIR 8	DIR 32	R/W	0 : TTL I/O line as Input 1 : TTL I/O line as Output
6	DIR 15	DIR 7	DIR 31		
5	DIR 14	DIR 6	DIR 30		
4	DIR 13	DIR 5	DIR 29		
3	DIR 12	DIR 4	DIR 28		
2	DIR 11	DIR 3	DIR 27		
1	DIR 10	DIR 2	DIR 26		
0 (LSB)	DIR 9	DIR 1	DIR 25		

Figure 5-8 : Line Direction Register Part 1 / byte access (IP Base Address + 0x0C / 0x0D / 0x0E)

Bit Number	0x0F	0x10	0x11	Access	Description
7 (MSB)	DIR 24	DIR 48	DIR 40	R/W	0 : TTL I/O line as Input 1 : TTL I/O line as Output
6	DIR 23	DIR 47	DIR 39		
5	DIR 22	DIR 46	DIR 38		
4	DIR 21	DIR 45	DIR 37		
3	DIR 20	DIR 44	DIR 36		
2	DIR 19	DIR 43	DIR 35		
1	DIR 18	DIR 42	DIR 34		
0 (LSB)	DIR 17	DIR 41	DIR 33		

Figure 5-9 : Line Direction Register Part 2 / byte access (IP Base Address + 0x0F / 0x10 / 0x11)

The reset value of the Line Direction Register is 0x0000 0000 0000. That means all TTL output lines are disabled.

5.4 Rising Edge Interrupt Status Registers

The Rising Edge Interrupt Status Register is subdivided into three word read/write registers and reflected in the corresponding bit a pending interrupt.

A pending interrupt request for a specific TTL I/O line is cleared by writing '1' to the according bit of the Rising Edge Interrupt Status Register.

Bit Number	0x12	0x14	0x16	Access	Description
15 (MSB)	IP_STA 16	IP_STA 32	IP_STA 48	R/W	Read access 0 : no interrupt request pending 1 : interrupt request pending Write access 1 : clear pending interrupt request
14	IP_STA 15	IP_STA 31	IP_STA 47		
13	IP_STA 14	IP_STA 30	IP_STA 46		
12	IP_STA 13	IP_STA 29	IP_STA 45		
11	IP_STA 12	IP_STA 28	IP_STA 44		
10	IP_STA 11	IP_STA 27	IP_STA 43		
9	IP_STA 10	IP_STA 26	IP_STA 42		
8	IP_STA 9	IP_STA 25	IP_STA 41		
7	IP_STA 8	IP_STA 24	IP_STA 40		
6	IP_STA 7	IP_STA 23	IP_STA 39		
5	IP_STA 6	IP_STA 22	IP_STA 38		
4	IP_STA 5	IP_STA 21	IP_STA 37		
3	IP_STA 4	IP_STA 20	IP_STA 36		
2	IP_STA 3	IP_STA 19	IP_STA 35		
1	IP_STA 2	IP_STA 18	IP_STA 34		
0 (LSB)	IP_STA 1	IP_STA 17	IP_STA 33		

Figure 5-10: Rising Edge Interrupt Status Register/word access (IP Base Address +0x12/0x14/0x16)

Bit Number	0x12	0x13	0x14	Access	Description
7 (MSB)	IP_STA 16	IP_STA 8	IP_STA 32	R/W	Read access 0 : no interrupt request pending 1 : interrupt request pending Write access 1 : clear pending interrupt request
6	IP_STA 15	IP_STA 7	IP_STA 31		
5	IP_STA 14	IP_STA 6	IP_STA 30		
4	IP_STA 13	IP_STA 5	IP_STA 29		
3	IP_STA 12	IP_STA 4	IP_STA 28		
2	IP_STA 11	IP_STA 3	IP_STA 27		
1	IP_STA 10	IP_STA 2	IP_STA 26		
0 (LSB)	IP_STA 9	IP_STA 1	IP_STA 25		

Figure 5-11: Rising Edge Interrupt Status Register Part 1/byte access (IP Base Address +0x12/0x13/0x14)

Bit Number	0x15	0x16	0x17	Access	Description
7 (MSB)	IP_STA 24	IP_STA 48	IP_STA 40	R/W	Read access 0 : no interrupt request pending 1 : interrupt request pending Write access 1 : clear pending interrupt request
6	IP_STA 23	IP_STA 47	IP_STA 39		
5	IP_STA 22	IP_STA 46	IP_STA 38		
4	IP_STA 21	IP_STA 45	IP_STA 37		
3	IP_STA 20	IP_STA 44	IP_STA 36		
2	IP_STA 19	IP_STA 43	IP_STA 35		
1	IP_STA 18	IP_STA 42	IP_STA 34		
0 (LSB)	IP_STA 17	IP_STA 41	IP_STA 33		

Figure 5-12: Rising Edge Interrupt Status Register Part 2/byte access (IP Base Address +0x15/0x16/0x17)

5.5 Rising Edge Interrupt Enable Registers

The Rising Edge Interrupt Enable Register is subdivided into three word read/write registers. To enable an interrupt for positive transitions on TTL input line the corresponding bit must be set to logic level '1'. To disable the interrupt source the corresponding bit must be set to logic level '0'.

Bit Number	0x18	0x1A	0x1C	Access	Description
15 (MSB)	IP_ENA 16	IP_ENA 32	IP_ENA 48	R/W	0 : Interrupt for I/O line disabled 1 : Interrupt for I/O line enabled
14	IP_ENA 15	IP_ENA 31	IP_ENA 47		
13	IP_ENA 14	IP_ENA 30	IP_ENA 46		
12	IP_ENA 13	IP_ENA 29	IP_ENA 45		
11	IP_ENA 12	IP_ENA 28	IP_ENA 44		
10	IP_ENA 11	IP_ENA 27	IP_ENA 43		
9	IP_ENA 10	IP_ENA 26	IP_ENA 42		
8	IP_ENA 9	IP_ENA 25	IP_ENA 41		
7	IP_ENA 8	IP_ENA 24	IP_ENA 40		
6	IP_ENA 7	IP_ENA 23	IP_ENA 39		
5	IP_ENA 6	IP_ENA 22	IP_ENA 38		
4	IP_ENA 5	IP_ENA 21	IP_ENA 37		
3	IP_ENA 4	IP_ENA 20	IP_ENA 36		
2	IP_ENA 3	IP_ENA 19	IP_ENA 35		
1	IP_ENA 2	IP_ENA 18	IP_ENA 34		
0 (LSB)	IP_ENA 1	IP_ENA 17	IP_ENA 33		

Figure 5-13: Rising Edge Interrupt Enable Register/word access 8 (IP Base Address +0x18/0x1A/0x1C)

Bit Number	0x18	0x19	0x1A	Access	Description
7 (MSB)	IP_ENA 16	IP_ENA 8	IP_ENA 32	R/W	0 : Interrupt for I/O line disabled 1 : Interrupt for I/O line enabled
6	IP_ENA 15	IP_ENA 7	IP_ENA 31		
5	IP_ENA 14	IP_ENA 6	IP_ENA 30		
4	IP_ENA 13	IP_ENA 5	IP_ENA 29		
3	IP_ENA 12	IP_ENA 4	IP_ENA 28		
2	IP_ENA 11	IP_ENA 3	IP_ENA 27		
1	IP_ENA 10	IP_ENA 2	IP_ENA 26		
0 (LSB)	IP_ENA 9	IP_ENA 1	IP_ENA 25		

Figure 5-14: Rising Edge Interrupt Enable Register Part 1/byte access (IP Base Address +0x18/0x19/0x1A)

Bit Number	0x1B	0x1C	0x1D	Access	Description
7 (MSB)	IP_ENA 24	IP_ENA 48	IP_ENA 40	R/W	0 : Interrupt for I/O line disabled 1 : Interrupt for I/O line enabled
6	IP_ENA 23	IP_ENA 47	IP_ENA 39		
5	IP_ENA 22	IP_ENA 46	IP_ENA 38		
4	IP_ENA 21	IP_ENA 45	IP_ENA 37		
3	IP_ENA 20	IP_ENA 44	IP_ENA 36		
2	IP_ENA 19	IP_ENA 43	IP_ENA 35		
1	IP_ENA 18	IP_ENA 42	IP_ENA 34		
0 (LSB)	IP_ENA 17	IP_ENA 41	IP_ENA 33		

Figure 5-15: Rising Edge Interrupt Enable Register Part 2/byte access (IP Base Address +0x1B/0x1C/0x1D)

If an interrupt for positive transitions on one TTL I/O line is enabled the TIP675 generates an IP interrupt after a rising edge occurs on this I/O line.

5.6 Falling Edge Interrupt Status Registers

The Falling Edge Interrupt Status Register is subdivided into three word read/write registers and reflected in the corresponding bit a pending interrupt.

A pending interrupt request for a specific TTL I/O line is cleared by writing '1' to the according bit of the Falling Edge Interrupt Status Register.

Bit Number	0x1E	0x20	0x22	Access	Description
15 (MSB)	IN_STA 16	IN_STA 32	IN_STA 48	R/W	Read access 0 : no interrupt request pending 1 : interrupt request pending Write access 1 : clear pending interrupt request
14	IN_STA 15	IN_STA 31	IN_STA 47		
13	IN_STA 14	IN_STA 30	IN_STA 46		
12	IN_STA 13	IN_STA 29	IN_STA 45		
11	IN_STA 12	IN_STA 28	IN_STA 44		
10	IN_STA 11	IN_STA 27	IN_STA 43		
9	IN_STA 10	IN_STA 26	IN_STA 42		
8	IN_STA 9	IN_STA 25	IN_STA 41		
7	IN_STA 8	IN_STA 24	IN_STA 40		
6	IN_STA 7	IN_STA 23	IN_STA 39		
5	IN_STA 6	IN_STA 22	IN_STA 38		
4	IN_STA 5	IN_STA 21	IN_STA 37		
3	IN_STA 4	IN_STA 20	IN_STA 36		
2	IN_STA 3	IN_STA 19	IN_STA 35		
1	IN_STA 2	IN_STA 18	IN_STA 34		
0 (LSB)	IN_STA 1	IN_STA 17	IN_STA 33		

Figure 5-16: Falling Edge Interrupt Status Register/word access (IP Base Address +0x1E/0x20/0x22)

Bit Number	0x1E	0x1F	0x20	Access	Description
7 (MSB)	IN_STA 16	IN_STA 8	IN_STA 32	R/W	Read access 0 : no interrupt request pending 1 : interrupt request pending Write access 1 : clear pending interrupt request
6	IN_STA 15	IN_STA 7	IN_STA 31		
5	IN_STA 14	IN_STA 6	IN_STA 30		
4	IN_STA 13	IN_STA 5	IN_STA 29		
3	IN_STA 12	IN_STA 4	IN_STA 28		
2	IN_STA 11	IN_STA 3	IN_STA 27		
1	IN_STA 10	IN_STA 2	IN_STA 26		
0 (LSB)	IN_STA 9	IN_STA 1	IN_STA 25		

Figure 5-17: Falling Edge Interrupt Status Register Part 1/byte access (IP Base Address +0x1E/0x1F/0x20)

Bit Number	0x21	0x22	0x23	Access	Description
7 (MSB)	IN_STA 24	IN_STA 48	IN_STA 40	R/W	Read access 0 : no interrupt request pending 1 : interrupt request pending Write access 1 : clear pending interrupt request
6	IN_STA 23	IN_STA 47	IN_STA 39		
5	IN_STA 22	IN_STA 46	IN_STA 38		
4	IN_STA 21	IN_STA 45	IN_STA 37		
3	IN_STA 20	IN_STA 44	IN_STA 36		
2	IN_STA 19	IN_STA 43	IN_STA 35		
1	IN_STA 18	IN_STA 42	IN_STA 34		
0 (LSB)	IN_STA 17	IN_STA 41	IN_STA 33		

Figure 5-18: Falling Edge Interrupt Status Register Part 2/byte access (IP Base Address +0x21/0x22/0x23)

5.7 Falling Edge Interrupt Enable Registers

The Falling Edge Interrupt Enable Register is subdivided into three word read/write registers. To enable an interrupt for negative transitions on TTL input line the corresponding bit must be set to logic level '1'. To disable the interrupt source the corresponding bit must be set to logic level '0'.

Bit Number	0x24	0x26	0x28	Access	Description
15 (MSB)	IN_ENA 16	IN_ENA 32	IN_ENA 48	R/W	0 : Interrupt for I/O line disabled 1 : Interrupt for I/O line enabled
14	IN_ENA 15	IN_ENA 31	IN_ENA 47		
13	IN_ENA 14	IN_ENA 30	IN_ENA 46		
12	IN_ENA 13	IN_ENA 29	IN_ENA 45		
11	IN_ENA 12	IN_ENA 28	IN_ENA 44		
10	IN_ENA 11	IN_ENA 27	IN_ENA 43		
9	IN_ENA 10	IN_ENA 26	IN_ENA 42		
8	IN_ENA 9	IN_ENA 25	IN_ENA 41		
7	IN_ENA 8	IN_ENA 24	IN_ENA 40		
6	IN_ENA 7	IN_ENA 23	IN_ENA 39		
5	IN_ENA 6	IN_ENA 22	IN_ENA 38		
4	IN_ENA 5	IN_ENA 21	IN_ENA 37		
3	IN_ENA 4	IN_ENA 20	IN_ENA 36		
2	IN_ENA 3	IN_ENA 19	IN_ENA 35		
1	IN_ENA 2	IN_ENA 18	IN_ENA 34		
0 (LSB)	IN_ENA 1	IN_ENA 17	IN_ENA 33		

Figure 5-19: Falling Edge Interrupt Enable Register/word access (IP Base Address +0x24/0x26/0x28)

Bit Number	0x24	0x25	0x26	Access	Description
7 (MSB)	IN_ENA 16	IN_ENA 8	IN_ENA 32	R/W	0 : Interrupt for I/O line disabled 1 : Interrupt for I/O line enabled
6	IN_ENA 15	IN_ENA 7	IN_ENA 31		
5	IN_ENA 14	IN_ENA 6	IN_ENA 30		
4	IN_ENA 13	IN_ENA 5	IN_ENA 29		
3	IN_ENA 12	IN_ENA 4	IN_ENA 28		
2	IN_ENA 11	IN_ENA 3	IN_ENA 27		
1	IN_ENA 10	IN_ENA 2	IN_ENA 26		
0 (LSB)	IN_ENA 9	IN_ENA 1	IN_ENA 25		

Figure 5-20: Falling Edge Interrupt Enable Register Part 1/byte access (IP Base Address +0x24/0x25/0x26)

Bit Number	0x27	0x28	0x29	Access	Description
7 (MSB)	IN_ENA 24	IN_ENA 48	IN_ENA 40	R/W	0 : Interrupt for I/O line disabled 1 : Interrupt for I/O line enabled
6	IN_ENA 23	IN_ENA 47	IN_ENA 39		
5	IN_ENA 22	IN_ENA 46	IN_ENA 38		
4	IN_ENA 21	IN_ENA 45	IN_ENA 37		
3	IN_ENA 20	IN_ENA 44	IN_ENA 36		
2	IN_ENA 19	IN_ENA 43	IN_ENA 35		
1	IN_ENA 18	IN_ENA 42	IN_ENA 34		
0 (LSB)	IN_ENA 17	IN_ENA 41	IN_ENA 33		

Figure 5-21: Falling Edge Interrupt Enable Register Part 2/byte access (IP Base Address +0x27/0x28/0x29)

If an interrupt for negative transitions on one TTL I/O line is enabled the TIP675 generates an IP interrupt after a falling edge occurs on this I/O line.

5.8 Control Register

The Control Register is a byte wide read/write register. The both used bits of the Control Register serve to enable and to switch the polarity of the external clock. I/O interface pin 49 is used as TTL compatible external clock input.

After enabling this external clock all 48 input latches and all 48 output drivers of the TIP675 change there state simultaneous on positive or negative edge of this external clock. Several TIP675 in the system could be synchronized in this way.

Bit Number	Bit Symbol	Access	Description
7 (MSB)	-		
6	-		
5	-		
4	-		
3	-		
2	-		
1	EX_CLK_POL	R/W	external clock polarity 0 : positive edge 1 : negative edge
0 (LSB)	EX_CLK_ENA	R/W	external clock enable 0 : disable 1 : enable

Figure 5-22 : Control Register (IP Base Address + 0x2B)

The maximum input frequency of the external clock is limited to 8MHz. The symmetry of this external clock does not require 50%, but the minimum pulse length is 10ns.

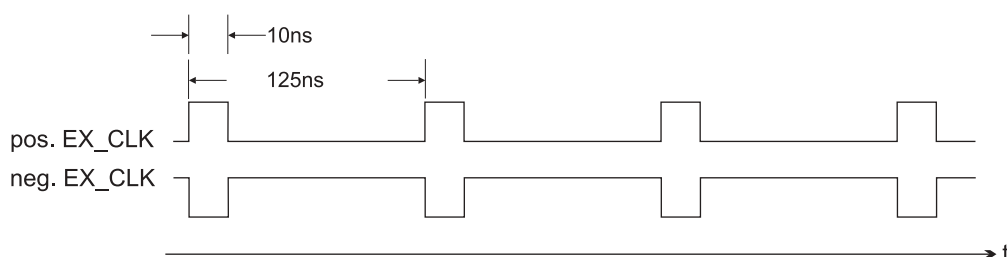


Figure 5-23 : Maximum Frequency of external Clock

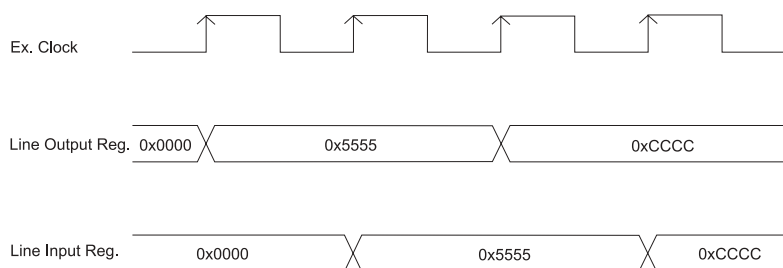
Info for using the External Clock

Input: After positive or negative external clock edge all input lines are latched and loaded into Line Input Register. Also input interrupts are generated with the external clock edge. This guarantees that the input transitions which are responsible for the interrupt are latched into the Line Input Register.

Output: The data of the Line Output Register are switched to the output port with positive or negative external clock edge.

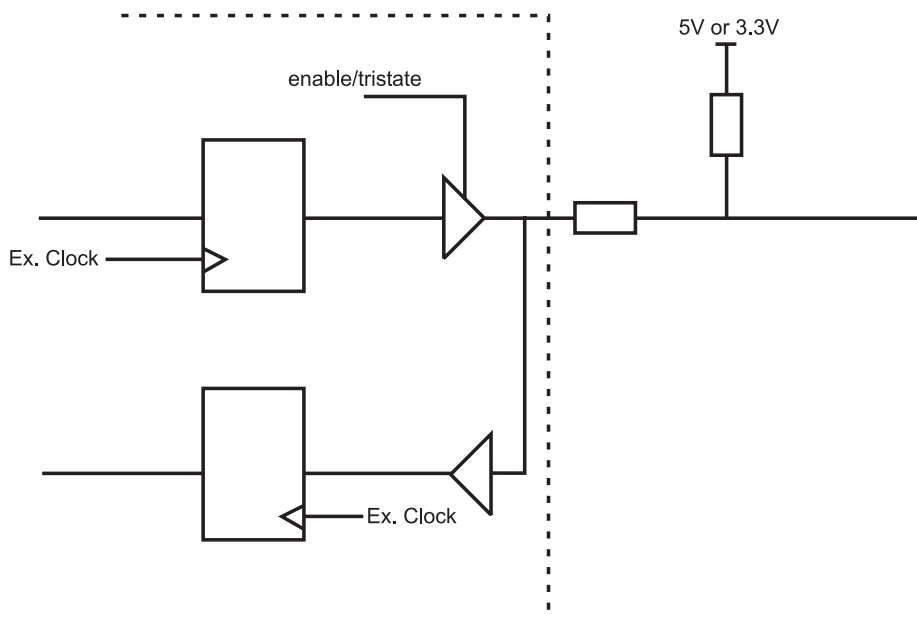
Input/Output: If the I/O lines are used as output port and the corresponding Line Input Register is read before a second external clock edge, both registers are different. Only after the second external clock edge both registers, Line Input and Line Output, are equal.

Example:



The reason for this is the internal switching time for the signals and the I/O circuit design of the TIP675. If the output register and the input register are triggered by the same external clock signal, both flip-flops load the value at the same time. The output signal needs some nanoseconds to reach the input of the input register. So the previous value at the input register is latched.

The following figure shows a simplified I/O block of the TIP675.



As well by using the internal 8MHz IP clock these internal switching times are present. But the time between two trigger impulses is short enough to load the actual value into the input registers before a new IP access could be released.

5.8.1 Interrupt Vector Register

The Interrupt Vector Register is a byte wide read/write register.

The value of the Interrupt Vector Register could be read/write during I/O cycle and also be read during an interrupt acknowledge cycle.

Bit Number	Bit Symbol	Access	Description
7 (MSB)	IVEC7	R/W	Used for IP interrupt acknowledge cycle
6	IVEC6		
5	IVEC5		
4	IVEC4		
3	IVEC3		
2	IVEC2		
1	IVEC1		
0 (LSB)	IVEC0		

Figure 5-24 : Interrupt Vector Register (IP Base Address + 0x2D)

All 48 digital I/O lines use the IP interrupt line 0 to signal a pending interrupt.

6 Installation TIP675

6.1 Pull Up Resistors

Six resistor networks (8 x 4.7k ohms) mounted in sockets are used to pull up the tri-state TTL I/O lines. The resistor networks can be removed or changed in value.

A resistor network is made out of eight individual resistors in one serial package.

Groups of resistors:

- N19 : I/O line 1 – 8
- N18 : I/O line 25 – 32
- N17 : I/O line 9 – 16
- N16 : I/O line 33 – 40
- N15 : I/O line 17 – 24
- N14 : I/O line 41 – 48

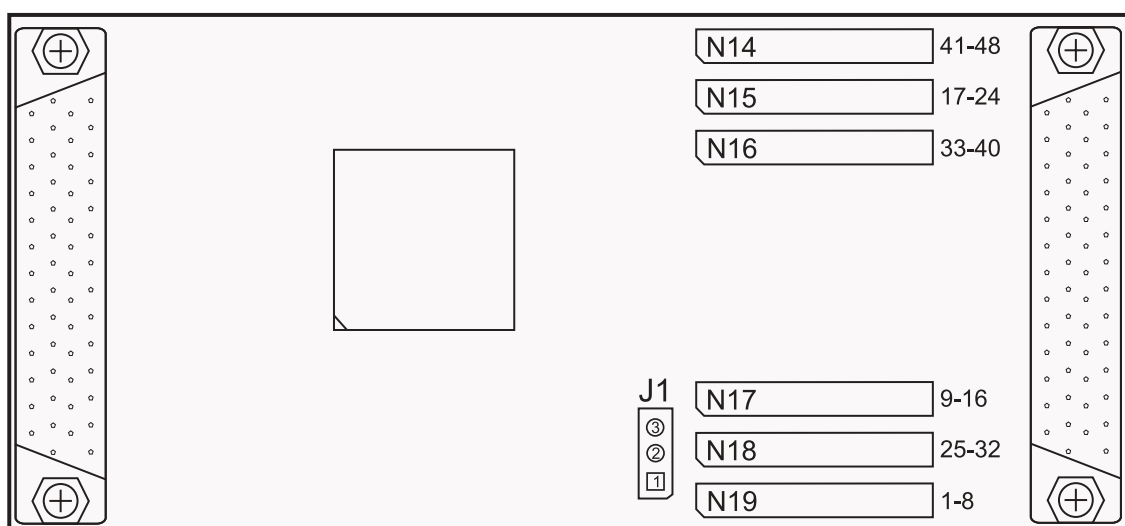


Figure 6-1 : Location of Pull Up Resistors

Resistor pinning:

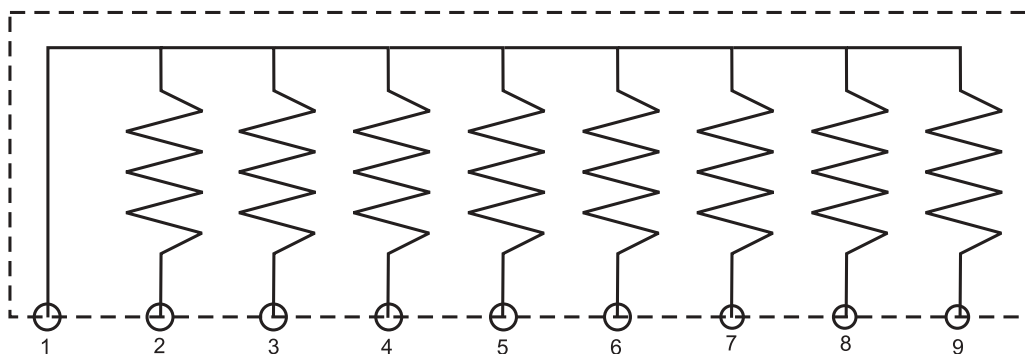


Figure 6-2 : Pining of Pull Up Resistors

6.2 Pull Up Voltage

To fit the maximum I/O output voltage to 5V or alternative 3.3V for designs with only 3.3V tolerant devices use the jumper J1. The default is 5V I/O voltage.

- | | |
|-----------|----------------------------------|
| Jumper J1 | 1 – 2 : I/O Voltage 3.3V |
| Jumper J1 | 2 – 3 : I/O Voltage 5V (default) |

6.3 TTL I/O Interface

The 48 TTL I/O lines are realized with an Input / Output register built in the XILINX FPGA and a few external passive devices. A serial resistor reduces spikes during switching process. The 4.7k ohms pull up for the tri-state output function and an electronic protection array for ESD and overvoltage protection.

See the following figure for more information of electrical circuitry.

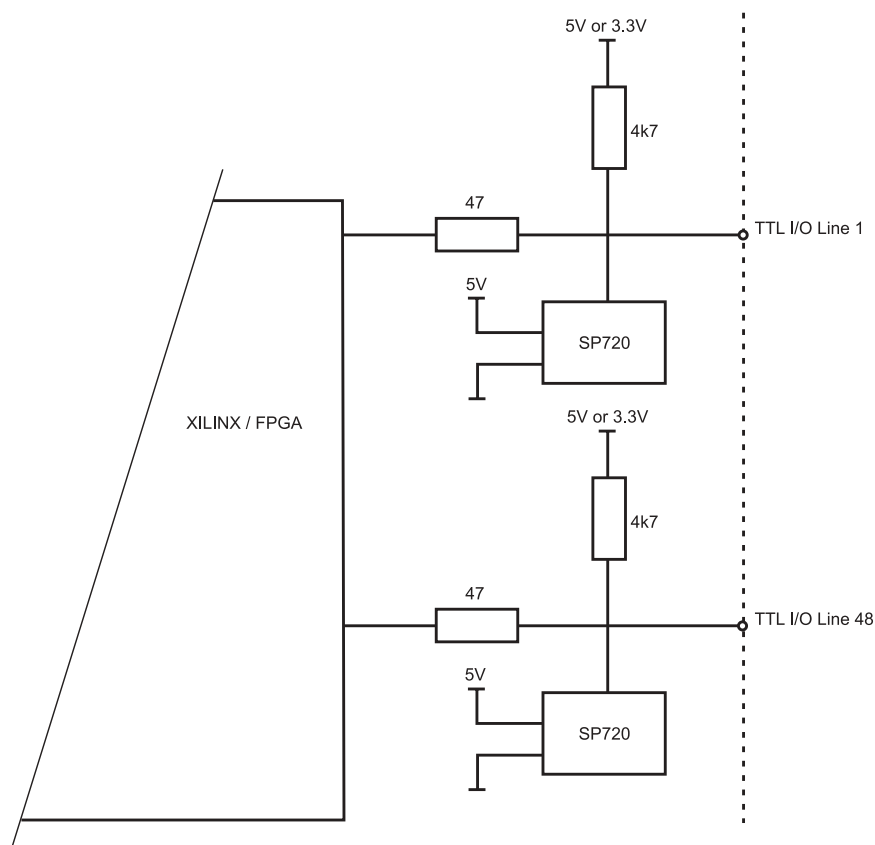


Figure 6-3 : TTL I/O Interface

Please note that the length and with it the large capacitance of flat cable connected to the TIP675 module should be kept very short to prevent large cross talk.

To reduce the cross talk already on the TIP675 all 48 I/O lines are switched not at the same time. The output lines are switched in 8 groups of 6 signals in steps of 15ns. So after about 120ns the switching process is completed.

7 I/O Pin Assignment

I/O Pin Number	Function	Signal Name
1	TTL I/O Line 1	I/O 1
2	TTL I/O Line 2	I/O 2
3	TTL I/O Line 3	I/O 3
4	TTL I/O Line 4	I/O 4
5	TTL I/O Line 5	I/O 5
6	TTL I/O Line 6	I/O 6
7	TTL I/O Line 7	I/O 7
8	TTL I/O Line 8	I/O 8
9	TTL I/O Line 9	I/O 9
10	TTL I/O Line 10	I/O 10
11	TTL I/O Line 11	I/O 11
12	TTL I/O Line 12	I/O 12
13	TTL I/O Line 13	I/O 13
14	TTL I/O Line 14	I/O 14
15	TTL I/O Line 15	I/O 15
16	TTL I/O Line 16	I/O 16
17	TTL I/O Line 17	I/O 17
18	TTL I/O Line 18	I/O 18
19	TTL I/O Line 19	I/O 19
20	TTL I/O Line 20	I/O 20
21	TTL I/O Line 21	I/O 21
22	TTL I/O Line 22	I/O 22
23	TTL I/O Line 23	I/O 23
24	TTL I/O Line 24	I/O 24
25	TTL I/O Line 25	I/O 25
26	TTL I/O Line 26	I/O 26
27	TTL I/O Line 27	I/O 27
28	TTL I/O Line 28	I/O 28
29	TTL I/O Line 29	I/O 29
30	TTL I/O Line 30	I/O 30
31	TTL I/O Line 31	I/O 31
32	TTL I/O Line 32	I/O 32
33	TTL I/O Line 33	I/O 33
34	TTL I/O Line 34	I/O 34
35	TTL I/O Line 35	I/O 35
36	TTL I/O Line 36	I/O 36

I/O Pin Number	Function	Signal Name
37	TTL I/O Line 37	I/O 37
38	TTL I/O Line 38	I/O 38
39	TTL I/O Line 39	I/O 39
40	TTL I/O Line 40	I/O 40
41	TTL I/O Line 41	I/O 41
42	TTL I/O Line 42	I/O 42
43	TTL I/O Line 43	I/O 43
44	TTL I/O Line 44	I/O 44
45	TTL I/O Line 45	I/O 45
46	TTL I/O Line 46	I/O 46
47	TTL I/O Line 47	I/O 47
48	TTL I/O Line 48	I/O 48
49	External Clock	EX_CLK
50	Signal Ground	GND

Figure 7-1 : I/O Pin Assignment