
TPMC866-12

8 Channel Serial Interface

RS422 / RS485 (FD / HD)

Version 1.1

User Manual

Issue 1.1.5

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TEWS TECHNOLOGIES GmbH

Am Bahnhof 7 25469 Halstenbek, Germany

Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19

e-mail: info@tews.com www.tews.com

TPMC866-12

8 channel serial interface PMC
RS422, RS485 (FD/HD) with front I/O and P14
I/O

TPMC866-12-ET

8 channel serial interface PMC
RS422, RS485 (FD/HD) with front I/O and P14
I/O, extended temperature range

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an 'Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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1 Product Description

The TPMC866-12 provides an 8 channel high performance serial interface. Each serial channel can be configured by a DIP switch to operate as an RS422, RS485-FD-M (Full Duplex Master), RS485-FD-S (Full Duplex Slave) or RS485-HD (Half Duplex) interface.

For RS422 and RS485-FD a four wire interface (RX+, RX-, TX+, TX-) plus ground (GND) is provided. For RS485-HD a two wire interface (DX+, DX-) plus ground (GND) is provided.

For front I/O a HD50 female connector is located in the front panel. For back I/O the P14 I/O connector is supported.

Each channel of the TPMC866-12 has a 128 byte transmit FIFO and a 128 byte receive FIFO to significantly reduce the overhead required to provide data to the transmitters and get data from the receivers. The FIFO trigger levels are programmable.

The baud rate is individually programmable up to 460.8Kbaud per channel.

For fast interrupt source detection the TPMC866-12 provides an Interrupt Status Register covering all interrupt sources.

I/O line transceivers are protected against electrostatic discharge (ESD).

The TPMC866-12 is available in extended temperature range as TPMC866-12-ET versions.

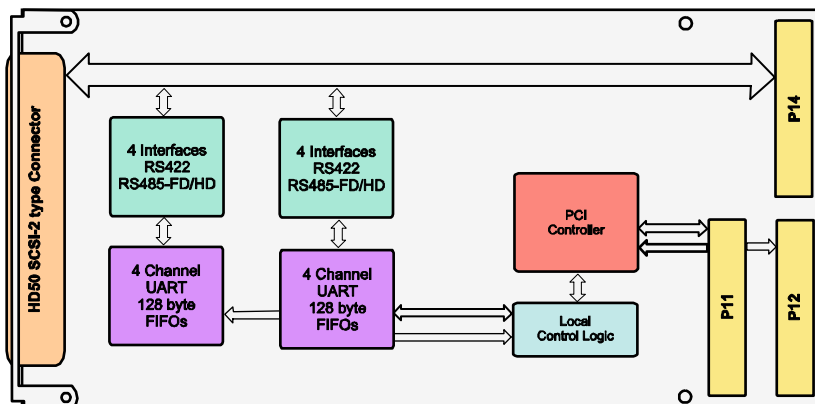


Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface	
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size
Electrical Interface	PCI Rev. 2.1 compliant 33 MHz / 32 bit PCI 5V PCI Signaling Voltage
On Board Devices	
PCI Target Chip	PCI9050-1 (PLX Technology)
Serial Controller	2x XR16C864 (Quad UART) (Exar)
Serial Interface	
Number of Channels	8
Physical Interface	RS422, RS485-FD (M/S) : TxD+, TxD-, RxD+, RxD-, GND RS485-HD : Dx+, Dx-, GND Configurable for each channel by DIP switch
Termination	Receive and transmit termination configurable by DIP switch
ESD Protection	+/-15kV Human Body Model +/- 8kV IEC 1000-4-2, Contact Discharge +/-15kV IEC 1000-4-2, Air-Gap Discharge
FIFO	128 byte transmit FIFO, 128 byte receive FIFO per channel
Baud Rates	Each channel programmable up to 460.8 kbaud
Interrupts	Using PCI INTA for all channels, on board Interrupt Status Register
I/O Connector	HD50 SCSI-2 type female connector (front I/O) PMC P14 I/O (64 pin Mezzanine Connector)
Physical Data	
Power Requirements	150mA typical @ +5V DC
Temperature Range	TPMC866-12 Operating 0 °C to +70 °C Storage -25°C to +125°C TPMC866-12-ET Operating -40 °C to +85 °C Storage -40°C to +125°C
MTBF	275743 h
Humidity	5 – 95 % non-condensing
Weight	75 g

Table 2-1 : Technical Specification

3 Local Space Addressing

3.1 PCI9050 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9050 local spaces.

PCI9050 Local Space	PCI9050 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	2 (0x18)	I/O	128	8	Little	Register Space

Table 3-1 : PCI9050 Local Space Configuration

3.2 Register Space

Base Address: PCI9050 PCI Base Address 2 for Local Space 0 (Offset 0x18 in PCI9050 PCI Configuration Space)

Offset	Description
0x00 to 0x07	Serial Channel 1 Register Set
0x08 to 0x0F	Serial Channel 2 Register Set
0x10 to 0x17	Serial Channel 3 Register Set
0x18 to 0x1F	Serial Channel 4 Register Set
0x20 to 0x27	Serial Channel 5 Register Set
0x28 to 0x2F	Serial Channel 6 Register Set
0x30 to 0x37	Serial Channel 7 Register Set
0x38 to 0x3F	Serial Channel 8 Register Set
0x40	FIFO Ready Register CH1-CH4
0x44	FIFO Ready Register CH5-CH8
0x48	Interrupt Status Register

Table 3-2 : Register Space Map

3.2.1 Serial Channel Register Set

Each serial channel belongs to a channel register set accessible in the PCI I/O space.

The address for a serial channel *register x* in a register set for *channel y* is:

- PCI Base Address 2 (see PCI9050 Target Chip)
- + Register Set Offset for *channel y* (see following tables)
- + Register Offset for *register x* (see following tables)

Because some serial channel registers overlap in the UART device address space, further access control must be programmed to access those registers.

Some serial channel registers are write only or read only registers.

All serial channel registers are byte sized.

Offset (to PCI Base Address) Base Address (of Register Set)	Description
0x00	Serial Channel 1 Register Set
0x08	Serial Channel 2 Register Set
0x10	Serial Channel 3 Register Set
0x18	Serial Channel 4 Register Set
0x20	Serial Channel 5 Register Set
0x28	Serial Channel 6 Register Set
0x30	Serial Channel 7 Register Set
0x38	Serial Channel 8 Register Set

Table 3-3 : Register Set Offset

Register Symbol	Register Name
DLL	Baud Rate Divisor LSB
DLM	Baud Rate Divisor MSB
EFR	Enhanced Feature Register
EMSR	Enhanced Mode Select Register
FC	FIFO Count Register
FCR	FIFO Control Register
FCTR	Feature Control Register
IER	Interrupt Enable Register
ISR	Interrupt Status Register
LCR	Line Control Register
LSR	Line Status Register
MCR	Modem Control Register
MSR	Modem Status Register
RHR	Receive Holding Register
SCPD	Scratchpad Register
THR	Transmit Holding Register
TRG	Trigger Level Register
XON1	Xon-1 Word
XON2	Xon-2 Word
XOFF1	Xoff-1 Word
XOFF2	Xoff-2 Word

Table 3-4 : Register Symbols

Please see the 16C864 data sheet for a complete description of these registers.

The following table provides the register offsets within a register set, access types and access control:

Access Control	Register Offset								Access Type
	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	
LCR Bit 7 = 0	RHR	IER	ISR	LCR	MCR	LSR	MSR	SCPD	Read
	THR	IER	FCR	LCR	MCR			SCPD	Write
LCR Bit 7 = 1 (but ≠ 0xBF)	DLL/ REV	DLM/ DID		LCR					Read
	DLL	DLM		LCR					Write
LCR = 0xBF	FC	FCTR	EFR	LCR	Xon1	Xon1	Xoff1	Xoff1	Read
	TRG	FCTR	EFR	LCR	Xon2	Xon2	Xoff2	Xoff2	Write

Table 3-5 : Serial Channel Register Offset and Access Control

3.2.2 Other Registers

For fast status detection there are two FIFO Status Register (one for channel 1 to 4 and one for channel 5 to 8) and an Interrupt Status Register covering all 8 channels.

Offset (to PCI Base Address)	Register Name	Size (Bit)
0x40	FIFO Ready Register 1 Channel 1-4	8
0x44	FIFO Ready Register 2 Channel 5-8	8
0x48	Interrupt Status Register	8

Table 3-6 : Special Register

3.2.2.1 FIFO Ready 1 Register (Channel 1-4)

The FIFO Ready Register 1 is a byte wide read only register. The FIFO Ready Register provides the real time status of the transmit and receive FIFO's of channel 1 to 4. Each TX and RX channel (1-4) has its own 128 byte FIFO. When any of the TX/RX FIFO's become empty/full, the status bit associated with the TX/RX function of channel 1-4 is set in the FIFO Ready Register.

Bit	Symbol	Description	Access	Reset Value
7	RXRDY 4	RX Ready Bit for channel 1-4	R	
6	RXRDY 3	0 = the corresponding receive FIFO is above the programmed trigger level or a time-out has occurred 1 = the receiver is ready and is below the programmed trigger level		
5	RXRDY 2			
4	RXRDY 1			
3	TXRDY 4	TX Ready Bit for channel 1-4	R	
2	TXRDY 3	0 = the corresponding transmit FIFO is full. This channel will not accept any more transmit data 1 = one or more empty locations exist in the corresponding FIFO		
1	TXRDY 2			
0	TXRDY 1			

Table 3-7 : FIFO Ready Register 1 (Channel 1-4)

3.2.2.2 FIFO Ready Register 2 (Channel 5-8)

The FIFO Ready Register 2 is a byte wide read only register. The FIFO Ready Register provides the real time status of the transmit and receive FIFO's of channel 5 to 8. Each TX and RX channel (5-8) has its own 128 byte FIFO. When any of the TX/RX FIFO's become empty/full, the status bit associated with the TX/RX function of channel 5-8 is set in the FIFO Ready Register.

Bit	Symbol	Description	Access	Reset Value
7	RXRDY 8	RX Ready Bit for channel 5-8 0 = the corresponding receive FIFO is above the programmed trigger level or a time-out has occurred 1 = the receiver is ready and is below the programmed trigger level	R	
6	RXRDY 7			
5	RXRDY 6			
4	RXRDY 5			
3	TXRDY 8	TX Ready Bit for channel 5-8 0 = the corresponding transmit FIFO is full. This channel will not accept any more transmit data 1 = one or more empty locations exist in the corresponding FIFO	R	
2	TXRDY 7			
1	TXRDY 6			
0	TXRDY 5			

Table 3-8 : FIFO Ready Register 2 (Channel 5-8)

3.2.2.3 Interrupt Status Register

The Interrupt Status Register ISR is a byte wide read only register located in the PCI Memory Space (PCI Base Address1 + 0x48) and reflects the interrupt status of the 8 serial channels.

Bit	Symbol	Description	Access	Reset Value
7	INT Channel 8	Interrupt Status of corresponding Channel 1-8 1 = interrupt is pending on corresponding channel 0 = no interrupt on corresponding channel	R	0x00
6	INT Channel 7			
5	INT Channel 6			
4	INT Channel 5			
3	INT Channel 4			
2	INT Channel 3			
1	INT Channel 2			
0	INT Channel 1			

Table 3-9 : Interrupt Status Register

Each of the 8 serial channels generates interrupts on the local interrupt 1 of the PCI target chip, which is mapped to PCI interrupt INTA.

If PCI interrupts are disabled in the PCI9050 PCI target chip (INTCSR bit 6 is set to '0') the Interrupt Status Register can be used as an interrupt status polling register for the 8 serial channels.

Interrupts of the 8 serial channels can be individually enabled / disabled by the ST16C864 UART registers. After reset all interrupts are disabled.

4 PCI9050 Target Chip

4.1 PCI Configuration Registers (PCR)

4.1.1 PCI9050 Header

PCI CFG Register Address	PCI9050 PCI Configuration Register								PCI writeable	Initial Values (Hex Values)
	31	24	23	16	15	8	7	0		
0x00	Device ID				Vendor ID				N	9050 10B5
0x04	Status				Command				Y	0280 0000
0x08	Class Code						Revision ID		N	070200 XX
0x0C	BIST	Header Type		PCI Latency Timer		Cache Line Size		Y[7:0]	00 00 00 00	
0x10	PCI Base Address 0 for MEM Mapped Config. Registers								Y	FFFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers								Y	FFFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0								Y	FFFFFFF81
0x1C	PCI Base Address 3 for Local Address Space 1								Y	00000000
0x20	PCI Base Address 4 for Local Address Space 2								Y	00000000
0x24	PCI Base Address 5 for Local Address Space 3								Y	00000000
0x28	PCI Cardbus Information Structure Pointer								N	00000000
0x2C	Subsystem ID				Subsystem Vendor ID				N	0362 1498
0x30	PCI Base Address for Local Expansion ROM								Y	00000000
0x34	Reserved						New Cap. Ptr.		N	00000000
0x38	Reserved								N	00000000
0x3C	Max_Lat	Min_Gnt		Interrupt Pin		Interrupt Line		Y[7:0]	00 00 01 00	

Table 4-1 : PCI9050 Header TPMC866-12

Device-ID : 0x9050 (PCI9050)
Vendor-ID : 0x10B5 (PLX Technology)
Subsystem-ID : 0x0362 (TPMC866)
Subvendor-ID : 0x1498 (TEWS TECHNOLOGIES)

4.1.2 PCI Base Address Initialization

PCI Base Address Initialization is scope of the PCI host software.

PCI9050 PCI Base Address Initialization:

- Write 0xFFFF_FFFF to the PCI9050 PCI Base Address Register.
- Read back the PCI9050 PCI Base Address Register.
- For PCI Base Address Registers 0:5, check bit 0 for PCI Address Space:
 - Bit 0 = '0' requires PCI Memory Space mapping
 - Bit 0 = '1' requires PCI I/O Space mapping
- For the PCI Expansion ROM Base Address Register, check bit 0 for usage:
 - Bit 0 = '0': Expansion ROM not used
 - Bit 0 = '1': Expansion ROM used
- Or PCI I/O Space mapping, starting at bit location 2, the first bit set determines the size of the required PCI I/O Space size.
 - For PCI Memory Space mapping, starting at bit location 4, the first bit set to '1' determines the size of the required PCI Memory Space size.
 - For PCI Expansion ROM mapping, starting at bit location 11, the first bit set to '1' determines the required PCI Expansion ROM size.
 - For example, if bit 5 of a PCI Base Address Register is detected as the first bit set to '1', the PCI9050 is requesting a 32 byte space (address bits 4:0 are not part of base address decoding).
- Determine the base address and write the base address to the PCI9050 PCI Base Address Register. For PCI Memory Space mapping the mapped address region must comply with the definition of bits 3:1 of the PCI9050 PCI Base Address Register.

After programming the PCI9050 PCI Base Address Registers, the software must enable the PCI9050 for PCI I/O and/or PCI Memory Space access in the PCI9050 PCI Command Register (Offset 0x04). To enable PCI I/O Space access to the PCI9050, set bit 0 to '1'. To enable PCI Memory Space access to the PCI9050, set bit 1 to '1'.

For further information please refer to the PCI9050 manual which is part of the TPMC866-ED-12 Engineering Documentation.

4.2 Local Configuration Register (LCR)

After reset, the PCI9050 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

The PCI base address for the PCI9050 Local Configuration Registers is:

PCI9050 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9050 PCI Configuration Register Space) or

PCI9050 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9050 PCI Configuration Register Space).

Do not change hardware dependent bit settings in the PCI9050 Local Configuration Registers.

Offset from PCI Base Address	Register	Value
0x00	Local Address Space 0 Range	0x0FFF_FF81
0x04	Local Address Space 1 Range	0x0000_0000
0x08	Local Address Space 2 Range	0x0000_0000
0x0C	Local Address Space 3 Range	0x0000_0000
0x10	Local Exp. ROM Range	0x0000_0000
0x14	Local Re-map Register Space 0	0x0000_0001
0x18	Local Re-map Register Space 1	0x0000_0000
0x1C	Local Re-map Register Space 2	0x0000_0000
0x20	Local Re-map Register Space 3	0x0000_0000
0x24	Local Re-map Register ROM	0x0000_0000
0x28	Local Address Space 0 Descriptor	0x5411_2880
0x2C	Local Address Space 1 Descriptor	0x0000_0000
0x30	Local Address Space 2 Descriptor	0x0000_0000
0x34	Local Address Space 3 Descriptor	0x0000_0000
0x38	Local Exp. ROM Descriptor	0x0000_0000
0x3C	Chip Select 0 Base Address	0x0000_0021
0x40	Chip Select 1 Base Address	0x0000_0043
0x44	Chip Select 2 Base Address	0x0000_0047
0x48	Chip Select 3 Base Address	0x0000_004B
0x4C	Interrupt Control/Status	0x0000_0041
0x50	Miscellaneous Control Register	0x0078_0240

Table 4-2 : PCI9050 Local Configuration Register

4.3 Configuration EEPROM

After power-on or PCI reset, the PCI9050 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x0E : PCI9050 PCI Configuration Register Values
- Address 0x10 to 0x62 : PCI9050 Local Configuration Register Values
- Address 0x64 to 0x7C : Not used
- Address 0x7E : TPMC variant

See the PCI9050 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x9050	0x10B5	0x0702	0x0000	0x0362	0x1498	0x0000	0x0100
0x10	0x0FFF	0xFF81	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x20	0x0000	0x0000	0x0000	0x0001	0x0000	0x0000	0x0000	0x0000
0x30	0x0000	0x0000	0x0000	0x0000	0x5411	0x2880	0x0000	0x0000
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0021
0x50	0x0000	0x0043	0x0000	0x0047	0x0000	0x004B	0x0000	0x0041
0x60	0x0078	0x0240	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x70	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	s.b.

Table 4-3 : Configuration EEPROM TPMC866-12

Board Option Value (Offset 0x7E): TPMC866-12 : 0x000C

4.4 PCI Interrupt Control/Status

PCI9050 PCI interrupts can be globally enabled / disabled by programming bit 6 of the PCI9050 Interrupt Control / Status Register (INTCSR) at offset 0x4C in the PCI9050 Local Configuration Register Space.

PCI Base Address for the PCI Memory mapped PCI9050 Local Configuration Register Space:
Offset 0x10 in the PCI9050 PCI Configuration Register Space.

INTCSR (Offset 0x4C) bit 6 = 0 disables PCI Interrupts, bit 6 = 1 enables PCI Interrupts.

4.5 Software Reset

The PCI9050 provides a Local Reset output (LRESET#) programmable in the PCI9050 Miscellaneous Control Register (CNTRL) at offset 0x50 in the PCI9050 Local Configuration Register Space.

PCI Base Address for the PCI Memory mapped PCI9050 Local Configuration Register Space:
Offset 0x10 in the PCI9050 PCI Configuration Register Space.

CNTRL (Offset 0x50) bit 30 = 0 de-asserts the LRESET# output, bit 30 = 1 asserts the LRESET# output.

The PCI9050 LRESET# output is used to reset the on board local logic. The PCI9050 controller will also be partly reset by this bit. The contents of the PCI and local configuration registers will not be reset.

4.6 Local Space Byte Ordering

The byte ordering for the PCI9050 Local Spaces is programmable in the Local Space Descriptor Registers in the PCI9050 Local Configuration Register Space.

PCI Base Address for the PCI Memory mapped PCI9050 Local Configuration Register Space:
Offset 0x10 in the PCI9050 PCI Configuration Register Space.

Offset for the Local Space 0 Descriptor Register: Offset 0x28

Offset for the Local Space 1 Descriptor Register: Offset 0x2C

In the Local Space Descriptor Registers bit 24 selects the local space byte ordering mode. A value of 1 indicates Big Endian; a value of 0 indicates Little Endian byte ordering.

5 Functional Description

For a detailed description of the UART functions please refer to the 16C864 UART data sheet (Exar) which is part of the TPMC866-ED-12 Engineering Documentation.

6 Programming Hints

6.1 Baud Rate Programming Formula

Each of the 8 serial isolated channels of the TPMC866-12 contains a programmable baud rate generator. The clock of the XR16C864 can be divided by any divisor from 1 to $2^{16} - 1$. The divisor can be programmed by the LSB and the MSB of the Divisor Latch Register. After reset the MCR bit 7 of each channel is default '0' and the value of LSB and MSB is 0xFFFF.

The basic formula of baud rate programming is:

$$\frac{7.3728MHz}{16 * DIVISOR * (1 + 3 * MCR_BIT7)}$$

Baud Rate MCR bit 7=0	Baud Rate MCR bit 7=1	Divisor	DLM Value	DLL Value
200	50	0x0900	0x09	0x00
300	75	0x0600	0x06	0x00
600	150	0x0300	0x03	0x00
1200	300	0x0180	0x01	0x80
2400	600	0x00C0	0x00	0xC0
4800	1200	0x0060	0x00	0x60
9600	2400	0x0030	0x00	0x30
19.2K	4800	0x0018	0x00	0x18
28.8K	7200	0x0010	0x00	0x10
38.4K	9600	0x000C	0x00	0x0C
76.8K	19.2K	0x0006	0x00	0x06
153.6K	38.4K	0x0003	0x00	0x03
230.4K	57.6K	0x0002	0x00	0x02
460.8K	115.2K	0x0001	0x00	0x01

Table 6-1 : Baud Rate Programming Table

Access to the DLM, DLL registers must be enabled in the LCR register.

These steps should be used to modify the DLM, DLL registers :

- Write 0x80 to LCR register (enable access to DLM, DLL registers)
- Modify DLM, DLL registers
- Write normal operation byte value to LCR register

The MCR (Modem Control Register) bits 5-7 must be enabled for modifying by setting EFR (Enhanced Feature Register) bit 4.

These steps should be used to modify MCR bit 7 :

- Write 0xBF to LCR register (enable access to EFR register)
- Set EFR register bit 4 to '1' (enable modification of MCR bits 5-7)
- Write 0x00 to LCR register (enable access to MCR register)
- Modify MCR bit 7
- Write 0xBF to LCR register (enable access to EFR register)
- Set EFR register bit 4 to '0' (Latch MCR bit setting)
- Write normal operation byte value to LCR register

7 Installation

7.1 I/O Connections

Connect channel I/O either to front I/O or P14 back I/O at a time. Do not connect an I/O channel to both front I/O connector and P14 back I/O connector at the same time.

The TPMC866-12 provides on board termination resistors. Do not apply additional external termination resistors here.

Please note that on the TPMC866-12, the P14 back I/O connector is always populated and connected to on board logic. Do not use these modules on carrier boards where P14/J14 is reserved for other system signals but PMC I/O. Ask support for special board options with front I/O only in this case.

7.2 Serial Channel Interface Overview

Figure below shows the hardware scheme of a TPMC866-12 serial channel interface.

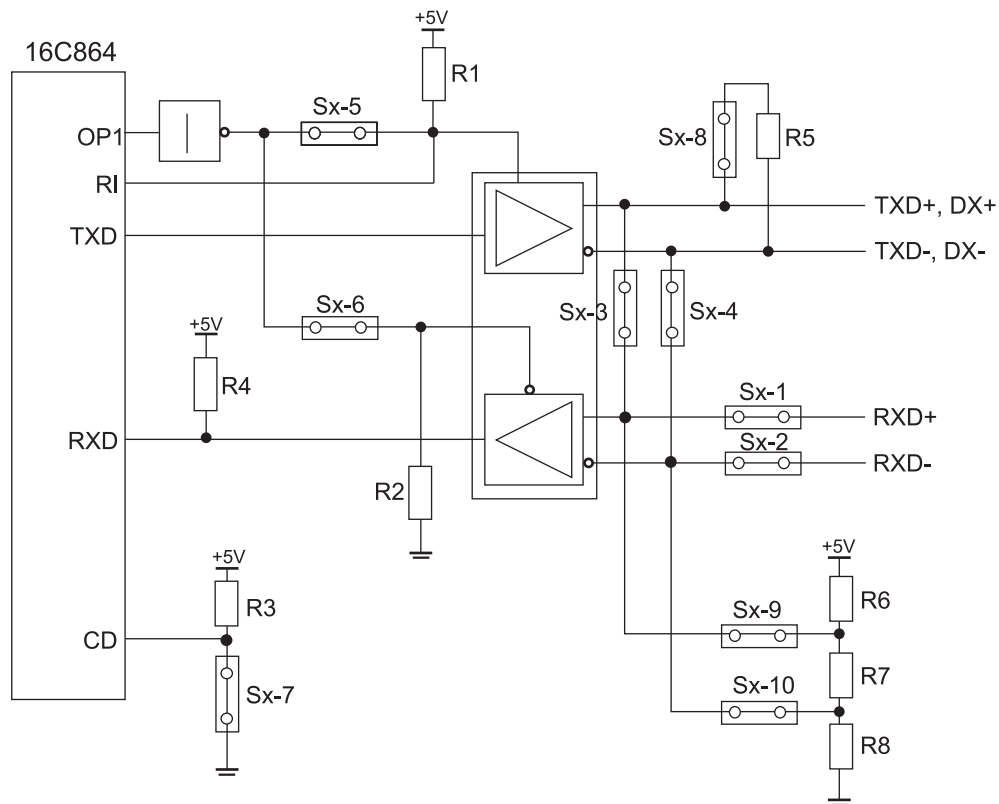


Figure 7-1 : Serial Channel Interface Overview

7.3 Serial Channel Interface Configuration

The serial channel interface is configurable by a DIP switch for each channel individually. There is a 10 switch DIP switch for each of the 8 serial channels.

Sx-y with x =1 to 8 (DIP switch for channel x) and y = 1 to 10 (switch number y within DIP switch x).

Switch ID	Function Group	Function	
Sx-1, Sx-2	Duplex Mode Configuration 1	ON	RS422 and RS485 FD Modes
		OFF	RS485 HD Mode
Sx-3, Sx-4	Duplex Mode Configuration 2	ON	RS485 HD Mode
		OFF	RS422 and RS485 FD Modes
Sx-5	Transmitter Enable Control	ON	Controlled by 16C864
		OFF	Transmitter Enabled
Sx-6	Receiver Enable Control	ON	Controlled by 16C864
		OFF	Receiver Enabled
Sx-7	Reserved	ON	Reserved
		OFF	
Sx-8	Transmit Line Termination	ON	120R Transmit Line Termination
		OFF	No Transmit Line Termination
Sx-9, Sx-10	Receive Line Termination	ON	120R Receive Line Termination
		OFF	No Receive Line Termination

FD: Full Duplex, HD: Half Duplex

Table 7-1 : DIP Switch Function

Mode	DIP Switch Configuration									
	Sx-1	Sx-2	Sx-3	Sx-4	Sx-5	Sx-6	Sx-7	Sx-8	Sx-9	Sx-10
RS422							X			
RS485 FD-M							X			
RS485 FD-S							X			
RS485 HD							X			

 Switch Closed (ON)

FD-M : Full Duplex Master

FD-S : Full Duplex Slave

HD : Half Duplex

X = Reserved

 Switch Open (OFF)


 Switch setting depends on bus configuration

Table 7-2 : DIP Switch Configuration

7.4 DIP Switch Locations

DIP Switch S1 is for channel 1 and so on.

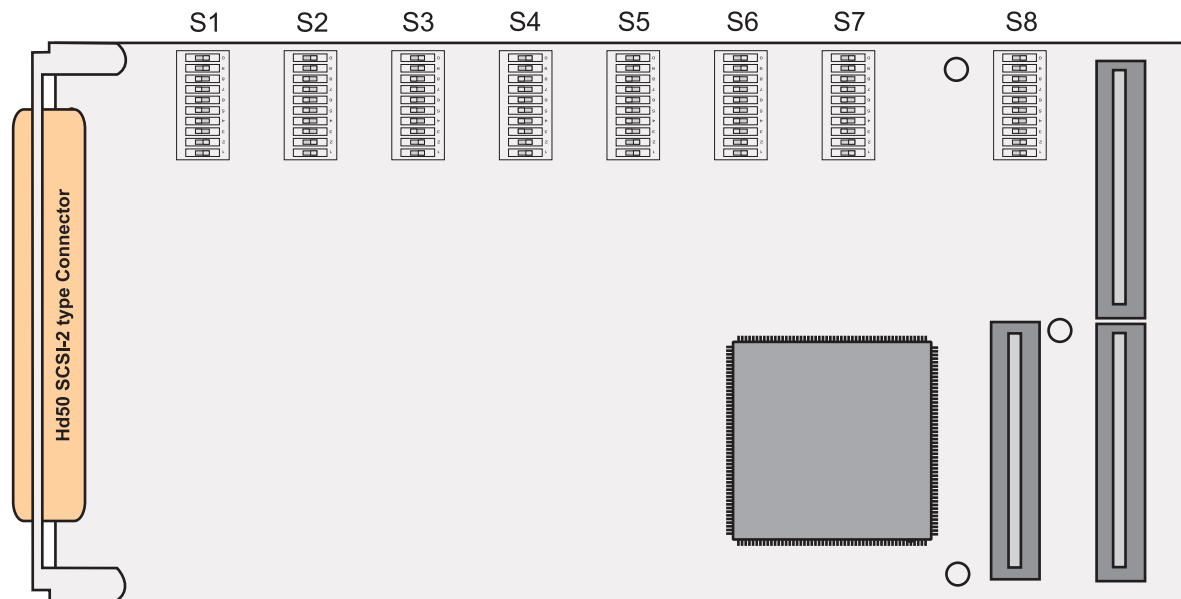


Figure 7-2 : DIP Switch Locations

7.5 Default Configuration

All 8 channels are configured to RS422 mode by factory default.

8 Pin Assignment – I/O Connector

Pin (front I/O & P14 I/O)	TPMC866-12 RS485-HD	TPMC866-12 RS422 / RS485-FD	Comment
1	GND	GND	Serial Channel 1
2	Dx0-	TxD0-	Serial Channel 1
3	Dx0+	TxD+	Serial Channel 1
4	-	RxD0-	Serial Channel 1
5	-	RxD0+	Serial Channel 1
6	GND	GND	Serial Channel 2
7	Dx1-	TxD1-	Serial Channel 2
8	Dx1+	TxD1+	Serial Channel 2
9	-	RxD1-	Serial Channel 2
10	-	RxD1+	Serial Channel 2
11	GND	GND	Serial Channel 3
12	Dx2-	TxD2-	Serial Channel 3
13	Dx2+	TxD2+	Serial Channel 3
14	-	RxD2-	Serial Channel 3
15	-	RxD2+	Serial Channel 3
16	GND	GND	Serial Channel 4
17	Dx3-	TxD3-	Serial Channel 4
18	Dx3+	TxD3+	Serial Channel 4
19	-	RxD3-	Serial Channel 4
20	-	RxD3+	Serial Channel 4
21	GND	GND	Serial Channel 5
22	Dx4-	TxD4-	Serial Channel 5
23	Dx4+	TxD4+	Serial Channel 5
24	-	RxD4-	Serial Channel 5
25	-	RxD4+	Serial Channel 5
26	GND	GND	Serial Channel 6
27	Dx5-	TxD5-	Serial Channel 6
28	Dx5+	TxD5+	Serial Channel 6
29	-	RxD5-	Serial Channel 6
30	-	RxD5+	Serial Channel 6
31	GND	GND	Serial Channel 7
32	Dx6-	TxD6-	Serial Channel 7
33	Dx6+	TxD6+	Serial Channel 7
34	-	RxD6-	Serial Channel 7
35	-	RxD6+	Serial Channel 7
36	GND	GND	Serial Channel 8
37	Dx7-	TxD7-	Serial Channel 8

Pin (front I/O & P14 I/O)	TPMC866-12 RS485-HD	TPMC866-12 RS422 / RS485-FD	Comment
38	Dx7+	TxD7+	Serial Channel 8
39	-	RxD7-	Serial Channel 8
40	-	RxD7+	Serial Channel 8
41	GND	GND	Opt. Termination Supply
42	+5V (not fused)	+5V (not fused)	Opt. Termination Supply
43...50 (front-I/O) 43...64 (back-I/O)	-	-	-

Table 8-1 : Pin Assignment I/O Connector

Connect channel I/O either to front I/O or P14 back I/O at a time. Do not connect an I/O channel to both front I/O connector and P14 back I/O connector at the same time.

The TPMC866-12 provides on board termination resistors. Do not apply additional external termination resistors here.

Please note that on the TPMC866-12, the P14 back I/O connector is always populated and connected to on board logic. Do not use these modules on carrier boards where P14/J14 is reserved for other system signals but PMC I/O. Ask support for special board options with front I/O only in this case.