The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC866

8 Channel Serial Interface

Version 1.0

User Manual

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TPMC866-10/-10-ET

8 channel RS232 serial interface PMC with front I/O and P14 I/O

TPMC866-11/-11-ET

8 channel RS422 serial interface PMC with front I/O and P14 I/O

TPMC866-10-ET

8 channel RS232 serial interface PMC with front I/O and P14 I/O, extended temperature range

TPMC866-11-ET

8 channel RS422 serial interface PMC with front I/O and P14 I/O, extended temperature range

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	March 1998
1.1	Addition PCI Target Chip and reduced variety	May 1999
1.2	General Revision	April 2003
1.3	Baud Rate Programming Note Update	December 2003
1.4	Added Module Versions TPMC866-xx-ET	May 2004

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1 Product Description

The TPMC866 is a standard single-width 32 bit PMC module and provides eight channels of high performance serial interface with front I/O and P14 back I/O.

The TPMC866-10 provides an 8 channel RS232 interface and supports Receive Data (RxD), Transmit Data (TxD), Ready-To-Send (RTS), Clear-To-Send (CTS) and GND for each channel. Additionally serial channel one and serial channel two provide Data-Set-Ready (DSR), Data-Terminal-Ready (DTR), Data-Carrier-Detect (DCD) and Ring-Detect-Indicator (RI).

The TPMC866-11 provides an 8 channel RS422 interface using differential line transceivers. The Transmit data (TxD +/-), Receive Data (RxD +/-) and GND signals are provided for each serial channel. The receiver signal termination for each channel (120ohm between RxD+ and RxD-) is provided on board the TPMC866.

Each channel of the TPMC866-10/11 has a 64 byte transmit FIFO and a 64 byte receive FIFO to significantly reduce the overhead required to provide data to and get data from the transmitters and receivers.

The baud rate is individually programmable for up to 460.8Kbaud per channel.

All channels use the PCI interrupt INTA. For fast interrupt source detection the TPMC866-xx provides an Interrupt Status Register covering all interrupt sources.

I/O line transceivers are protected against electrostatic discharge (ESD).

All TPMC866 modules are available in extended temperature range as TPMC866-xx-ET versions.

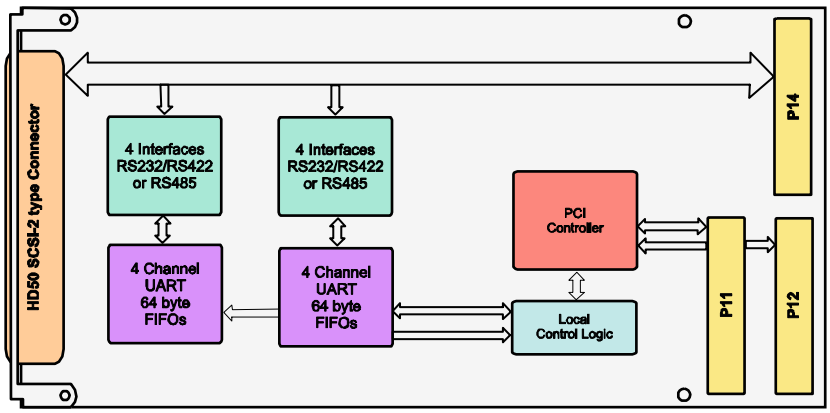

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size	
Electrical Interface	PCI Rev. 2.1 compliant 33 MHz / 32 bit PCI 5V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip	PCI9050-1 (PLX Technology)	
Serial Controller	2x ST16C654 (Quad UART) (Exar)	
Serial Interface		
Number of Serial Channels	8	
Physical Interface	TPMC866-10: RS232 TPMC866-11: RS422	
I/O Signals	TPMC866-10: TxD, RxD, RTS, CTS, GND Additionally for Channel 1 and 2: DTR, DSR, DCD, RI TPMC866-11: TxD+, TxD-, RxD+, RxD-, GND	
On Board Termination	TPMC866-11: 120 ohms between RxD+ and RxD- for each channel	
ESD Protection	+/-15kV Human Body Model +/- 8kV IEC 1000-4-2, Contact Discharge (RS232) +/-15kV IEC 1000-4-2, Air-Gap Discharge (RS232)	
FIFO	64 byte transmit FIFO, 64 byte receive FIFO per channel	
Baud Rates	Each channel programmable for up to 460.8 kbaud	
I/O Connector	HD50 SCSI-2 type female connector (front I/O) PMC P14 I/O (64 pin Mezzanine Connector)	
Physical Data		
Power Requirements	TPMC866-10: 180mA typical @ +5V DC TPMC866-11: 400mA typical @ +5V DC	
Temperature Range	TPMC866-10/-11 TPMC866-xx-ET	Operating: 0°C to +70 °C Storage: -25°C to +125°C Operating: -40°C to +85°C Storage: -40°C to +125°C
MTBF	TPMC866-10: 466809h TPMC866-11: 568266h	
Humidity	5 – 95 % non-condensing	
Weight	79 g	

Figure 2-1 : Technical Specification

3 Local Space Addressing

3.1 PCI9050 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9050 local spaces.

PCI9050 Local Space	PCI9050 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	2 (0x18)	I/O	128	8	Little	Register Space

Figure 3-1 : PCI9050 Local Space Configuration

3.2 Register Space

Base Address: PCI9050 PCI Base Address 2 for Local Space 0 (Offset 0x18 in PCI9050 PCI Configuration Space)

Offset	Description
0x00 to 0x07	Serial Channel 0 Register Set
0x08 to 0x0F	Serial Channel 1 Register Set
0x10 to 0x17	Serial Channel 2 Register Set
0x18 to 0x1F	Serial Channel 3 Register Set
0x20 to 0x27	Serial Channel 4 Register Set
0x28 to 0x2F	Serial Channel 5 Register Set
0x30 to 0x37	Serial Channel 6 Register Set
0x38 to 0x3F	Serial Channel 7 Register Set
0x40	FIFO Ready Register CH0-CH3
0x44	FIFO Ready Register CH4-CH7
0x48	Interrupt Status Register

Figure 3-2 : Register Space Map

3.2.1 Serial Channel Register Set

Each of the 8 serial channels of the TPMC866 is accessed in the TPMC866 Register Space by two register sets. Both register sets have a common register, the Line Control Register (LCR). Bit 7 of the Line Control Register is used to switch between the two register sets of a channel.

Offset (to PCI Base Address) Base Address (for Register Set)	Description
0x00	Serial Channel 0 Register Set
0x08	Serial Channel 1 Register Set
0x10	Serial Channel 2 Register Set
0x18	Serial Channel 3 Register Set
0x20	Serial Channel 4 Register Set
0x28	Serial Channel 5 Register Set
0x30	Serial Channel 6 Register Set
0x38	Serial Channel 7 Register Set

Figure 3-3 : Serial Channel Register Set Base Address

3.2.1.1 Channel Register Set 1

Channel Register Set 1 is accessible if bit 7 of the Line Control Register is set to '0'. After reset Channel Register Set 1 is accessible for each channel.

Offset (to Register Set Base Address)	Read Mode	Write Mode	Size (Bit)
0x00	Receive Holding Register	Transmit Holding Register	8
0x01	-	Interrupt Enable Register	8
0x02	Interrupt Status Register	FIFO Control Register	8
0x03	-	Line Control Register (LCR)	8
0x04	-	Modem Control Register	8
0x05	Line Status Register	-	8
0x06	Modem Status Register	-	8
0x07	Scratchpad Register	Scratchpad Register	8

Figure 3-4 : Channel Register Set 1

3.2.1.2 Channel Register Set 2

Channel Register Set 2 is accessible if bit 7 of the Line Control Register is set to '1'. The Enhanced Feature Register, Xon-1/2 and Xoff-1/2 registers are accessible if the Line Control Register is set to 0xBF.

Offset (to Register Set Base Address)	Read / Write Mode	Size (Bit)	Access Enable Control
0x00	LSB of Divisor Latch (DLL)	8	LCR bit 7 set to '1' (but ≠ 0xBF)
0x01	MSB of Divisor Latch (DLM)	8	LCR bit 7 set to '1' (but ≠ 0xBF)
0x02	Enhanced Feature Register (EFR)	8	LCR set to 0xBF
0x03	Line Control Register (LCR)	8	Always accessible
0x04	Xon-1 Word	8	LCR set to 0xBF
0x05	Xon-2 Word	8	LCR set to 0xBF
0x06	Xoff-1 Word	8	LCR set to 0xBF
0x07	Xoff-2 Word	8	LCR set to 0xBF

Figure 3-5 : Channel Register Set 2

3.2.2 Other Registers

For fast status detection there are two FIFO Status Register (one for channel 0 to 3 and one for channel 4 to 7) and an Interrupt Status Register covering all 8 channels.

Offset	Register Name	Size (Bit)
0x40	FIFO Ready Register 1 (Channel 0-3)	8
0x44	FIFO Ready Register 2 (Channel 4–7)	8
0x48	Interrupt Status Register	8

Figure 3-6 : Special Register

3.2.2.1 FIFO Ready 1 Register Channel 0-3

The FIFO Ready Register 1 is a byte wide read only register. The FIFO Ready Register provides the real time status of the transmit and receive FIFO's of channel 0 to 3. Each TX and RX channel (0-3) has its own 64 byte FIFO. When any of the TX/RX FIFO's become empty/full, the status bit associated with the TX/RX function of channel 0-3 is set in the FIFO Ready Register.

Bit	Symbol	Description	Access
7	RXRDY Channel 3	RX Ready Bit for Channel 0-3 0 = the corresponding receive FIFO is above the programmed trigger level or a time-out has occurred 1 = the receiver is ready and is below the programmed trigger level	R
6	RXRDY Channel 2		
5	RXRDY Channel 1		
4	RXRDY Channel 0		
3	TXRDY Channel 3	TX Ready Bit for Channel 0-3 0 = the corresponding transmit FIFO is full. This channel will not accept any more transmit data 1 = one or more empty locations exist in the corresponding FIFO	R
2	TXRDY Channel 2		
1	TXRDY Channel 1		
0	TXRDY Channel 0		

Figure 3-7 : FIFO Ready Register 1 (Channel 0-3)

3.2.2.2 FIFO Ready 2 Register Channel 4-7

The FIFO Ready Register FIFORDY2 is a byte wide read only register. The FIFO Ready Register provides the real time status of the transmit and receive FIFO's of channel 4 to 7. Each TX and RX channel (4-7) has its own 64 byte FIFO. When any of the TX/RX FIFO's become empty/full, the status bit associated with the TX/RX function of channel 4-7 is set in the FIFO Ready Register.

Bit	Symbol	Description	Access	Reset Value
7	RXRDY Channel 7	RX Ready Bit for Channel 4-7 0 = the corresponding receive FIFO is above the programmed trigger level or a time-out has occurred 1 = the receiver is ready and is below the programmed trigger level	R	
6	RXRDY Channel 6			
5	RXRDY Channel 5			
4	RXRDY Channel 4			
3	TXRDY Channel 7	TX Ready Bit for Channel 4-7 0 = the corresponding transmit FIFO is full. This channel will not accept any more transmit data 1 = one or more empty locations exist in the corresponding FIFO	R	
2	TXRDY Channel 6			
1	TXRDY Channel 5			
0	TXRDY Channel 4			

Figure 3-8 : FIFO Ready Register 2 (Channel 4-7)

3.2.2.3 Interrupt Status Register

The Interrupt Status Register is a byte wide read only register located in the PCI Memory Space (PCI Base Address1 + 0x48) and reflects the interrupt status for the 8 serial channels.

Bit	Symbol	Description	Access	Reset Value
7	Interrupt Channel 7	Interrupt Status of Channel 0-7 0 = no pending interrupt 1 = indicates pending interrupt	R	0x00
6	Interrupt Channel 6			
5	Interrupt Channel 5			
4	Interrupt Channel 4			
3	Interrupt Channel 3			
2	Interrupt Channel 2			
1	Interrupt Channel 1			
0	Interrupt Channel 0			

Figure 3-9 : Interrupt Status Register

Each of the 8 serial channels generates interrupts on the local interrupt 1 of the PCI target chip, which is mapped to PCI interrupt INTA.

If PCI interrupts are disabled in the PCI9050 PCI target chip (INTCSR bit 6 is set to '0') the Interrupt Status Register can be used as an interrupt status polling register for the 8 serial channels.

Interrupts of the 8 serial channels can be individually enabled / disabled by the ST16C654 UART registers. After reset all interrupts are disabled.

4 PCI9050 Target Chip

4.1 PCI Configuration Registers (PCR)

4.1.1 PCI9050 Header

PCI CFG Register Address	PCI9050 PCI Configuration Register								PCI writeable	Initial Values (Hex Values)
	31	24	23	16	15	8	7	0		
0x00	Device ID				Vendor ID				N	9050 10B5
0x04	Status				Command				Y	0280 0000
0x08	Class Code						Revision ID		N	118000 XX
0x0C	BIST		Header Type		PCI Latency Timer		Cache Line Size		Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers								Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers								Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0								Y	FFFFFF81
0x1C	PCI Base Address 3 for Local Address Space 1								Y	00000000
0x20	PCI Base Address 4 for Local Address Space 2								Y	00000000
0x24	PCI Base Address 5 for Local Address Space 3								Y	00000000
0x28	PCI Cardbus Information Structure Pointer								N	00000000
0x2C	Subsystem ID				Subsystem Vendor ID				N	0362 1498
0x30	PCI Base Address for Local Expansion ROM								Y	00000000
0x34	Reserved								N	00000000
0x38	Reserved								N	00000000
0x3C	Max_Lat		Min_Gnt		Interrupt Pin		Interrupt Line		Y[7:0]	00 00 01 00

Figure 4-1 : PCI9050 Header TPMC866

Device-ID: 0x9050 (PCI9050)

Vendor-ID: 0x10B5 (PLX Technology)

Subsystem-ID: 0x0362 (TPMC866)

Subvendor-ID: 0x1498 (TEWS TECHNOLOGIES)

4.1.2 PCI Base Address Initialization

PCI Base Address Initialization is scope of the PCI host software.

PCI9050 PCI Base Address Initialization:

- Write 0xFFFF_FFFF to the PCI9050 PCI Base Address Register.
- Read back the PCI9050 PCI Base Address Register.
- For PCI Base Address Registers 0:5, check bit 0 for PCI Address Space:

  Bit 0 = '0' requires PCI Memory Space mapping

  Bit 0 = '1' requires PCI I/O Space mapping

  For the PCI Expansion ROM Base Address Register, check bit 0 for usage:

  Bit 0 = '0': Expansion ROM not used

  Bit 0 = '1': Expansion ROM used

- Or PCI I/O Space mapping, starting at bit location 2, the first bit set determines the size of the required PCI I/O Space size.

  For PCI Memory Space mapping, starting at bit location 4, the first bit set to '1' determines the size of the required PCI Memory Space size.

  For PCI Expansion ROM mapping, starting at bit location 11, the first bit set to '1' determines the required PCI Expansion ROM size.

  For example, if bit 5 of a PCI Base Address Register is detected as the first bit set to '1', the PCI9050 is requesting a 32 byte space (address bits 4:0 are not part of base address decoding).

- Determine the base address and write the base address to the PCI9050 PCI Base Address Register. For PCI Memory Space mapping the mapped address region must comply with the definition of bits 3:1 of the PCI9050 PCI Base Address Register.

  After programming the PCI9050 PCI Base Address Registers, the software must enable the PCI9050 for PCI I/O and/or PCI Memory Space access in the PCI9050 PCI Command Register (Offset 0x04). To enable PCI I/O Space access to the PCI9050, set bit 0 to '1'. To enable PCI Memory Space access to the PCI9050, set bit 1 to '1'.

For further information please refer to the PCI9050 manual which is part of the TPMC866-ED Engineering Documentation.

4.2 Local Configuration Register (LCR)

After reset, the PCI9050 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

The PCI base address for the PCI9050 Local Configuration Registers is:

PCI9050 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9050 PCI Configuration Register Space) or

PCI9050 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9050 PCI Configuration Register Space).

Do not change hardware dependent bit settings in the PCI9050 Local Configuration Registers.

Offset	Register	Value
0x00	Local Address Space 0 Range	0x0FFF_FF81
0x04	Local Address Space 1 Range	0x0000_0000
0x08	Local Address Space 2 Range	0x0000_0000
0x0C	Local Address Space 3 Range	0x0000_0000
0x10	Local Exp. ROM Range	0x0000_0000
0x14	Local Re-map Register Space 0	0x0000_0001
0x18	Local Re-map Register Space 1	0x0000_0000
0x1C	Local Re-map Register Space 2	0x0000_0000
0x20	Local Re-map Register Space 3	0x0000_0000
0x24	Local Re-map Register ROM	0x0000_0000
0x28	Local Address Space 0 Descriptor	0x5411_2880
0x2C	Local Address Space 1 Descriptor	0x0000_0000
0x30	Local Address Space 2 Descriptor	0x0000_0000
0x34	Local Address Space 3 Descriptor	0x0000_0000
0x38	Local Exp. ROM Descriptor	0x0000_0000
0x3C	Chip Select 0 Base Address	0x0000_0021
0x40	Chip Select 1 Base Address	0x0000_0043
0x44	Chip Select 2 Base Address	0x0000_0047
0x48	Chip Select 3 Base Address	0x0000_004B
0x4C	Interrupt Control/Status	0x0000_0041
0x50	Miscellaneous Control Register	0x0078_0240

Figure 4-2 : PCI9050 Local Configuration Register

4.3 Configuration EEPROM

After power-on or PCI reset, the PCI9050 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x0F: PCI9050 PCI Configuration Register Values
- Address 0x10 to 0x64: PCI9050 Local Configuration Register Values
- Address 0x65 to 0x7C: Not used
- Address 0x7E: TPMC variant

See the PCI9050 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x9050	0x10B5	0x0702	0x0000	0x0362	0x1498	0x0000	0x0100
0x10	0x0FFF	0xFF81	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x20	0x0000	0x0000	0x0000	0x0001	0x0000	0x0000	0x0000	0x0000
0x30	0x0000	0x0000	0x0000	0x0000	0x5411	0x2880	0x0000	0x0000
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0021
0x50	0x0000	0x0043	0x0000	0x0047	0x0000	0x004B	0x0000	0x0041
0x60	0x0078	0x0240	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x70	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	s.b.

Figure 4-3 : Configuration EEPROM TPMC866-xx

Board Option Value (Offset 0x7E): TPMC866-10: 0x000A

TPMC866-11: 0x000B

4.4 PCI Interrupt Control/Status

PCI9050 PCI interrupts can be globally enabled / disabled by programming bit 6 of the PCI9050 Interrupt Control / Status Register (INTCSR) at offset 0x4C in the PCI9050 Local Configuration Register Space.

PCI Base Address for the PCI Memory mapped PCI9050 Local Configuration Register Space:
Offset 0x10 in the PCI9050 PCI Configuration Register Space.

INTCSR (Offset 0x4C) bit 6 = 0 disables PCI Interrupts, bit 6 = 1 enables PCI Interrupts.

4.5 Software Reset

The PCI9050 provides a Local Reset output (LRESET#) programmable in the PCI9050 Miscellaneous Control Register (CNTRL) at offset 0x50 in the PCI9050 Local Configuration Register Space.

PCI Base Address for the PCI Memory mapped PCI9050 Local Configuration Register Space: Offset 0x10 in the PCI9050 PCI Configuration Register Space.

CNTRL (Offset 0x50) bit 30 = 0 de-asserts the LRESET# output; bit 30 = 1 asserts the LRESET# output.

The PCI9050 LRESET# output is used to reset the on board local logic. The PCI9050 controller will also be partly reset by this bit. The contents of the PCI and local configuration registers will not be reset.

4.6 Local Space Byte Ordering

The byte ordering for the PCI9050 Local Spaces is programmable in the Local Space Descriptor Registers in the PCI9050 Local Configuration Register Space.

PCI Base Address for the PCI Memory mapped PCI9050 Local Configuration Register Space: Offset 0x10 in the PCI9050 PCI Configuration Register Space.

Offset for the Local Space 0 Descriptor Register: Offset 0x28

Offset for the Local Space 1 Descriptor Register: Offset 0x2C

In the Local Space Descriptor Registers bit 24 selects the local space byte ordering mode. A value of 1 indicates Big Endian; a value of 0 indicates Little Endian byte ordering.

5 Functional Description

For a detailed description of the UART functions please refer to the 16C654 UART data sheet (Exar) which is part of the TPMC866-ED Engineering Documentation.

6 Programming Hints

6.1 Baud Rate Programming Formula

Each of the 8 serial isolated channels of the TPMC866 contains a programmable baud rate generator. The clock of the ST16C654 can divided by any divisor from 1 to 2^{16} – 1. The divisor can be programmed by the LSB and the MSB of the Divisor Latch Register. After reset the MCR bit 7 of each channel is default '0' and the value of LSB and MSB is 0xFFFF.

The basic formula of baud rate programming is:

$$\frac{7.3728MHz}{16 * DIVISOR * (1 + 3 * MCR\_BIT7)}$$

Baud Rate MCR bit 7=0	Baud Rate MCR bit 7=1	Divisor (DLM, DLL)
200	50	0x0900
300	75	0x0600
600	150	0x0300
1200	300	0x0180
2400	600	0x00C0
4800	1200	0x0060
9600	2400	0x0030
19.2K	4800	0x0018
28.8K	7200	0x0010
38.4K	9600	0x000C
76.8K	19.2K	0x0006
153.6K	38.4K	0x0003
230.4K	57.6K	0x0002
460.8K	115.2K	0x0001

Figure 6-1 : Baud Rate Programming Table

Access to the DLM, DLL registers must be enabled in the LCR register.

These steps should be used to modify the DLM, DLL registers :

- **Write 0x80 to LCR register (enable access to DLM, DLL registers)**
- **Modify DLM, DLL registers**
- **Write normal operation byte value to LCR register**

The MCR (Modem Control Register) bits 5-7 must be enabled for modifying by setting EFR (Enhanced Feature Register) bit 4.

These steps should be used to modify MCR bit 7 :

- **Write 0xBF to LCR register (enable access to EFR register)**
- **Set EFR register bit 4 to '1' (enable modification of MCR bits 5-7)**
- **Write 0x00 to LCR register (enable access to MCR register)**
- **Modify MCR bit 7**
- **Write 0xBF to LCR register (enable access to EFR register)**
- **Set EFR register bit 4 to '0' (Latch MCR bit setting)**
- **Write normal operation byte value to LCR register**

7 Installation Hints

Connect channel I/O either to front I/O or P14 back I/O at a time. Do not connect an I/O channel to both front I/O connector and P14 back I/O connector at the same time.

The TPMC866-11 (RS422) provides on board 120ohms termination resistors. Do not apply additional external 120ohms termination resistors here.

Please note that on the TPMC866-10 and TPMC866-11, the P14 back I/O connector is always populated and connected to on board logic. Do not use these modules on carrier boards where P14/J14 is reserved for other system signals but PMC I/O. Ask support for special board options with front I/O only in this case.

8 I/O Connector Pin Assignment

Pin Number (front I/O & P14 I/O)	TPMC866-10 RS232 Interface	TPMC866-11 RS422 Interface	Comment
1	GND	GND	Serial Channel 0
2	TxD0	TxD0-	Serial Channel 0
3	RxT0	TxD+	Serial Channel 0
4	RTS0	RxD0-	Serial Channel 0
5	CTS0	RxD0+	Serial Channel 0
6	GND	GND	Serial Channel 1
7	TxD1	TxD1-	Serial Channel 1
8	RxT1	TxD1+	Serial Channel 1
9	RTS1	RxD1-	Serial Channel 1
10	CTS1	RxD1+	Serial Channel 1
11	GND	GND	Serial Channel 2
12	TxD2	TxD2-	Serial Channel 2
13	RxT2	TxD2+	Serial Channel 2
14	RTS2	RxD2-	Serial Channel 2
15	CTS2	RxD2+	Serial Channel 2
16	GND	GND	Serial Channel 3
17	TxD3	TxD3-	Serial Channel 3
18	RxT3	TxD3+	Serial Channel 3
19	RTS3	RxD3-	Serial Channel 3
20	CTS3	RxD3+	Serial Channel 3
21	GND	GND	Serial Channel 4
22	TxD4	TxD4-	Serial Channel 4
23	RxT4	TxD4+	Serial Channel 4
24	RTS4	RxD4-	Serial Channel 4
25	CTS4	RxD4+	Serial Channel 4
26	GND	GND	Serial Channel 5
27	TxD5	TxD5-	Serial Channel 5
28	RxT5	TxD5+	Serial Channel 5
29	RTS5	RxD5-	Serial Channel 5
30	CTS5	RxD5+	Serial Channel 5
31	GND	GND	Serial Channel 6
32	TxD6	TxD6-	Serial Channel 6
33	RxT6	TxD6+	Serial Channel 6
34	RTS6	RxD6-	Serial Channel 6
35	CTS6	RxD6+	Serial Channel 6

Pin Number (front I/O & P14 I/O)	TPMC866-10 RS232 Interface	TPMC866-11 RS422 Interface	Comment
36	GND	GND	Serial Channel 7
37	TxD7	TxD7-	Serial Channel 7
38	RxT7	TxD7+	Serial Channel 7
39	RTS7	RxD7-	Serial Channel 7
40	CTS7	RxD7+	Serial Channel 7
41	GND	GND	Termination Bias Supply
42	+5V	+5V	Termination Bias Supply
43	CD0	-	Data Carrier Detect CH0
44	DTR0	-	Data Terminal Ready CH0
45	RI0	-	Ring Indicator CH0
46	DSR0	-	Data Set Ready CH0
47	CD1	-	Data Carrier Detect CH1
48	DTR1	-	Data Terminal Ready CH1
49	RI1	-	Ring Indicator CH1
50	DSR1	-	Data Set Ready CH1
51 ... 64 (P14 I/O Only)	-	-	-

Figure 8-1 : I/O Connector Pin Assignment

Connect channel I/O either to front I/O or P14 back I/O at a time. Do not connect an I/O channel to both front I/O connector and P14 back I/O connector at the same time.

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