



PMCSpan PMC Carrier Module

Installation and Use

6806800A59B

September 2008



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Safety Summary

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

The safety precautions listed below represent warnings of certain dangers of which Emerson is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. If the equipment is supplied with a three-conductor AC power cable, the power cable must be plugged into an approved three-contact electrical outlet, with the grounding wire (green/yellow) reliably connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards and local electrical regulatory codes.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in any explosive atmosphere such as in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment could result in an explosion and cause injury or damage.

Keep Away From Live Circuits Inside the Equipment.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Service personnel should not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, such personnel should always disconnect power and discharge circuits before touching components.

Use Caution When Exposing or Handling a CRT.

Breakage of a Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, do not handle the CRT and avoid rough handling or jarring of the equipment. Handling of a CRT should be done only by qualified service personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Emerson representative for service and repair to ensure that all safety features are maintained.

Observe Warnings in Manual.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.



To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.

Flammability

All Emerson PWBs (printed wiring boards) are manufactured with a flammability rating of 94V-0 by UL-recognized manufacturers.

EMI Caution



This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used with adequate EMI protection.

CE Notice (European Community)



This is a Class A product. In a domestic environment, this product may cause radio interference, in which case the user may be required to take adequate measures.

Emerson products with the CE marking comply with the EMC Directive (89/336/EEC). Compliance with this directive implies conformity to the following European Norms:

EN55022 "Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment"; this product tested to Equipment Class A

EN 300 386 V.1.2.1 "Electromagnetic compatibility and radio spectrum matters (ERM); Telecommunication network equipment; Electromagnetic compatibility (EMC) requirements"

System products also fulfill EN60950 (product safety) which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

Board products are tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a CE-marked system will maintain the required EMC/safety performance.

In accordance with European Community directives, a "Declaration of Conformity" has been made and is on file within the European Union. The "Declaration of Conformity" is available on request. Please contact your sales representative.

The product has been designed to meet the directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS) Directive 2002/95/EC.

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PMCspan is a PMC carrier module that provides PCI expansion capability for a host VME processor module. The PMCspan has two PMC slots which support either two single-wide PMC modules or one double-wide PMC module. Two PMCspans can be stacked on a host VME processor, allowing up to four additional PMC modules.

PMCspan Models

As of the publication of this manual, the following PMCspan models are supported.

| Model Number | Description |
|--|---|
| PMCSPAN16E-002 | Primary PMC Carrier Module that attaches to the MVME51005E/MVME55006E and provides two PMC slots. It includes a PLX PCI6150 PCI-to-PCI bridge chip with 32-bit PCI support, and accepts a PMCspan26E-010 Secondary PCI Expansion Module. Scanbe handles. |
| PMCSPAN26E-002 | Primary PMC Carrier Module that attaches to the MVME51005E/MVME55006E and provides two PMC slots. It includes a PLX PCI16150 PCI-to-PCI bridge chip with 32-bit PCI support and accepts a PMCspan16E-010 Secondary PCI Expansion Module. IEEE handles. |
| PMCSPAN16E-010 | Secondary PMC Carrier Module that attaches to a PMCspan16E-002 and provides two PMC slots. The PMCspan16E-010 is identical to the PMCspan16E-002 except that the PCI-to-PCI bridge chip, the Clock Configuration logic, and the primary PCI expansion connector are not present. Scanbe handles. |
| PMCSPAN26E-010 | Secondary PMC Carrier Module that attaches to either a PMCspan26E-002 and provides two PMC slots. The PMCspan26E-010 is identical to the PMCspan26E-002 except that the PCI-to-PCI bridge chip, the Clock Configuration logic, and the primary PCI expansion connector are not present. IEEE handles. |
| All PMCspan models provide both front panel and VME bus I/O. | |

Overview of Contents

This manual is divided into the following chapters and appendices:

Chapter 1, PMCspan Introduction

Chapter 2, Hardware Installation

Chapter 3, Functional Description

Chapter 4, Programming Model

Chapter 5, Connectors

Appendix A, Related Documentation

This manual is intended for anyone who wants to supply OEM systems, add capability to an existing compatible system, and/or work in a lab environment for experimental purposes. A basic knowledge of computers and digital logic is assumed.

Summary of Changes

This manual has been revised and replaces all prior editions.

| Part Number | Publication Date | Description |
|-------------|------------------|--|
| 6806800A59A | July 2006 | First edition |
| 6806800A59B | September 2008 | Update document to Emerson style (logo, copyright, trademark, etc) |

Comments and Suggestions

We welcome and appreciate your comments on our documentation. We want to know what you think about our manuals and how we can make them better.

Mail comments to us by filling out the following online form:

<http://www.emersonnetworkpowerembeddedcomputing.com/> > Contact Us > Online Form

In "Area of Interest" select "Technical Documentation". Be sure to include the title, part number, and revision of the manual and tell us how you used it.

Conventions Used in This Manual

The following typographical conventions are used in this document:

bold

is used for user input that you type just as it appears; it is also used for commands, options and arguments to commands, and names of programs, directories and files.

italic

is used for names of variables to which you assign values. Italic is also used for comments in screen displays and examples, and to introduce new terms.

`courier`

is used for system output (for example, screen displays, reports), examples, and system prompts.

<Enter>, <Return> or <CR>

represents the carriage return or Enter key.

Ctrl

represents the Control key. Execute control characters by pressing the Ctrl key and the letter simultaneously, for example, Ctrl-d.

The PMCSpan is a PMC carrier module that provides PCI expansion capability. PMCSpans have the following features:

- ❑ Compatible with the MVME51005E and MVME55006E processor modules (hereafter referred to as the MVME5100 and MVME5500 processor modules)
- ❑ Support for two single-width PMC module or one double-width PMC module
- ❑ +5V bus signaling voltage
- ❑ Support for both PMC Bus and VMEbus connectors with the following features:
 - Two sets of three EIA E700 AAAB connectors for 32-bit PMC interface to secondary PCI bus and user specific I/O
 - P1 connector for power and BGNT and IACK daisy chaining
 - 5-row P2 connector for power and PMC I/O
- ❑ PCI6150 PCI-to-PCI Bridge Interface device, with the following features:
 - PCI Revision 2.1 compliant
 - 32-bit primary bus interface
 - 32-bit secondary bus interface
 - Delayed transactions for all PCI configuration, I/O, and memory read commands, allowing up to three transactions simultaneously in each direction
 - Buffering (data and address) for posted memory write commands in each direction, allowing up to five posted write transactions simultaneously in each direction
 - Read data buffering in each direction
 - Concurrent primary and secondary bus operation to isolate traffic
 - Enhanced address decoding
 - PCI transaction forwarding

PMCspan Mechanical Layouts

The next figures show the component side layout and front panel features for the PMCspan16E-002.

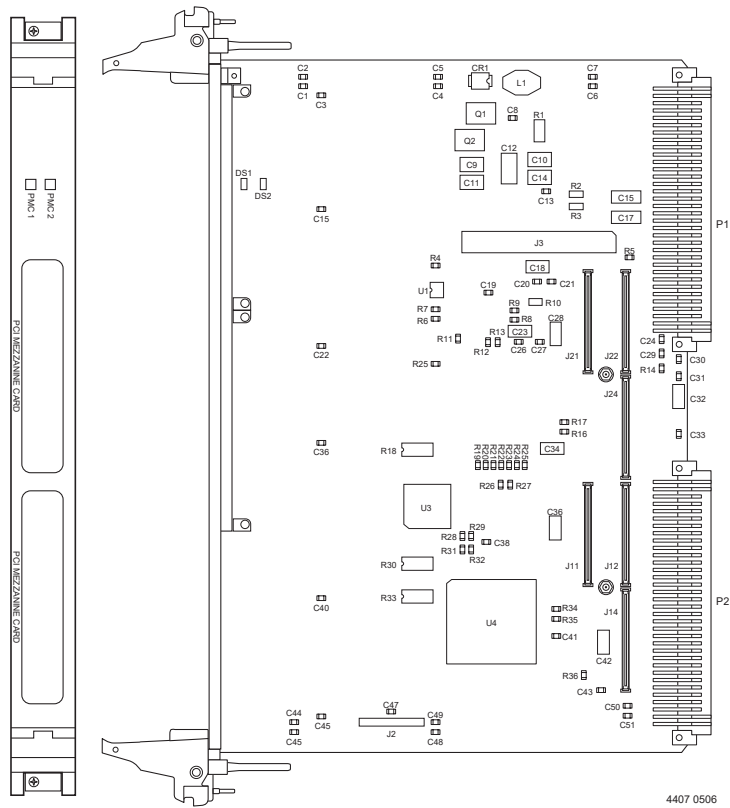


Figure 1-1. PMCspan16E-002 Component Layout and Front Panel

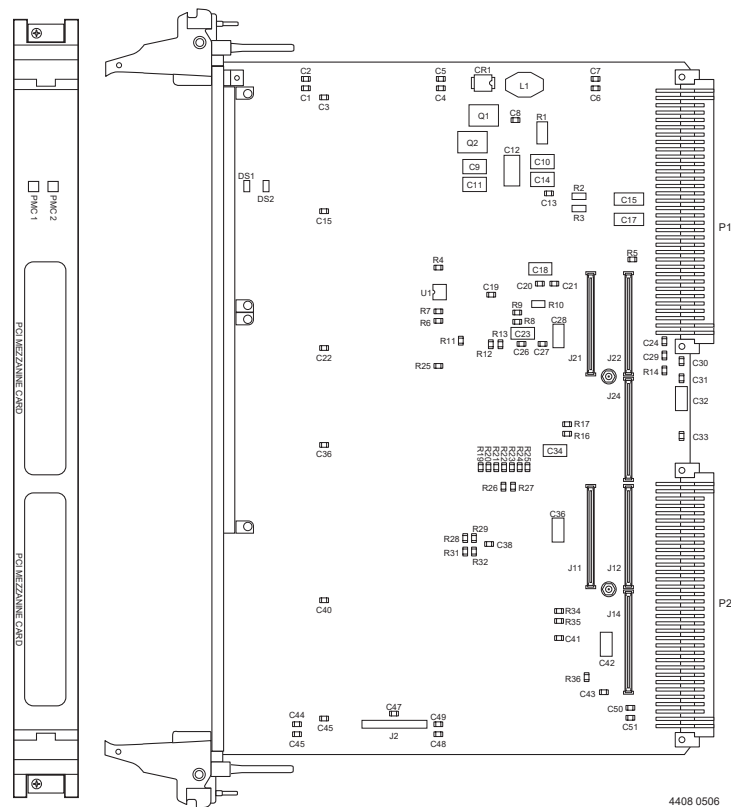
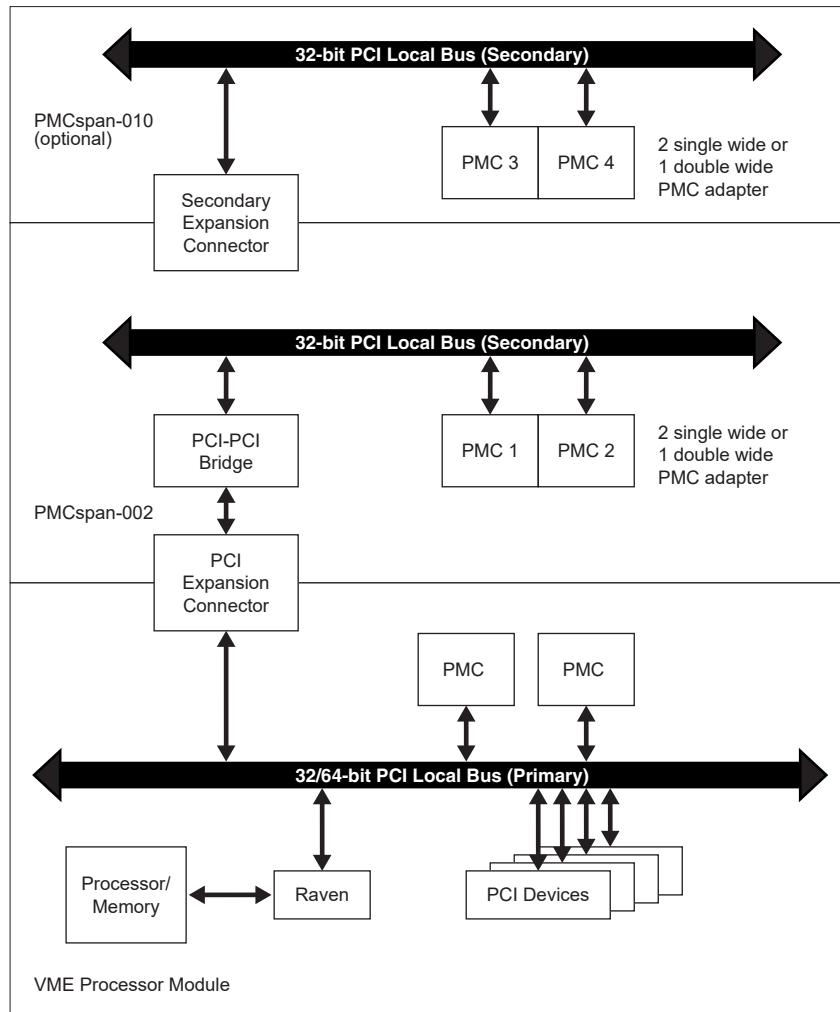


Figure 1-2. PMCspan16E-010 Component Layout and Front Panel

VME Processor/PMCspan System

Figure 1-3 shows a block diagram of a PMCspan system: a VME processor module, a PMCspan16E-002 primary PMC carrier module, and a PMCspan16E-010 secondary PMC carrier module. The primary PMCspan interfaces to the VME processor module via the PCI expansion connector. The expansion connector on the secondary bus supports the secondary PMCspan. The PCI-to-PCI bridge chip on the PMCspan provides the interface between the primary PCI bus and the secondary PCI bus.

The next figure shows a block diagram of the PMCspan's architecture.



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Figure 1-3. VME Processor/PMCspan System Diagram

Electrical Requirements

The voltage and current requirements for the PMCspan are as follows:

+5V 290 mA typical

440 mA maximum

+12V None

-12V None

Product Reliability (MTBF)

The reliability for the PMCspan is 75,000 hours MTBF.

Introduction

The following sections discuss the installation of the PMCspan modules and PMC modules. The following installation procedures are provided:

- ❑ PMC module on a PMCspan
- ❑ PMCspanX6E-002 Primary PMC Carrier Module on a MVME5100 or MVME5500 VME processor module
- ❑ PMCspanX6E-010 Secondary PMC Carrier Module on a PMCspanX6E-002 Primary PMC Carrier Module

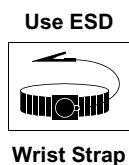
Refer to the installation instructions in VME processor module's installation and use manual before proceeding with these instructions.

Packaging

The PMCspan is packed in an anti-static package to protect it from any static discharge. Observe standard handling practices of static sensitive equipment.

Note Each PMCspan ships with a standoff hardware kit for attaching the primary PMCspan to the VME processor module and the secondary PMCspan to the primary PMCspan.

ESD Precautions



Emerson strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to electrostatic discharge (ESD). After removing the component from its protective wrapper or from the system, place the component flat on a grounded, static-free surface (and, in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores) that is attached to an active electrical ground. Note that a system chassis may not be grounded if it is unplugged.

Installing PMC Modules

PCI mezzanine card (PMC) modules mount on the PMCspan. Install the PMC modules on the PMCspan prior to installing the PMCspan onto the VME processor module. The PMCspan is keyed to accept only +5V PMC modules. Refer to the installation instructions that come with the PMC for any prerequisites.



Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

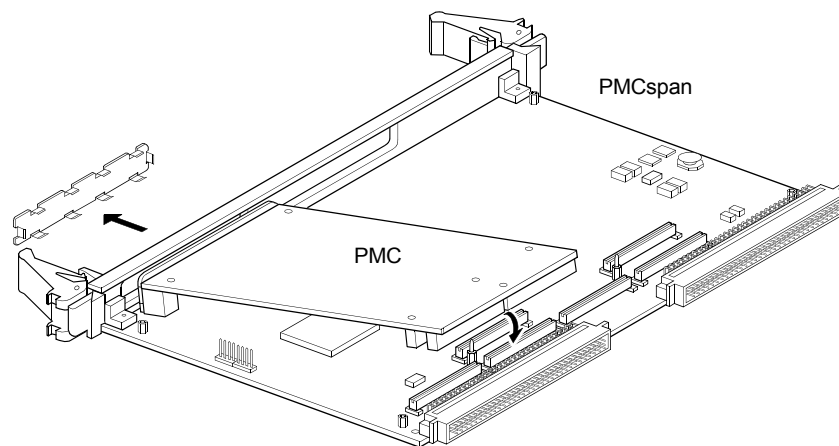


Inserting or removing modules with power applied may result in damage to module components. Avoid touching areas of integrated circuitry, static discharge can damage these circuits.

Note This procedure assumes that you have read the user's manual that was furnished with your VME module and that you have properly configured your according to the information in the MVME5100 or MVME5500 Installation and Use manuals. Refer to the list of documentation in [Appendix A, Related Documentation](#).

To install a PMC module on your PMCspan, perform the following steps while referring to the figure on the next page.

1. Position the PMCspan with the P1 and P2 connectors facing you.
2. Remove the PMC slot filler panel from the PMCspan front panel.



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Figure 2-1. PMC (Expansion) Module Placement on PMCspan

3. Slide the PMC module port connector into the PMC slot opening on the PMCspan front panel.

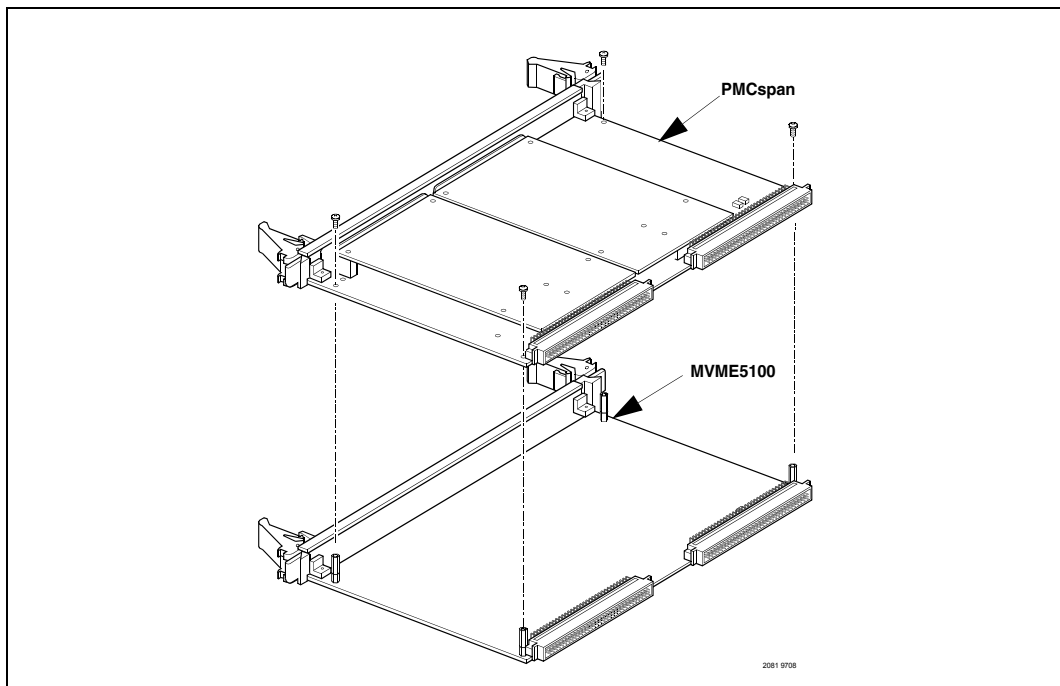
4. Align the PMC module over the PMCspan.
 - Align the connectors on the underside of the PMC module with the corresponding connectors (J11, J12, and J14) on the PMCspan.
 - Align the keying hole on the PMC module with the keying pin on the PMCspan.
5. Gently press the PMC onto the PMCspan.
 - Turn the PMCspan component-side down.
6. Insert the four short Phillips screws supplied with the PMC module through the holes on the underside of the PMCspan, into the standoffs at the corners of the PMC module (note that some PMCs take a screw at each corner; others require only two screws at the forward corners). Tighten the screws.

Installing a PMCspan

PMCspanX6E-002

The PMCspanx6E-002 mounts onto an MVME51005E or MVME55006E series processor module. To upgrade or install a PMCspan, refer to the next figure and proceed as follows.

Figure 2-2. Typical PMC Module Placement on a VME Module



Primary PMCspan

To install a PMCspan module on your VME module, perform the following steps while referring to the figure on the next page:



Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.



Inserting or removing modules with power applied may result in damage to module components. Avoid touching areas of integrated circuitry, static discharge can damage these circuits.

Note This procedure assumes that you have read the user's manual that was furnished with your VME module and that you have properly configured your board according to the information in the MVME5100 or MVME5500 Installation and Use manuals. Refer to the list of documentation in [Appendix A, Related Documentation](#).

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to an electrical ground. Note that the system chassis may not be grounded if it is unplugged. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the VME modules.
3. If the VME module has already been installed in a VMEbus card slot, carefully remove it and place it with connectors P1 and P2 facing you.
4. Attach the four standoffs to the VME module. For each standoff:
 - Insert the threaded end into the standoff hole at each corner of the VME module
 - Thread the locking nuts into the standoff tips and tighten
5. Place the PMCspan on top of the VME module. Align the mounting holes in each corner to the standoffs and align PMCspan connector P4 with MVME5100 connector J25, or connector J4 on the MVME5500.
6. Gently press the PMCspan and VME module together and verify that the connectors are fully seated.
7. Insert four short screws (Phillips type) through the holes at the corners of the PMCspan and into the standoffs on the VME module. Tighten screws securely.

Secondary PMCspan

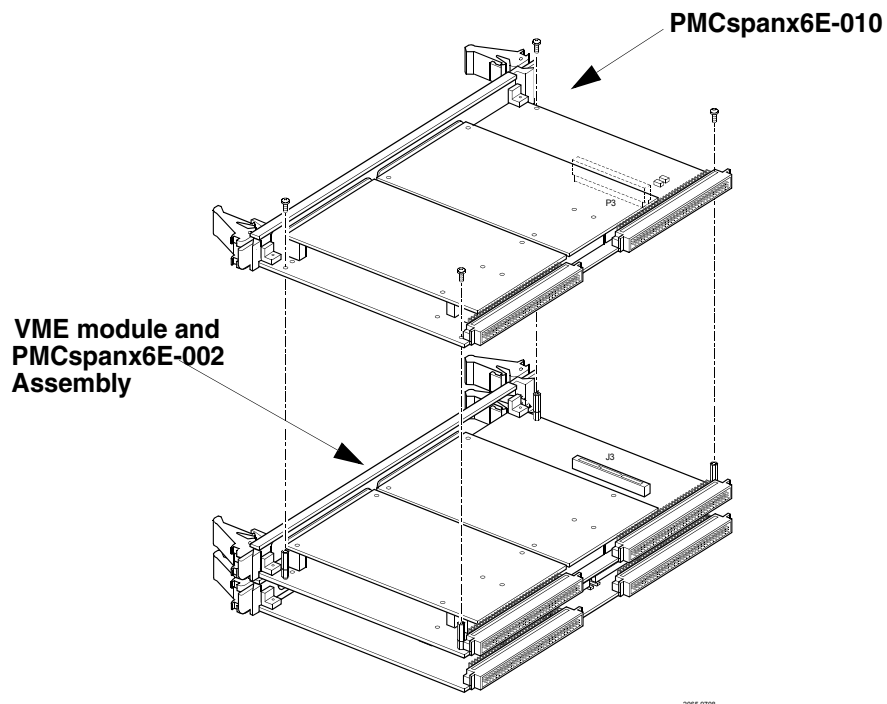
The secondary PMCspan mounts on top of a primary PMCspan module. To install on your VME module, perform the following steps while referring to the figure on the next page:



Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.



Inserting or removing modules with power applied may result in damage to module components. Avoid touching areas of integrated circuitry, static discharge can damage these circuits.



1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to an electrical ground. Note that the system chassis may not be grounded if it is unplugged. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. Remove chassis or system cover(s) as necessary for access to the VME module.
3. If the primary PMC Carrier Module and VME module assembly is already installed in the VME chassis, carefully remove it and place it with connectors P1 and P2 facing you.
4. Remove four screws (Phillips type) from the standoffs in each corner of the primary PCI expansion module.

5. Attach the four standoffs from the secondary PMCspan mounting kit to the primary PMCspan by screwing the threaded male portion of the standoffs in the locations where the screws were removed in the previous step.
6. Place the secondary PMCspan on top of the primary PMCspan. Align the mounting holes in each corner to the standoffs and align the secondary PMCspan connector P3 with primary PMCspan connector J3.
7. Gently press the two PMCspan modules together and verify that P3 is fully seated in J3.
8. Insert the four screws (Phillips type) through the holes at the corners of the secondary PMCspan and into the standoffs on the primary PMCspan. Tighten screws securely.

Note The screws have two different head diameters. Use the screws with the smaller heads on the standoffs next to VMEbus connectors P1 and P2.

Introduction

This chapter describes the physical and electrical structure of the PMCspan. [Figure 3-1](#) and [Figure 3-2](#) show the detailed block diagrams of the PMCspan and its primary interfaces.

PMC module I/O is available through the PMCspan front panel opening (for PMC modules with front panel connectors) or through the PMCspan VMEbus P2 backplane connector.

PCI-to-PCI Bridge Chip

The primary component on the PMCspan is the PCI6150 PCI-to-PCI bridge chip. This device provides the interface between the primary PCI bus (processor side), and the secondary PCI bus, which provides the interface to the PMC module. The bridge chip connects to the VMEbus processor module PCI bus through the PCI Expansion connector. The secondary PCI bus connects to each of the PCM slots and a an optional secondary expansion connector. For a detailed description of the PCI6150 chip, refer to the data book listed in [Appendix A, Related Documentation](#).

The PCI6150 PCI-to-PCI Bridge chip supports a 32-bit primary bus interface and a 32-bit secondary bus interface. This chip provides full support for delayed transactions which enables the buffering of memory read, I/O, and configuration transactions. It supports buffering of simultaneous multiple posted write and delayed transactions in both directions.

The PCI6150 has clock and arbitration pins to support PCI bus masters on the secondary bus. These are used to provide clocks an bus arbitration for the PMC module. The PCI6150 supports concurrent operation on the primary and secondary PCI busses providing traffic isolation between the primary and secondary busses.

Figure 3-1. PMCspanx6E-002 Block Diagram

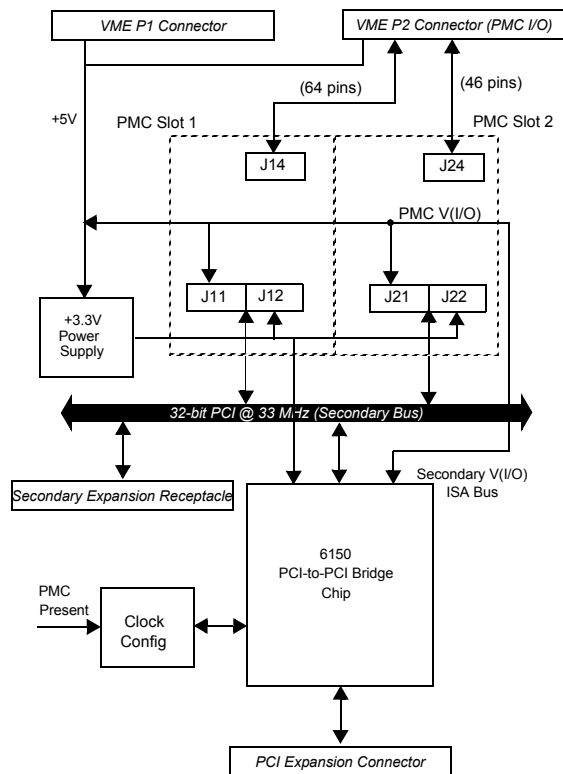
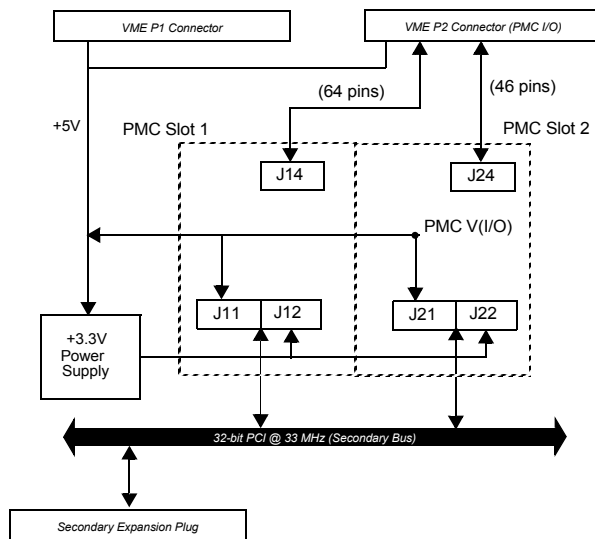


Figure 3-2. PMCspanx6E-010 Block Diagram



On-Board +3.3 Volt Power Supply

The on-board PMCspan power supply circuit generates the +3.3 volts used by the PCI-to-PCI bridge chip. The PCI-to-PCI bridge consumes 400 mA maximum, leaving 4.6 Amps available to the PMC modules. On the PMCspanx6E-010, 5 Amps is available to the PMC modules.

PMC Interface

Each PMC slot has three EIA E700 AAAB connectors for a 32-bit PMC interface to secondary PCI bus and user specific I/O. The PMCspan VME backplane connector P2 provides 64 I/O signals for PMC 1, and 46 P2 I/O signals for PMC 2. Refer to [Chapter 5, Connectors](#), for the pin signal assignments.

PCI Expansion

The PCI expansion interface is provided by a 114-pin plug connector (P4 or P5) on the secondary side of the PMCspan. This mates to the PCI Expansion connector on the VME processor module. Refer to Chapter [Chapter 5, Connectors](#), for the pin signal assignments.

The IDSEL for the PCI6150 chip is connected to AD20 on the PMCspan. Therefore the PCI6150 Device Number on the primary PCI bus is 1_0100b.

Secondary Expansion

Secondary PCI bus expansion is provided by a 114-pin receptacle connector, J3, on the primary side of the PMCspan16E-002. This mates to a 114-pin plug connector, P3, mounted on the secondary side of the PMCspan26E-010. Refer to [Chapter 5, Connectors](#) for the pin signal assignments.

Clock Configuration

The PCI6150 PCI-to-PCI Bridge chip will access the Clock Configuration logic following a primary PCI bus reset. The PCI6150 will automatically enable the PCI clock for all four PMC slots.

PMC Present Signals

The PMC PRESENT signal (BUSMODE1#) from each of the PMC modules (up to four) may be read any time following a reset through the General Purpose I/O interface in the PCI6150. Refer to [PMC Present Signal Assignment on page 25](#).

Front Panel LEDs

There are two green LEDs located on the front panel of the PMCspan, one for each PMC module. Both LEDs will be illuminated during reset. An individual LED will be illuminated whenever a PMC module has been granted bus mastership of the secondary PCI bus.

PMC Performance

All PMCspan models support 32-bit PCI operations at 33 MHz on the PMC (secondary) side. The PMCspan16E-002 primary carrier module supports 32-bit PCI operations on the processor (primary) side. Refer to the PCI6150 data book, listed in [Appendix A, Related Documentation](#) for PCI transaction timing information across the bridge.

Writes to the PCI bus are also posted by the Raven chip ASIC, so this section will focus mainly on read cycles. The read access latency for PMCspan-bound cycles initiated by 60X bus master consists of the following components:

- T_{start}** Start-up time (TS# to PCI bus Request).
T_{start} is 6 system clocks.
- T_{arb}** On-board PCI bus arbitration time.
- T_{ac}** On-board PCI access time (FRAME# to TRDY#).
- T_{lat}** Latency through PCI-to-PCI bridge.
- T_{delay}** Delay time from TRDY# on PCI to TA# on 60X bus. **T_{delay}** is 4 system clocks.

[Table 3-1](#) shows the access timings for various types of transfers initiated by a 60X system bus master to a PMCspan module.

Table 3-1. PowerPC 60x Bus to PMCspan PMC Access Timing

| Access Type | System Clock Periods Required for: | | | | Total Clocks |
|--|--|----------|----------|----------|--------------|
| | 1st Beat | 2nd Beat | 3rd Beat | 4th Beat | |
| 4-Beat Read (32-bit PCI Target) | 49 | 1 | 1 | 1 | 52 |
| 4-Beat Write (32-bit PCI Target) | 4 | 1 | 1 | 1 | 7 |
| 1-Beat Read (aligned, 4 bytes or less) | 38 | - | - | - | 38 |
| 1-Beat Write | 4 | - | - | - | 4 |
| Notes | Write cycles are posted by the Raven ASIC. Assumes no pipeline. Pipelined cycles would improve these numbers. T_{arb} is assumed to be 4 system clocks (2 PCI clocks). T_{ac} is assumed to be 6 system clocks (3 PCI clocks): Medium DEVSEL# target, zero wait PCI timing. | | | | |

Table 3-2 shows the ECC memory access latency for PMCspan-initiated cycles.

Table 3-2. PMCspan PMC to ECC Memory Access Timing

| Access Type | PCI Clock Periods Required for: | | | |
|---------------------|---------------------------------|----------|----------|------------------|
| | 1st Beat | 2nd Beat | 3rd Beat | <i>n</i> th Beat |
| 32-bit Burst Reads | 17 | 1 | 1 | 1 |
| 32-bit Burst Writes | 3 | 1 | 1 | 1 |
| 1-Beat Read | 17 | - | - | - |
| 1-Beat Write | 3 | - | - | - |

Notes

1. The latency assumes two system clocks for 60X system bus arbitration.
2. The latency is based on 60ns, fast-page DRAM timing. It is also assumed that L2 is either disabled or missed.
3. Write timings assume write posting FIFO is initially empty.

Introduction

This chapter describes the programming model for the PMCspan.

PLX PCI6150 Configuration Registers

The PCI Configuration Registers for the PLX PCI6150 PCI-to-PCI Bridge chip are shown in [Table 4-1](#). For a detailed register bit description, refer to the PLX PCI6150 data book listed in [Appendix A, Related Documentation](#).

Configuration Transactions

PCI configuration transactions are used to initialize the PCI system including the PCI-to-PCI bridge and devices on the PMC module. All PCI6150 registers are accessible only in the configuration space. In addition to accepting configuration transactions for initialization of its own configuration registers, the PCI6150 also forwards configuration transactions bound for devices on the PMC module, as well as special cycle generation on the secondary PCI bus. These two types of configuration transactions are supported by Type 0 and Type 1 configuration cycles.

Table 4-1. PLX PCI6150 PCI Configuration Register Address Mapping

| PCI Configuration Register Address | 31 | 24 | 23 | 16 | 15 | 8 | 7 | 0 | PC Writable | Serial EEPROM Writable | |
|------------------------------------|---|----|--------------|----|-----------------------|---|-----------------|---|-------------|------------------------|-----|
| 00h | Device ID (3388h) | | | | Vendor ID* | | | | | Yes | Yes |
| 04h | Primary Status | | | | Command | | | | | Yes | No |
| 08h | Class Code* | | | | | | Revision ID | | | Yes | Yes |
| 0Ch | Built-in Self Test* | | Header Type* | | Primary Latency Timer | | Cache Line Size | | Yes | Yes | |
| Notes: | <p>*Writable only when the Read-Only Register's Write Enable bit is set (RRC[7]=1;PCI:9Ch).</p> <p>Writes to Reserved locations have no effect.</p> <p>Reads of Reserved locations return zeros.</p> <p>To ensure software compatibility with other versions of the PCI 6150 family and to ensure future compatibility, write zeros to all unused bits..</p> <p>Refer to the individual register descriptions to determine which bits are writable.</p> | | | | | | | | | | |

Table 4-1. PLX PCI6150 PCI Configuration Register Address Mapping

| PCI Configuration Register Address | | | | | PC Writable | Serial EEPROM Writable | | | | |
|------------------------------------|---|----|------------------------------------|----|----------------------------------|------------------------|--|---|-----|-----|
| | 31 | 24 | 23 | 16 | 15 | 8 | 7 | 0 | | |
| 10h-17h | Reserved | | | | | | | | No | No |
| 18h | Secondary Latency Timer | | Subordinate Bus Number | | Secondary Bus Number | | Primary Bus Number | | Yes | No |
| 1Ch | Secondary Status | | | | I/O Limit | | I/O Base | | Yes | No |
| 20h | Memory Limit | | | | Memory Base | | | | Yes | No |
| 24h | Prefetchable Memory Limit | | | | Prefetchable Memory Base | | | | Yes | No |
| 28h | Prefetchable Memory Base Upper 32 Bits | | | | | | | | Yes | No |
| 2Ch | Prefetchable Memory Limit Upper 32 Bits | | | | | | | | Yes | No |
| 30h | I/O Limit Upper 16 Bits | | | | I/O Base Upper 16 Bits | | | | Yes | No |
| 34h | Reserved | | | | | | New Capability Pointer (DCh if Power Management Support; otherwise, E4h) | | No | No |
| 38h | Reserved | | | | | | | | No | No |
| 3Ch | Bridge Control | | | | Interrupt Pin | | Reserved | | Yes | No |
| 40h | Arbiter Control | | | | Diagnostic Control | | Chip Control | | Yes | No |
| 44h | Miscellaneous Options | | | | Timeout Control | | Primary Flow-through Control | | Yes | Yes |
| 48h | Secondary Incremental Prefetch Count | | Primary Incremental Prefetch Count | | Secondary Prefetch LineCount | | Primary Prefetch Line Count | | Yes | Yes |
| 4Ch | Reserved | | Secondary Flow-through Control | | Secondary Maximum Prefetch Count | | Primary Maximum Prefetch Count | | Yes | Yes |
| 50h | Reserved | | Test | | Internal Arbiter Control | | | | Yes | No |

Notes: *Writable only when the Read-Only Register's Write Enable bit is set (RRC[7]=1;PCI:9Ch).
Writes to Reserved locations have no effect.
Reads of Reserved locations return zeros.
To ensure software compatibility with other versions of the PCI 6150 family and to ensure future compatibility, write zeros to all unused bits..
Refer to the individual register descriptions to determine which bits are writable.

Table 4-1. PLX PCI6150 PCI Configuration Register Address Mapping

| PCI Configuration Register Address | 31 | 24 | 23 | 16 | 15 | 8 | 7 | 0 | PC Writable | Serial EEPROM Writable |
|------------------------------------|--|----------------------------------|------------------------------|--|--|--------------------------------------|--------------------------------------|-----|-------------|------------------------|
| 54h | Serial EEPROM Data | | | Serial EEPROM Address | | Serial EEPROM Control | | | Yes | No |
| 58h-63h | Reserved | | | | | | | | No | No |
| 64h | GPIO [3:0] Input Data | | GPIO [3:0] Output Enable | | GPIO [3:0] Output Data | | P_SERR# Event Disable | | Yes | No |
| 68h | Reserved | | P_SERR# Status | | Secondary Clock Control | | | Yes | No | |
| 6Ch-96h | Reserved | | | | | | | | No | No |
| 9Ch | Reserved | | | | | | Read Only Register Control | | Yes | No |
| A0h-D8h | Reserved | | | | | | | | Yes | No |
| DCh | Power Management Capabilities* | | | Power Management Next Capability Pointer (E4h) | | Power Management Capability ID (01h) | | | Yes | Yes |
| E0h | Power Management Data* | PMCSR Bridge Supports Extensions | | Power Management Control/Status* | | | | | Yes | Yes |
| E4h | Reserved | | Hot Swap Control/Status (0h) | | Hot Swap Next Capability Pointer (E8h) | | Hot Swap Control (Capability ID) 06h | | Yes | No |
| E8h | VPD Address (0h) | | | VPD Next Capability Pointer (00h) | | VPD Capability ID (03h) | | | Yes | No |
| ECh | VPD Data (0h) | | | | | | | | Yes | No |
| Notes: | <p>*Writable only when the Read-Only Register's Write Enable bit is set (RRC[7]=1;PCI:9Ch).</p> <p>Writes to Reserved locations have no effect.</p> <p>Reads of Reserved locations return zeros.</p> <p>To ensure software compatibility with other versions of the PCI 6150 family and to ensure future compantibility, write zeros to all unused bits..</p> <p>Refer to the individual register descriptions to determine which bits are writable.</p> | | | | | | | | | |

Table 4-2. Register 6-1 (PCIIDR; PCI:00h) PCI Configuration ID

| Bit | Description | Read | Write | Value after Reset |
|-------|---|------|---------------------------------|-------------------|
| 15:0 | Vendor ID, identifies PCI6150 manufacturer. Defaults to the PCI-SIG-issued PLX Vendor ID (3388h) if a blank or no serial EEPROM is present. | Yes | Only if RRC[7]=1; Serial EEPROM | 3388h |
| 31:16 | Device ID. Identifies the particular device. Defaults to PLX PCI6150 part number (0022h) if a blank or no serial EEPROM is present | Yes | Only if RRC[7]=1; Serial EEPROM | 0022h |

Type 0 Configuration Cycles

Type 0 configuration cycles are issued to configure devices on the same bus as the initiator. The processor will access configuration registers within the PCI6150, issuing a Type 0 cycle on the primary PCI bus by programming the Raven CONADD Register for Bus Number 0, and Device Number 1_0100 (binary). The Function Code is ignored by the PCI6150 since it is a single-function device. The RAVEN chip will translate this configuration address to an IDSEL# on AD20, which is connected to the DEVSEL# on the PCI6150 on the PMCspan.

The PCI6150 limits all configuration register accesses to a single double word data transfer and returns a target disconnect with the first data transfer if additional data phases are requested. All bytes of the requested double word are returned, regardless of the PCI byte enable bits. Type 0 configuration transactions do not use the PCI6150 data buffers so these transactions are completed immediately regardless of the state of the data buffers.

The PCI6150 will ignore all Type 0 transactions initiated on the secondary PCI bus.

Type 1 Configuration Cycles

Type 1 configuration cycles are issued to configure PMC modules. The processor will access configuration registers within the PMC modules by issuing a Type 1 cycle on the primary PCI bus by programming the Raven CONADD Register for Bus Number \$01 (i.e., the Bus Number programmed into the Secondary Bus Number register), and the Device Number per [Table 4-3](#). The Function Code is dependent on the PMC modules.

The PCI6150 will perform a Type 1 to Type 0 translation when the Type 1 transaction generated on the primary bus is intended for a PMC module on the secondary bus. The PMC module can then respond to the Type 0 transaction.

The PCI6150 forwards Type 1 to Type 0 configuration transactions as delayed transactions which are limited to a single data transfer.

Table 4-3. Secondary Device Number to IDSEL Mapping

| Device Number (Hex) | Secondary AD (31:16) (Binary) | AD Bit Used as IDSEL# | Purpose |
|---------------------|--|-----------------------|--|
| 0-1 | 0000_0000_0000_0001 - 0000_0000_0000_0010 | - | Implemented by 6150 but not used |
| 2 | 0000_0000_0000_0100 | 18 | PMC 1 IDSEL# (Slot 1 on PMCspan16E-002) |
| 3 | 0000_0000_0000_1000 | 19 | PMC 2 IDSEL# (Slot 2 on PMCspan16E-002) |
| 4 | 0000_0000_0001_0000 | 20 | PMC 3 IDSEL# (Slot 1 on PMCspan26E-010) |
| 5 | 0000_0000_0010_0000 | 21 | PMC 4 IDSEL# (Slot 2 on PMCspan26E-010) |
| 6 - F | 0000_0000_0100_0000 - 1000_0000_0000_0000 | 22 - 31 | Implemented by 6150 but not used |
| 10 - 1E | 0000_0000_0000_0000 | None | Not implemented by PCI6150 |
| 1F | Special Cycle Data | - | Special Cycles for PMC |

Type 1 to Type 1 Forwarding

If the PCI6150 detects a Type 1 configuration transaction intended for a PCI bus downstream from the secondary bus (such as another PCI bus on a PMC module), the PCI6150 will forward the transaction unchanged to the secondary bus. This transaction will eventually get translated to a Type 0 transaction or a Special Cycle by a downstream PCI-to-PCI bridge.

Special Cycles

Special cycle transactions generated on the primary PCI bus are ignored by the PCI6150. However, Special Cycle commands can be sent to the PMC module using a Type 1 Configuration transaction. The PCI6150 will generate a Special Cycle on the secondary bus when it detects a Type 1 transaction on the primary bus with the following conditions:

- ❑ The lower two primary address bits AD(1:0) are 01 (binary)
- ❑ The device number in AD(15:11) is 1_1111 (binary)
- ❑ The function number in AD(10:8) is 111 (binary)
- ❑ The register number in AD(7:2) is 00_0000 (binary)
- ❑ The bus number in AD(23:16) is \$01 (the value in the Secondary Bus Number Register)
- ❑ The bus command on C/BE# is a configuration write command

The PCI6150 translates the Type 1 Configuration command to a Special Cycle and forwards the address and data unchanged. The transaction is forwarded as a delayed transaction but the target response is not forwarded back because Special Cycles result in a master abort. If more than one data transfer is requested during a Special Cycle, the PCI6150 responds with a target disconnect during the first data phase.

PMC Interrupts

The routing of interrupts from each PMC module is described in [Table 4-4](#).

Table 4-4. PMC Interrupt Routing

| Device on Secondary Bus (Hex) | Device (PMC module) Interrupt Pin | PCI Interrupt |
|-------------------------------|-----------------------------------|---------------|
| 02 (PMC 1) | INTA# | INTC# |
| | INTB# | INTD# |
| | INTC# | INTA# |
| | INTD# | INTB# |
| 03 (PMC 2) | INTA# | INTD# |
| | INTB# | INTA# |
| | INTC# | INTB# |
| | INTD# | INTC# |
| 04 (PMC 3) | INTA# | INTA# |
| | INTB# | INTB# |
| | INTC# | INTC# |
| | INTD# | INTD# |
| 05 (PMC 4) | INTA# | INTB# |
| | INTB# | INTC# |
| | INTC# | INTD# |
| | INTD# | INTA# |

PMC Clock, Request, Grant Assignment

The PCI6150 bridge chip provide individual clock sources and arbitration logic for each PMC module on the secondary PCI bus. The PMCspan routes the secondary PCI bus Clock, Request and Grant signals between the PCI6150 bridge chip and the PMC slots as shown in [Table 4-5](#).

Table 4-5. PMC Clock, Request, Grant Assignments

| PMC | 6150 Clock Source | 6150 Request | 6150 Grant |
|------------------------------|-------------------|--------------|------------|
| 1 (Slot 1 on PMCspan16E-002) | s_clk_o(0) | s_req_l(0) | s_gnt_l(0) |
| 2 (Slot 2 on PMCspan16E-002) | s_clk_o(1) | s_req_l(1) | s_gnt_l(1) |
| 3 (Slot 1 on PMCspan26E-010) | s_clk_o(2) | s_req_l(2) | s_gnt_l(2) |
| 4 (Slot 2 on PMCspan26E-010) | s_clk_o(3) | s_req_l(3) | s_gnt_l(3) |

PMC Present Signal Assignment

The PMCspan hardwires the BUSMODE(4:2)# encoding signals to 001 (binary) for each PMC slot indicating that the PMCspan supports PCI protocol. The signal BUSMODE1# returned from each PMC module indicates there is a PMC module installed in the slot and that the PMC module supports PCI protocol. The PMC Present signals from each PMC slot may be read at any time following a reset on the PCI6150 GPIO pins. [Table 4-6](#) shows the assignment of the PMC Present signals to the GPIO pins. [Figure 4-7](#) shows the values in the Serial Clock Mask register following a reset. Serial Clock Mask bit 13 is 0 in order to enable s_clk_o(9) for the 6150 s_clk input.

Table 4-6. PMC Present to GPIO Assignments

| PMC Present Signal | GPIO bit |
|------------------------------|----------|
| 1 (Slot 1 on PMCspan16E-002) | 0 |
| 2 (Slot 2 on PMCspan16E-002) | 1 |
| 3 (Slot 1 on PMCspan26E-010) | 2 |
| 4 (Slot 2 on PMCspan26E-010) | 3 |

Table 4-7. Serial Clock Mask

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Introduction

The PMCspan module connectors provide I/O and for interfaces to the VME processor modules and to other PMCspan modules. The pin assignments for the connectors PMCspan connections are provided in the following sections.

VMEbus Connectors (P1/P2)

The VMEbus P1 connector is a partially populated version of the 96-pin DIN type connector. The P1 Connector contains 23 pins and is used to provide +5V power to the PMCspan module. IACK and Bus Grant signals are passed through as required by the VME specification. The P2 VMEbus connector is a 5-row 160-pin connector and provides P2 I/O for the PMC modules.

The pin assignments for P1 and P2 are shown in Table 5-1 and 5.2.

Table 5-1. VME P1 Connector Pin Assignments

| Pin | ROW A | ROW B | ROW C | :in |
|-----|-------|----------|-------|-----|
| 1 | | | | 1 |
| 2 | | | | 2 |
| 3 | | | | 3 |
| 4 | | BG0IN_L | | 4 |
| 5 | | BG0OUT_L | | 5 |
| 6 | | BG1IN_L | | 6 |
| 7 | | BG1OUT_L | | 7 |
| 8 | | BG2IN_L | | 8 |
| 9 | GND | BG2OUT_L | GND | 9 |
| 10 | | BG3IN_L | | 10 |
| 11 | GND | BG3OUT_L | | 11 |
| 12 | | | | 12 |
| 13 | | | | 13 |
| 14 | | | | 14 |
| 15 | GND | | | 15 |
| 16 | | | | 16 |
| 17 | GND | | | 17 |
| 18 | | | | 18 |
| 19 | GND | | | 19 |

Table 5-1. VME P1 Connector Pin Assignments (continued)

| Pin | ROW A | ROW B | ROW C | :in |
|-----|-----------|-------|-------|-----|
| 20 | | GND | | 20 |
| 21 | IACKIN_L | | | 21 |
| 22 | IACKOUT_L | | | 22 |
| 23 | | GND | | 23 |
| 24 | | | | 24 |
| 25 | | | | 25 |
| 26 | | | | 26 |
| 27 | | | | 27 |
| 28 | | | | 28 |
| 29 | | | | 29 |
| 30 | | | | 30 |
| 31 | -12V | | +12V | 31 |
| 32 | +5.0V | +5.0V | +5.0V | 32 |

Table 5-2. VME P2 Connector Pin Assignments

| | ROW Z | ROW A | ROW B | ROW C | ROW D | |
|----|----------|----------|-------|----------|----------|----|
| 1 | PMC2IO2 | PMC1IO2 | +5.0V | PMC1IO1 | PMC2IO1 | 1 |
| 2 | GND | PMC1IO4 | GND | PMC1IO3 | PMC2IO3 | 2 |
| 3 | PMC2IO5 | PMC1IO6 | | PMC1IO5 | PMC2IO4 | 3 |
| 4 | GND | PMC1IO8 | | PMC1IO7 | PMC2IO6 | 4 |
| 5 | PMC2IO8 | PMC1IO10 | | PMC1IO9 | PMC2IO7 | 5 |
| 6 | GND | PMC1IO12 | | PMC1IO11 | PMC2IO9 | 6 |
| 7 | PMC2IO11 | PMC1IO14 | | PMC1IO13 | PMC2IO10 | 7 |
| 8 | GND | PMC1IO16 | | PMC1IO15 | PMC2IO12 | 8 |
| 9 | PMC2IO14 | PMC1IO18 | | PMC1IO17 | PMC2IO13 | 9 |
| 10 | GND | PMC1IO20 | | PMC1IO19 | PMC2IO15 | 10 |
| 11 | PMC2IO17 | PMC1IO22 | | PMC1IO21 | PMC2IO16 | 11 |
| 12 | GND | PMC1IO24 | GND | PMC1IO23 | PMC2IO18 | 12 |
| 13 | PMC2IO20 | PMC1IO26 | +5.0V | PMC1IO25 | PMC2IO19 | 13 |
| 14 | GND | PMC1IO28 | | PMC1IO27 | PMC2IO21 | 14 |
| 15 | PMC2IO23 | PMC1IO30 | | PMC1IO29 | PMC2IO22 | 15 |
| 16 | GND | PMC1IO32 | | PMC1IO31 | PMC2IO24 | 16 |
| 17 | PMC2IO26 | PMC1IO34 | | PMC1IO33 | PMC2IO25 | 17 |
| 18 | GND | PMC1IO36 | | PMC1IO35 | PMC2IO27 | 18 |
| 19 | PMC2IO29 | PMC1IO38 | | PMC1IO37 | PMC2IO28 | 19 |

Table 5-2. VME P2 Connector Pin Assignments (continued)

| | ROW Z | ROW A | ROW B | ROW C | ROW D | |
|----|----------|----------|-------|----------|------------|----|
| 20 | GND | PMC1IO40 | | PMC1IO39 | PMC2IO30 | 20 |
| 21 | PMC2IO32 | PMC1IO42 | | PMC1IO41 | PMC2IO31 | 21 |
| 22 | GND | PMC1IO44 | GND | PMC1IO43 | PMC2IO33 | 22 |
| 23 | PMC2IO35 | PMC1IO46 | | PMC1IO45 | PMC2IO34 | 23 |
| 24 | GND | PMC1IO48 | | PMC1IO47 | PMC2IO36 | 24 |
| 25 | PMC2IO38 | PMC1IO50 | | PMC1IO49 | PMC2IO37 | 25 |
| 26 | GND | PMC1IO52 | | PMC1IO51 | PMC2IO39 | 26 |
| 27 | PMC2IO41 | PMC1IO54 | | PMC1IO53 | PMC2IO40 | 27 |
| 28 | GND | PMC1IO56 | | PMC1IO55 | PMC2IO42 | 28 |
| 29 | PMC2IO44 | PMC1IO58 | | PMC1IO57 | PMC2IO43 | 29 |
| 30 | GND | PMC1IO60 | | PMC1IO59 | PMC2IO45 | 30 |
| 31 | PMC2IO46 | PMC1IO62 | GND | PMC1IO61 | GND | 31 |
| 32 | GND | PMC1IO64 | +5.0V | PMC1IO63 | No Connect | 32 |

PMC Slot Connectors (J11/J12/J14) (J21/J22/J24)

Each PMC slot has a set of three 64-pin connectors (EIA E700 AAAB) for connection to the 32-bit secondary PCI bus and for PMC I/O. The PMC Slot 1 connectors are as J11, J12 and J14; the PMC Slot 2 connectors are J21, J22 and J24.

All 64 I/O signals from PMC 1 (J14) are routed to P2, while only the first 46 I/O signals of PMC 2 (J24) are routed to P2. The pin assignments for these connectors are shown in the following tables.

Table 5-3. PMC J11 Connector Pin Assignments

| Pin | Signal | Signal | Pin |
|-----|-----------|-----------|-----|
| 1 | TCK | -12V | 2 |
| 3 | GND | PMCINTAD# | 4 |
| 5 | PMCINTBA# | PMCINTCB# | 6 |
| 7 | PMC13P# | +5.0V | 8 |
| 9 | PMCINTDC# | PCI-RSVD | 10 |
| 11 | GND | PCI-RSVD | 12 |
| 13 | PMC13CLK | GND | 14 |
| 15 | GND | PMC13GNT# | 16 |
| 17 | PMC13REQ# | +5.0v | 18 |
| 19 | V(I/O) | S_AD31 | 20 |
| 21 | S_AD28 | S_AD27 | 22 |

Table 5-3. PMC J11 Connector Pin Assignments

| Pin | Signal | Signal | Pin |
|-----|-----------|----------|-----|
| 23 | S_AD25 | GND | 24 |
| 25 | GND | S_C/BE3# | 26 |
| 27 | S_AD22 | S_AD21 | 28 |
| 29 | S_AD19 | +5.0V | 30 |
| 31 | V(I/O) | S_AD17 | 32 |
| 33 | S_FRAME# | GND | 34 |
| 35 | GND | S_IRDY# | 36 |
| 37 | S_DEVSEL# | +5.0V | 38 |
| 39 | GND | S_LOCK# | 40 |
| 41 | S_SDONE# | S_SBO# | 42 |
| 43 | S_PAR | GND | 44 |
| 45 | V(I/O) | S_AD15 | 46 |
| 47 | S_AD12 | S_AD11 | 48 |
| 49 | S_AD9 | +5.0V | 50 |
| 51 | GND | S_C/BE0# | 52 |
| 53 | S_AD6 | S_AD5 | 54 |
| 55 | S_AD4 | GND | 56 |
| 57 | V(I/O) | S_AD3 | 58 |
| 59 | S_AD2 | S_AD1 | 60 |
| 61 | S_AD0 | +5.0V | 62 |
| 63 | GND | S_REQ64# | 64 |

Table 5-4. PMC J12 Connector Pin Assignments

| Pin | Signal | Signal | Pin |
|-----|-----------|----------------|-----|
| 1 | +12V | TRST# | 2 |
| 3 | TMS | PMC24TDI (TDO) | 4 |
| 5 | PMC13TDI | GND | 6 |
| 7 | GND | PCI-RSVD | 8 |
| 9 | PCI-RSVD | PCI-RSVD | 10 |
| 11 | BUSMODE2# | +3.3V | 12 |
| 13 | S_PCIRST# | BUSMODE3# | 14 |
| 15 | 3.3V | BUSMODE4# | 16 |
| 17 | PCI-RSVD | GND | 18 |
| 19 | S_AD30 | S_AD29 | 20 |
| 21 | GND | S_AD26 | 22 |

Table 5-4. PMC J12 Connector Pin Assignments (continued)

| Pin | Signal | Signal | Pin |
|-----|------------|----------|-----|
| 23 | S_AD24 | +3.3V | 24 |
| 25 | PMC13IDSEL | S_AD23 | 26 |
| 27 | +3.3V | S_AD20 | 28 |
| 29 | S_AD18 | GND | 30 |
| 31 | S_AD16 | S_C/BE2# | 32 |
| 33 | GND | PMC-RSVD | 34 |
| 35 | S_TRDY# | +3.3V | 36 |
| 37 | GND | S_STOP# | 38 |
| 39 | S_PERR# | GND | 40 |
| 41 | +3.3V | S_SERR# | 42 |
| 43 | S_C/BE1# | GND | 44 |
| 45 | S_AD14 | S_AD13 | 46 |
| 47 | GND | S_AD10 | 48 |
| 49 | S_AD8 | +3.3V | 50 |
| 51 | S_AD7 | PMC-RSVD | 52 |
| 53 | +3.3V | PMC-RSVD | 54 |
| 55 | PMC-RSVD | GND | 56 |
| 57 | PMC-RSVD | PMC-RSVD | 58 |
| 59 | GND | PMC-RSVD | 60 |
| 61 | S_ACK64# | +3.3V | 62 |
| 63 | GND | PMC-RSVD | 64 |

Table 5-5. PMC J14 Connector Pin Assignments

| Pin | Signal | Signal | Pin |
|-----|-----------|-----------|-----|
| 1 | PMC13IO1 | PMC13IO2 | 2 |
| 3 | PMC13IO3 | PMC13IO4 | 4 |
| 5 | PMC13IO5 | PMC13IO6 | 6 |
| 7 | PMC13IO7 | PMC13IO8 | 8 |
| 9 | PMC13IO9 | PMC13IO10 | 10 |
| 11 | PMC13IO11 | PMC13IO12 | 12 |
| 13 | PMC13IO13 | PMC13IO14 | 14 |
| 15 | PMC13IO15 | PMC13IO16 | 16 |
| 17 | PMC13IO17 | PMC13IO18 | 18 |
| 19 | PMC13IO19 | PMC13IO20 | 20 |
| 21 | PMC13IO21 | PMC13IO22 | 22 |

Table 5-5. PMC J14 Connector Pin Assignments (continued)

| Pin | Signal | Signal | Pin |
|-----|-----------|-----------|-----|
| 23 | PMC13IO23 | PMC13IO24 | 24 |
| 25 | PMC13IO25 | PMC13IO26 | 26 |
| 27 | PMC13IO27 | PMC13IO28 | 28 |
| 29 | PMC13IO29 | PMC13IO30 | 30 |
| 31 | PMC13IO31 | PMC13IO32 | 32 |
| 33 | PMC13IO33 | PMC13IO34 | 34 |
| 35 | PMC13IO35 | PMC13IO36 | 36 |
| 37 | PMC13IO37 | PMC13IO38 | 38 |
| 39 | PMC13IO39 | PMC13IO40 | 40 |
| 41 | PMC13IO41 | PMC13IO42 | 42 |
| 43 | PMC13IO43 | PMC13IO44 | 44 |
| 45 | PMC13IO45 | PMC13IO46 | 46 |
| 47 | PMC13IO47 | PMC13IO48 | 48 |
| 49 | PMC13IO49 | PMC13IO50 | 50 |
| 51 | PMC13IO51 | PMC13IO52 | 52 |
| 53 | PMC13IO53 | PMC13IO54 | 54 |
| 55 | PMC13IO55 | PMC13IO56 | 56 |
| 57 | PMC13IO57 | PMC13IO58 | 58 |
| 59 | PMC13IO59 | PMC13IO60 | 60 |
| 61 | PMC13IO61 | PMC13IO62 | 62 |
| 63 | PMC13IO63 | PMC13IO64 | 64 |

Table 5-6. PMC J21 Connector Pin Assignments

| Pin | Signal | Signal | Pin |
|-----|-----------|-----------|-----|
| 1 | TCK | -12V | 2 |
| 3 | GND | PMCINTBA# | 4 |
| 5 | PMCINTCB# | PMCINTDC# | 6 |
| 7 | PMC24P# | +5.0V | 8 |
| 9 | PMCINTAD# | PCI-RSVD | 10 |
| 11 | GND | PCI-RSVD | 12 |
| 13 | PMC24CLK | GND | 14 |
| 15 | GND | PMC24GNT# | 16 |
| 17 | PMC24REQ# | +5.0v | 18 |
| 19 | V(I/O) | S_AD31 | 20 |
| 21 | S_AD28 | S_AD27 | 22 |

Table 5-6. PMC J21 Connector Pin Assignments (continued)

| Pin | Signal | Signal | Pin |
|-----|-----------|----------|-----|
| 23 | S_AD25 | GND | 24 |
| 25 | GND | S_C/BE3# | 26 |
| 27 | S_AD22 | S_AD21 | 28 |
| 29 | S_AD19 | +5.0V | 30 |
| 31 | V(I/O) | S_AD17 | 32 |
| 33 | S_FRAME# | GND | 34 |
| 35 | GND | S_IRDY# | 36 |
| 37 | S_DEVSEL# | +5.0V | 38 |
| 39 | GND | S_LOCK# | 40 |
| 41 | S_SDONE# | S_SBO# | 42 |
| 43 | S_PAR | GND | 44 |
| 45 | V(I/O) | S_AD15 | 46 |
| 47 | S_AD12 | S_AD11 | 48 |
| 49 | S_AD9 | +5.0V | 50 |
| 51 | GND | S_C/BE0# | 52 |
| 53 | S_AD6 | S_AD5 | 54 |
| 55 | S_AD4 | GND | 56 |
| 57 | V(I/O) | S_AD3 | 58 |
| 59 | S_AD2 | S_AD1 | 60 |
| 61 | S_AD0 | +5.0V | 62 |
| 63 | GND | S_REQ64# | 64 |

Table 5-7. PMC J22 Connector Pin Assignments

| Pin | Signal | Signal | Pin |
|-----|----------------|---------------|-----|
| 1 | +12V | TRST# | 2 |
| 3 | TMS | PMC24TDO(TDO) | 4 |
| 5 | PMC24TDI (TDI) | GND | 6 |
| 7 | GND | PCI-RSVD | 8 |
| 9 | PCI-RSVD | PCI-RSVD | 10 |
| 11 | BUSMODE2# | +3.3V | 12 |
| 13 | S_PCIRST# | BUSMODE3# | 14 |
| 15 | 3.3V | BUSMODE4# | 16 |
| 17 | PCI-RSVD | GND | 18 |
| 19 | S_AD30 | S_AD29 | 20 |
| 21 | GND | S_AD26 | 22 |

Table 5-7. PMC J22 Connector Pin Assignments (continued)

| Pin | Signal | Signal | Pin |
|-----|------------|----------|-----|
| 23 | S_AD24 | +3.3V | 24 |
| 25 | PMC24IDSEL | S_AD23 | 26 |
| 27 | +3.3V | S_AD20 | 28 |
| 29 | S_AD18 | GND | 30 |
| 31 | S_AD16 | S_C/BE2# | 32 |
| 33 | GND | PMC-RSVD | 34 |
| 35 | S_TRDY# | +3.3V | 36 |
| 37 | GND | S_STOP# | 38 |
| 39 | S_PERR# | GND | 40 |
| 41 | +3.3V | S_SERR# | 42 |
| 43 | S_C/BE1# | GND | 44 |
| 45 | S_AD14 | S_AD13 | 46 |
| 47 | GND | S_AD10 | 48 |
| 49 | S_AD8 | +3.3V | 50 |
| 51 | S_AD7 | PMC-RSVD | 52 |
| 53 | +3.3V | PMC-RSVD | 54 |
| 55 | PMC-RSVD | GND | 56 |
| 57 | PMC-RSVD | PMC-RSVD | 58 |
| 59 | GND | PMC-RSVD | 60 |
| 61 | S_ACK64# | +3.3V | 62 |
| 63 | GND | PMC-RSVD | 64 |

Table 5-8. PMC J24 Connector Pin Assignments

| Pin | Signal | Signal | Pin |
|-----|------------|-----------|-----|
| 1 | PMC24IO1 | PMC24IO2 | 2 |
| 3 | PMC24IO3 | PMC24IO4 | 4 |
| 5 | PMC24IO5 | PMC24IO6 | 6 |
| 7 | PMC24IO7 | PMC24IO8 | 8 |
| 9 | PMC24IO9 | PMC24IO10 | 10 |
| 11 | PMC24IO11 | PMC24IO12 | 12 |
| 13 | PMC24IO13/ | PMC24IO14 | 14 |
| 15 | PMC24IO15 | PMC24IO16 | 16 |
| 17 | PMC24IO17 | PMC24IO18 | 18 |
| 19 | PMC24IO19 | PMC24IO20 | 20 |
| 21 | PMC24IO21 | PMC24IO22 | 22 |

Table 5-8. PMC J24 Connector Pin Assignments (continued)

| Pin | Signal | Signal | Pin |
|-----|-----------|-----------|-----|
| 23 | PMC24IO23 | PMC24IO24 | 24 |
| 25 | PMC24IO25 | PMC24IO26 | 26 |
| 27 | PMC24IO27 | PMC24IO28 | 28 |
| 29 | PMC24IO29 | PMC24IO30 | 30 |
| 31 | PMC24IO31 | PMC24IO32 | 32 |
| 33 | PMC24IO33 | PMC24IO34 | 34 |
| 35 | PMC24IO35 | PMC24IO36 | 36 |
| 37 | PMC24IO37 | PMC24IO38 | 38 |
| 39 | PMC24IO39 | PMC24IO40 | 40 |
| 41 | PMC24IO41 | PMC24IO42 | 42 |
| 43 | PMC24IO43 | PMC24IO44 | 44 |
| 45 | PMC24IO45 | PMC24IO46 | 46 |
| 47 | N/C | N/C | 48 |
| 49 | N/C | N/C | 50 |
| 51 | N/C | N/C | 52 |
| 53 | N/C | N/C | 54 |
| 55 | N/C | N/C | 56 |
| 57 | N/C | N/C | 58 |
| 59 | N/C | N/C | 60 |
| 61 | N/C | N/C | 62 |
| 63 | N/C | N/C | 64 |

PMCSpan16E-002 PCI Expansion Connector (P4/P5)

A 114-pin plug connector provides the interface to the VME processor module's PCI expansion bus. P4 on the PMCSpan16E-002 connects to J25 on the MVME5100 or MVME5500. The pin assignments for these connectors are shown in [Table 5-9](#).

Table 5-9. PMCSpan16E-002 P4/P5 Pin Assignments

| Pin | Signal | Signal | Pin | Pin |
|-----|--------------|--------|--------------|-----|
| 1 | 3.3V | GND | 3.3V | 2 |
| 3 | P_PCICLK | GND | INTA# | 4 |
| 5 | GND | GND | INTB# | 6 |
| 7 | PURST# | GND | INTC# | 8 |
| 9 | HRESET# | GND | INTD# | 10 |
| 11 | PCIXTDO(TDO) | GND | 6150TDI(TDI) | 12 |

Table 5-9. PMCspan16E-002 P4/P5 Pin Assignments (continued)

| Pin | Signal | Signal | Pin | Pin |
|-----|-----------|--------|-----------|-----|
| 13 | TMS | GND | TCK | 14 |
| 15 | TRST# | GND | PCIXP# | 16 |
| 17 | PCIXGNT# | GND | PCIXREQ# | 18 |
| 19 | | GND | -12 V | 20 |
| 21 | P_PERR# | GND | P_SERR# | 22 |
| 23 | P_LOCK# | GND | P_SDONE | 24 |
| 25 | P_DEVSEL# | GND | P_SBO# | 26 |
| 27 | GND | GND | GND | 28 |
| 29 | P_TRDY# | GND | P_IRDY# | 30 |
| 31 | P_STOP# | GND | P_FRAME# | 32 |
| 33 | GND | GND | GND | 34 |
| 35 | P_ACK64# | GND | Reserved | 36 |
| 37 | P_REQ64# | GND | Reserved | 38 |
| 39 | P_PAR | +5V | P_PCIRST# | 40 |
| 41 | P_C/BE1# | +5V | P_C/BE0# | 42 |
| 43 | P_C/BE3# | +5V | P_C/BE2# | 44 |
| 45 | P_AD1 | +5V | P_AD0 | 46 |
| 47 | P_AD3 | +5V | P_AD2 | 48 |
| 49 | P_AD5 | +5V | P_AD4 | 50 |
| 51 | P_AD7 | +5V | P_AD6 | 52 |
| 53 | P_AD9 | +5V | P_AD8 | 54 |
| 55 | P_AD11 | +5V | P_AD10 | 56 |
| 57 | P_AD13 | +5V | P_AD12 | 58 |
| 59 | P_AD15 | +5V | P_AD14 | 60 |
| 61 | P_AD17 | +5V | P_AD16 | 62 |
| 63 | P_AD19 | +5V | P_AD18 | 64 |
| 65 | P_AD21 | +5V | P_AD20 | 66 |
| 67 | P_AD23 | +5V | P_AD22 | 68 |
| 69 | P_AD25 | +5V | P_AD24 | 70 |
| 71 | P_AD27 | +5V | P_AD26 | 72 |
| 73 | P_AD29 | +5V | P_AD28 | 74 |
| 75 | P_AD31 | +5V | P_AD30 | 76 |
| 77 | P_PAR64 | GND | Reserved | 78 |
| 79 | P_C/BE5# | GND | P_C/BE4# | 80 |
| 81 | P_C/BE7# | GND | P_C/BE6# | 82 |

Table 5-9. PMCspan16E-002 P4/P5 Pin Assignments (continued)

| Pin | Signal | Signal | Pin | Pin |
|-----|--------|--------|--------|-----|
| 83 | P_AD33 | GND | P_AD32 | 84 |
| 85 | P_AD35 | GND | P_AD34 | 86 |
| 87 | P_AD37 | GND | P_AD36 | 88 |
| 89 | P_AD39 | GND | P_AD38 | 90 |
| 91 | P_AD41 | GND | P_AD40 | 92 |
| 93 | P_AD43 | GND | P_AD42 | 94 |
| 95 | P_AD45 | GND | P_AD44 | 96 |
| 97 | P_AD47 | GND | P_AD46 | 98 |
| 99 | P_AD49 | GND | P_AD48 | 100 |
| 101 | P_AD51 | GND | P_AD50 | 102 |
| 103 | P_AD53 | GND | P_AD52 | 104 |
| 105 | P_AD55 | GND | P_AD54 | 106 |
| 107 | P_AD57 | GND | P_AD56 | 108 |
| 109 | P_AD59 | GND | P_AD58 | 110 |
| 111 | P_AD61 | GND | P_AD60 | 112 |
| 113 | P_AD63 | GND | P_AD62 | 114 |

PMCspan16E-002 Secondary PCI Bus Connector (J3)

A 114-pin receptacle connector, J3, provides the secondary PCI bus expansion interface on the PMCspan16E-002. It connects to P3 on the PMCspan26E-010. The pin assignments for this connector are shown in [Table 5-10](#).

Table 5-10. PMCspan16E-002 J3 Pin Assignments

| Pin | Signal | Signal | Pin | Pin |
|-----|--------------|--------|--------------|-----|
| 1 | SCLK2ST | GND | PMC3P# | 2 |
| 3 | SCLK3ST | GND | INTA# | 4 |
| 5 | GND | GND | INTB# | 6 |
| 7 | Reserved | GND | INTC# | 8 |
| 9 | Reserved | GND | INTD# | 10 |
| 11 | PCIXTDO(TDO) | GND | PMC3TDI(TDI) | 12 |
| 13 | TMS | GND | TCK | 14 |
| 15 | TRST# | GND | PMC4P# | 16 |
| 17 | SGNT2# | GND | SREQ2# | 18 |
| 19 | SGNT3# | GND | SREQ3# | 20 |
| 21 | S_PERR# | GND | S_SERR# | 22 |

Table 5-10. PMCspan16E-002 J3 Pin Assignments (continued)

| Pin | Signal | Signal | Pin | Pin |
|-----|-----------|--------|-----------|-----|
| 23 | S_LOCK# | GND | S_SDONE | 24 |
| 25 | S_DEVSEL# | GND | S_SBO# | 26 |
| 27 | GND | GND | GND | 28 |
| 29 | S_TRDY# | GND | S_IRDY# | 30 |
| 31 | S_STOP# | GND | S_FRAME# | 32 |
| 33 | GND | GND | GND | 34 |
| 35 | S_ACK64# | GND | Reserved | 36 |
| 37 | S_REQ64# | +5V | Reserved | 38 |
| 39 | S_PAR | +5V | S_PCIRST# | 40 |
| 41 | S_C/BE1# | +5V | S_C/BE0# | 42 |
| 43 | S_C/BE3# | +5V | S_C/BE2# | 44 |
| 45 | S_AD1 | +5V | S_AD0 | 46 |
| 47 | S_AD3 | +5V | S_AD2 | 48 |
| 49 | S_AD5 | +5V | S_AD4 | 50 |
| 51 | S_AD7 | +5V | S_AD6 | 52 |
| 53 | S_AD9 | +5V | S_AD8 | 54 |
| 55 | S_AD11 | +5V | S_AD10 | 56 |
| 57 | S_AD13 | +5V | S_AD12 | 58 |
| 59 | S_AD15 | +5V | S_AD14 | 60 |
| 61 | S_AD17 | +5V | S_AD16 | 62 |
| 63 | S_AD19 | +5V | S_AD18 | 64 |
| 65 | S_AD21 | +5V | S_AD20 | 66 |
| 67 | S_AD23 | +5V | S_AD22 | 68 |
| 69 | S_AD25 | +5V | S_AD24 | 70 |
| 71 | S_AD27 | +5V | S_AD26 | 72 |
| 73 | S_AD29 | +5V | S_AD28 | 74 |
| 75 | S_AD31 | GND | S_AD30 | 76 |
| 77 | | GND | | 78 |
| 79 | | GND | | 80 |
| 81 | | GND | | 82 |
| 83 | | GND | | 84 |
| 85 | | GND | | 86 |
| 87 | | GND | | 88 |
| 89 | | GND | | 90 |
| 91 | | GND | | 92 |

Table 5-10. PMCspan16E-002 J3 Pin Assignments (continued)

| Pin | Signal | Signal | Pin | Pin |
|-----|--------|--------|-----|-----|
| 93 | | GND | | 94 |
| 95 | | GND | | 96 |
| 97 | | GND | | 98 |
| 99 | | GND | | 100 |
| 101 | | GND | | 102 |
| 103 | | GND | | 104 |
| 105 | | GND | | 106 |
| 107 | | GND | | 108 |
| 109 | | GND | | 110 |
| 111 | | GND | | 112 |
| 113 | | GND | | 114 |

PMCspan26E-010-010 PCI Bus Connector (P3)

A 114-pin receptacle connector, P3, provides the secondary PCI bus expansion interface for the PMCspan26E-010-010. It connects to J3 on the PMCspan16E-002. The pin assignments for this connector are shown in [Table 5-11](#).

Table 5-11. PMCspan26E-010 P3 Pin Assignments

| Pin | Signal | Signal | Pin | Pin |
|-----|------------|--------|------------|-----|
| 1 | PMC3CLK | GND | PMC13P# | 2 |
| 3 | PMC4CLK | GND | SXINTA# | 4 |
| 5 | GND | GND | SXINTB# | 6 |
| 7 | Reserved | GND | SXINTC# | 8 |
| 9 | Reserved | GND | SXINTD# | 10 |
| 11 | SXTDO(TDO) | GND | SXTDI(TDI) | 12 |
| 13 | TMS | GND | TCK | 14 |
| 15 | TRST# | GND | PMC24P# | 16 |
| 17 | PMC3GNT# | GND | PMC3REQ# | 18 |
| 19 | PMC4GNT# | GND | PMC4REQ# | 20 |
| 21 | S_PERR# | GND | S_SERR# | 22 |
| 23 | S_LOCK# | GND | S_SDONE | 24 |
| 25 | S_DEVSEL# | GND | S_SBO# | 26 |
| 27 | GND | GND | GND | 28 |
| 29 | S_TRDY# | GND | S_IRDY# | 30 |
| 31 | S_STOP# | GND | S_FRAME# | 32 |

Table 5-11. PMCspan26E-010 P3 Pin Assignments (continued)

| Pin | Signal | Signal | Pin | Pin |
|-----|----------|--------|-----------|-----|
| 33 | GND | GND | GND | 34 |
| 35 | S_ACK64# | GND | Reserved | 36 |
| 37 | S_REQ64# | GND | Reserved | 38 |
| 39 | S_PAR | +5V | S_PCIRST# | 40 |
| 41 | S_C/BE1# | +5V | S_C/BE0# | 42 |
| 43 | S_C/BE3# | +5V | S_C/BE2# | 44 |
| 45 | S_AD1 | +5V | S_AD0 | 46 |
| 47 | S_AD3 | +5V | S_AD2 | 48 |
| 49 | S_AD5 | +5V | S_AD4 | 50 |
| 51 | S_AD7 | +5V | S_AD6 | 52 |
| 53 | S_AD9 | +5V | S_AD8 | 54 |
| 55 | S_AD11 | +5V | S_AD10 | 56 |
| 57 | S_AD13 | +5V | S_AD12 | 58 |
| 59 | S_AD15 | +5V | S_AD14 | 60 |
| 61 | S_AD17 | +5V | S_AD16 | 62 |
| 63 | S_AD19 | +5V | S_AD18 | 64 |
| 65 | S_AD21 | +5V | S_AD20 | 66 |
| 67 | S_AD23 | +5V | S_AD22 | 68 |
| 69 | S_AD25 | +5V | S_AD24 | 70 |
| 71 | S_AD27 | +5V | S_AD26 | 72 |
| 73 | S_AD29 | +5V | S_AD28 | 74 |
| 75 | S_AD31 | +5V | S_AD30 | 76 |
| 77 | | GND | | 78 |
| 79 | | GND | | 80 |
| 81 | | GND | | 82 |
| 83 | | GND | | 84 |
| 85 | | GND | | 86 |
| 87 | | GND | | 88 |
| 89 | | GND | | 90 |
| 91 | | GND | | 92 |
| 93 | | GND | | 94 |
| 95 | | GND | | 96 |
| 97 | | GND | | 98 |
| 99 | | GND | | 100 |
| 101 | | GND | | 102 |

Table 5-11. PMCspan26E-010 P3 Pin Assignments (continued)

| Pin | Signal | Signal | Pin | Pin |
|-----|--------|--------|-----|-----|
| 103 | | GND | | 104 |
| 105 | | GND | | 106 |
| 107 | | GND | | 108 |
| 109 | | GND | | 110 |
| 111 | | GND | | 112 |
| 113 | | GND | | 114 |



Emerson Network Power - Embedded Computing Documents

The Emerson Network Power - Embedded Computing publications listed below are referenced in this manual. You can obtain electronic copies of Emerson Network Power - Embedded Computing publications by contacting your local Emerson sales office. For documentation of final released (GA) products, you can also visit the following website:

www.emersonnetworkpower.com/embeddedcomputing > Solution Services > Technical Documentation Search. This site provides the most up-to-date copies of Emerson Network Power - Embedded Computing product documentation.

Table A-1. Emerson Network Power - Embedded Computing Publications

| Document Title | Publication Number |
|---|--------------------|
| MVME51005E Single Board Computer Installation and Use | 6806800A38A |
| MVME55006E Single Board Computer Installation and Use | 6806800A37A |

Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table A-2. Related Publications

| Document Title | Publication Number |
|---|---------------------------------|
| PCI Special Interest Group | |
| PCI Local Bus Specification | Revision 2.1 10/21/94 |
| IEEE | |
| Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC | P1386.1/Draft 2.0 April 4, 1995 |
| Draft Standard for a Common Mezzanine Card Family: CMC | P1386/Draft 2.0 April 4, 1995 |
| PLX Technologies | |
| PCI6150 PCI-to-PCI Bridge Data Book | PCI6150BB_DB_V2.11 |

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