AMC-CAN4

4 Channel AMC CAN Module

High-Speed CAN at High Performance AMC Board

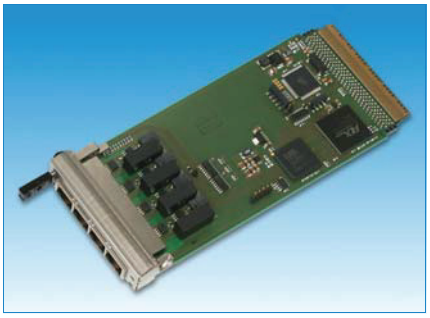
- *4 high-speed CAN interfaces according to ISO 11898-2*
- *High performance: local data management by FPGA and PCI Express® bus mastering*

Well-Proven Design at a Highly Integrated CAN Module

- *All CAN channels controlled by Advanced CAN Core (esdACC) controller implemented in a Xilinx® Spartan® 3e FPGA*
- *CAN interfaces via RJ45 sockets in the front panel, pin assignment acc. CiA® specification CiA 303-1*

Wide Software Support

- *Drivers for Windows®, Linux®, QNX® and other operating systems*



AMC CAN Interfaces

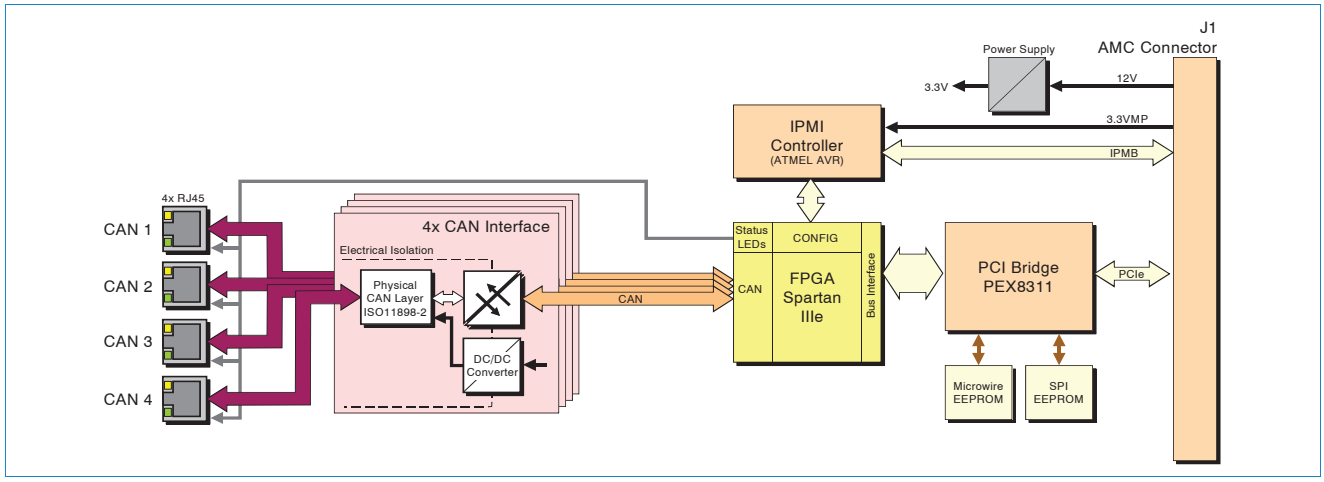
The AMC-CAN4 features four high-speed CAN interfaces according to ISO 11898-2. The CAN interfaces are electrically isolated against the controller potential and against each other. CAN status is displayed by two LEDs for each CAN channel placed at the RJ45 connectors.

CAN Data Management

The four independent CAN nets according to ISO 11898-1 are driven by the esd Advanced CAN Core (esdACC) CAN controller implemented in the Xilinx Spartan 3e FPGA. Controlled by the FPGA the AMC-CAN4 supports PCI bus mastering as an initiator, meaning that it is capable of initiating write cycles to the host CPU's RAM independent of the CPU or the system DMA controller. This results in a reduction of overall latency on servicing I/O transactions in particular at higher data rates.

Software Support

CAN layer 2 (CAN-API) software drivers are available for Windows, RTX, VxWorks®[1], QNX[1] and Linux[1]. Drivers for other operating systems are available on request.
The CANopen® software package is available for Windows, VxWorks[1], RTX[1], QNX[1] and Linux[1]. The J1939 software package is available for Windows, VxWorks[1], QNX[1] and Linux[1].



Technical Specifications:

MicroTCA®/AMC® standards:	
µTCA	*PICMG® MTCA.0 R1.0, PICMG® AMC.0 R2.0*
IPMI	*IPMI V1.5, controller Atmel® AVR*
Updates	*PICMG® HPM.1 R1.0*
PCIe bridge	*PCISIG® PCIe spec. R.1.0a*
CAN interfaces:	
CAN controller	*esdACC in FPGA Spartan 3e, acc. to ISO 11898-1 (CAN 2.0 A/B)*
Physical interface	*4x CAN high-speed interface acc. to ISO 11898-2, 1 Mbit/s, electrically isolated*
CAN connector	*4x RJ45, pin assignment acc. to CiA 303-1*
General :	
Dimensions	*Single mid-size AMC Module (73.5 x 180 mm)*
Ambient temp.	*0 ...+70 °C (free convection)*
Humidity	*Max. 90 %, non-condensing*
Power supply	*3.3 V ($I_{3.3VMPMAX}$= 70 mA), 12 V ($I_{12VTYPICAL}$ = 0.4 A, I_{12VMAX}= 0.5 A)*
Connectors	*J1: AMC B/B+ compatible (MicroTCA™)*
LEDs	*Blue (hot plug), red (IPMI), green (OK), 4x yellow and 4x green (CAN status)*

Order information:

Hardware		*Order No.*
AMC-CAN4	*4x CAN interface, ISO11898-2, incl. CAN layer 2 drivers for Windows and Linux on CD*	*U.1002.01*
AMC-CAN4-DSUB9-Adapter	*Adapter cable RJ45 to 9-pin DSUB male, 1.5 m, (4 are required per module)*	*U.1002.10*

Software Support

Additional CAN layer 2 object licences including CD-ROM[1]	
CAN-DRV-LCD QNX	*C.1101.32*
CAN-DRV-LCD RTX	*C.1101.35*
CAN-DRV-LCD VxWorks	*C.1101.55*
CANopen object licences and J1939 stacks including CD-ROM[1]:	
CANopen-LCD Windows/Linux	*C.1101.06*
CANopen-LCD QNX	*C.1101.17*
CANopen-LCD RTX	*C.1101.16*
CANopen-LCD VxWorks	*C.1101.18*
J1939 Stack for Windows (Object)	*C.1130.10*
J1939 Stack for Linux (Object)	*C.1130.11*

[1] *For detailed information about the driver availability of your special operating system please contact our sales team.*

esd electronic system design gmbh
Vahrenwalder Str. 207
30165 Hannover / Germany

Ph
Fax
Ema

Ehlbeek 15a
30938 Burgwedel
fon 05139-9980-0
fax 05139-9980-49

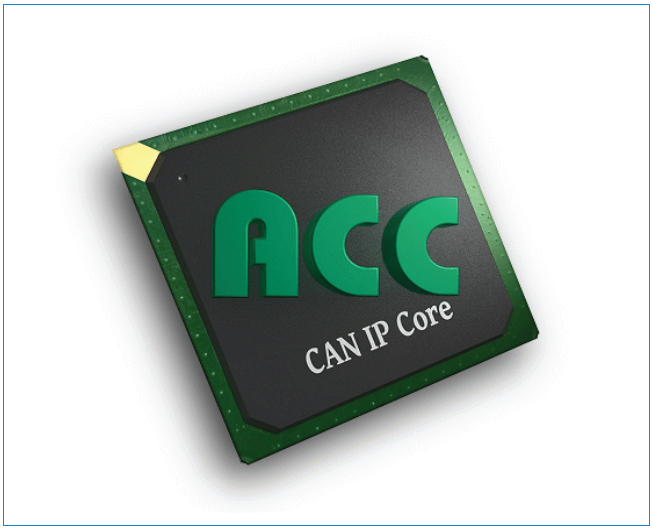
www.powerbridge.de
info@powerbridge.de

AMC-CAN4

Driven by esdACC (Advanced CAN Core)

Basic Product Features:

- CAN ISO 11898-1 protocol compatibility
- 11-bit and 29-bit CAN IDs
- Bit rates from 10kbit/s up to 1 Mbit/s supported
- Receive buffer (64 CAN messages)
- Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Single-shot transmission (no re-transmission)
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (software supported bit rate detection)
- Acceptance filter (4-byte code, 4-byte mask)
- Self reception mode (reception of 'own' messages)



Superior esdACC Features:

- Operating system independently programmable via esd's NTCAN-API
- 32-bit register interface optimized for CAN needs
  - Easy to program
  - Transmission and reception of CAN frames with a minimum of register accesses
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 20.833 ns)
  - On hardware with IRIG-B interfaces IRIG-B time is used for timestamping
- TX FIFO (8 CAN frames deep)
  - Providing the means to generate 100% busload even with non-realtime operating systems
  - Providing the means for real back-to-back transmission
- Frame accurate abortion of transmissions with minimum delay
  - e.g. for driver timeouts
  - ISO11898-1 conform
  - Aborted frames in FIFO won't be blocked by low priority TX
- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
- Optional integration with 32-bit microcontroller to further relieve host CPU
- Optional different sources for timestamps (e.g. IRIG-B)
- CAN error injection units
  - Simulating a wide range of error situations on CAN bus, e.g.:
    - ID pollution (100% bus load on certain CAN ID/priority)
    - Defective sensor (Destroying all CAN messages of a given CAN ID)
  - Different trigger modes
    - Bit pattern match
    - Time triggered
    - Immediate regarding CAN arbitration
    - External
  - 'Cross CAN bus triggering' (event on one CAN bus triggers event on another bus)
- Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
- The esdACC IP core has been verified on Xilinx Spartan and Altera Cyclone FPGAs.

Driver Availability:

Windows, Linux[1], QNX[1], VxWorks[1], RTX[1]

[1] For detailed information about the driver availability for your operating system and the particular esd CAN interface please contact our sales team.

Available higher level protocols:

CANopen, ARINC825, J1939

For further information on the esdACC IP Core please contact our sales team.

esd electronic system design gmbh
Vahrenwalder Str. 207
30165 Hannover / Germany

Phone: +49 (0) 511 3 72 98-0
Fax: +49 (0) 511 3 72 98-68
Email: info@esd.eu