IC-FEP-VPX3b

Xilinx Virtex®-6 3U VPX board with FMC Site

The **IC-FEP-VPX3b** is a VPX board, the first of our Front End Processing family based on a Xilinx Virtex®-6 FPGA, offering highest performances with low power consumption.

Designed for applications requiring a very high level of computing power in a compact 3U form factor, the **IC-FEP-VPX3b** board mixes the flexibility of a Virtex-6 FPGA with the VPX high bandwith serial interfaces.

A FMC mezzanine site enlarges the adaptability of the board to connect ADC, DAC, general IOs, video, sFPDP or additionnal FPGA FMC modules.

As part of our 3U VPX range, the **IC-FEP-VPX3b**, associated with our Intel® or Freescale SBCs and our XMC carrier supporting IOs boards, provides the ideal platform for radar, sonar, electronic warfare and other digital signal processing applications.

Description

The Virtex®-6 FPGAs used on the **IC-FEP-VPX3b** are built on a 40-nanometer (nm) process using third-generation Xilinx ASMBL architecture. Equipped with the Virtex®-6 SX315T (*others : LX315T, SX475T...please consult us*), the **IC-FEP-VPX3b** provides the high-performance logic, high-bandwidth I/O and powerful DSP resources claimed by the most computation-intensive systems.

The DDR3 memory supports a significant transfert data rate of up to 8 GB/s whereas the DDRII+ SRAM supports a throughput of up to 1600MB/s

The Fabric Links of the VPX backplane are connected to the FPGA GTX transveivers, allowing data rate of up to 6,5 Gbps (*), depending on the type of interface : PCIe (GEN2), Aurora... (SRIO available thanks to specific IP).
It is also possible to take advantage of the embedded 10/100/1000 MAC blocks to provide four Ethernet ports on the backplane.
The **IC-FEP-VPX3b** is compliant with several Module Profiles of the ***OpenVPX*** standard.

The Virtex®-6 FPGA is interfaced with its Mirror flash (local bitstreams storage) and a SPI flash (user parameters storage) through a Spartan®-6 FPGA (LX-45T).

The FMC site of the **IC-FEP-VPX3b** is compliant with the FPGA Mezzanine Card standard (VITA 57.1), allowing to install FMC modules provided by IC, third-party or developped by the customers. These mezzanine modules will authorize to systematically use the latest / best suited high resolution A/D components in regards of the needs.

Moreover, the FMC can be equiped with a IOs connector to route sixteen differential pairs from the FMC module directly to the P2 VPX connector.

(*) : FPGA -2 speed grade. 5Gbps for -1 speed grade

Main features

Processing Unit
- Xilinx virtex-6 XC6VSX315T (others on demand)
- Two banks of DDR3-800 : 40-bit wide, 1.25 GBytes each
- DDRII+ SRAM : 18-bit wide / 9 MBytes
- flash :
  - one NOR Flash eeprom (128 MBytes)
  - one SPI flash (16 MBytes)
- Spartan®-6 LX-45T (control Node)

VPX Interfaces
- Four 4-lanes Fabric ports (on P1)
  - 4 GTX x4 channel (Fat Pipes A, B, C & D) (one lane of Fat Pipe D can be used to feed the Spartan-6)
- General purpose IOs (on P2)
  - 16 differential pairs (from FPGA)
  - 16 differential pairs (from FMC IOs connector)
- GPIOs user-defined on P1

FMC interfaces
- 1 GTX x4 link
- 80 Differential pairs
- 4 reference clocks

Miscelaneous
- PIC µ-controller for System Management (per VITA 46.11)
- 4 leds
- 4 switches

Accessories
- Engineering kit : JTAG ports for FPGA direct configuration

The **IC-FEP-VPX3b** is a VPX 3U / 4HP 0.8" (1" on request) board compliant with 3U module definitions of the VITA 46.0 standard.

It is available in standard, rugged and conduction-cooled grades.

powerBridge Computer
Ehlbeek 15a
30938 Burgwedel
www.powerbridge.de
INTERFACE CONCEPT

IC-FEP-VPX3b

XILINX Virtex-6 3U VPX board with FMC site

On-board firmware

The **IC-FEP-VPX3b** hardware platform is compatible with the Xilinx development tools (ISE Design Suite, Platform cable...).

Interface Concept provides :
- ►VHDL code for system services (DDR3, DDRII+, PCIe, Aurora, IC FMC interfaces...) and Reference Designs (PCIe DMA Engine, Signal capture & processing...). Their implementation requires the Xilinx ISE Design Tools.Integration from Xilinx System Generator will be availble soon.
- ►host drivers for our CPU (Linux, VxWorks)

The customers implement their own realtime applications with the capability to integrate the existing openSource code or third-party IP cores.

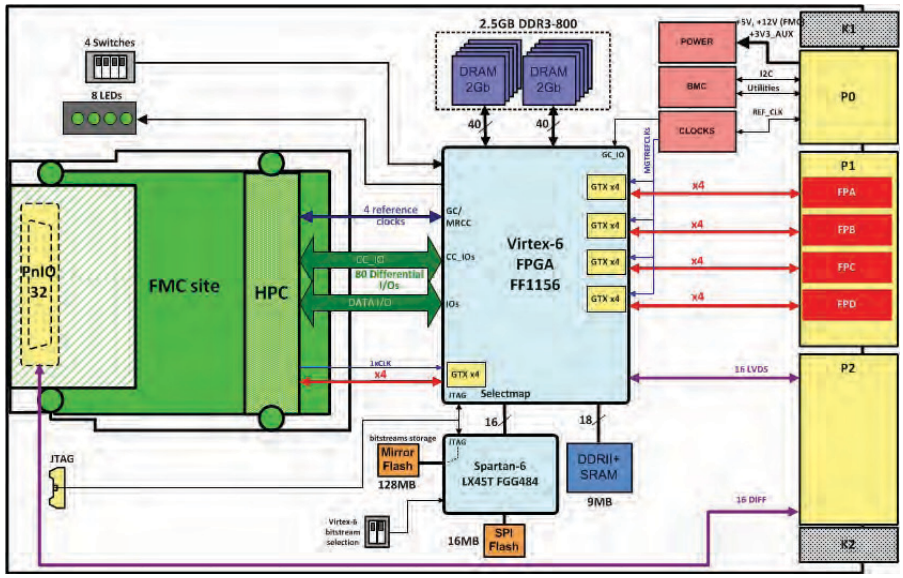
Interface features

P1 connector
- ►four 4-lanes Fabric ports
  - • four GTX x4 (ports A, B, C & D)
- ►GPIOs - user defined

P2 connector
- ►General purpose IOs (on P2)
  - • sixteen differential pairs
  - • sixteen differential pairs (from FMC IOs connector)

FMC connector
- ►one GTPx4 link
- ►80 differential pairs
- ►4 clocks (LVDS Diff)

Block Diagram



FMC modules

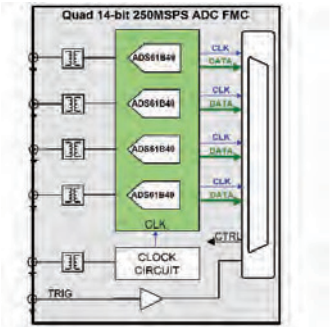
Interface Concept provides FMC modules.
Examples :

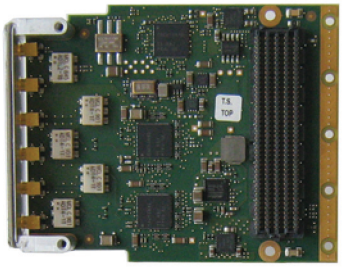
IC-ADC-FMCa :
►Quad 16-bit 135 Msps ADC

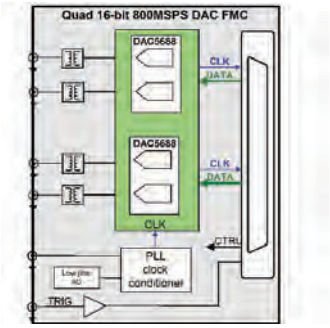
IC-ADC-FMCb :
►Quad 14-bit 250 Msps ADC

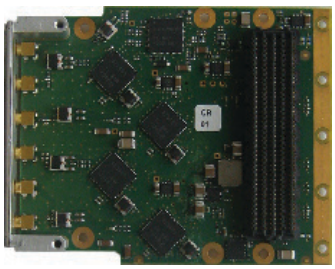
IC-DAC-FMCa :
►Quad 16-bit 800 Msps DAC

and IO FMC modules (Ethernet, SFP...)
Please consult us for technical details and availability.









Environnement Specifications:

Please consult the **IC-FEP-VPX3b** page at **www.interfaceconcept.com**.

Ordering Information:

Please contact our sales department : tel. **+33 (0)2 98 57 30 30** - email : **info@interfaceconcept.com**

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