NAMC-psTimer
Picosecond Timing AMC Module
Installation and Configuration Manual V1.3

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Note:

The release of the Installation and Configuration Manual is related to a certain HW board and SW revision given in the document title. For HW and SW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Manual release.

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*.
The following table gives a list of the abbreviations used in this document.

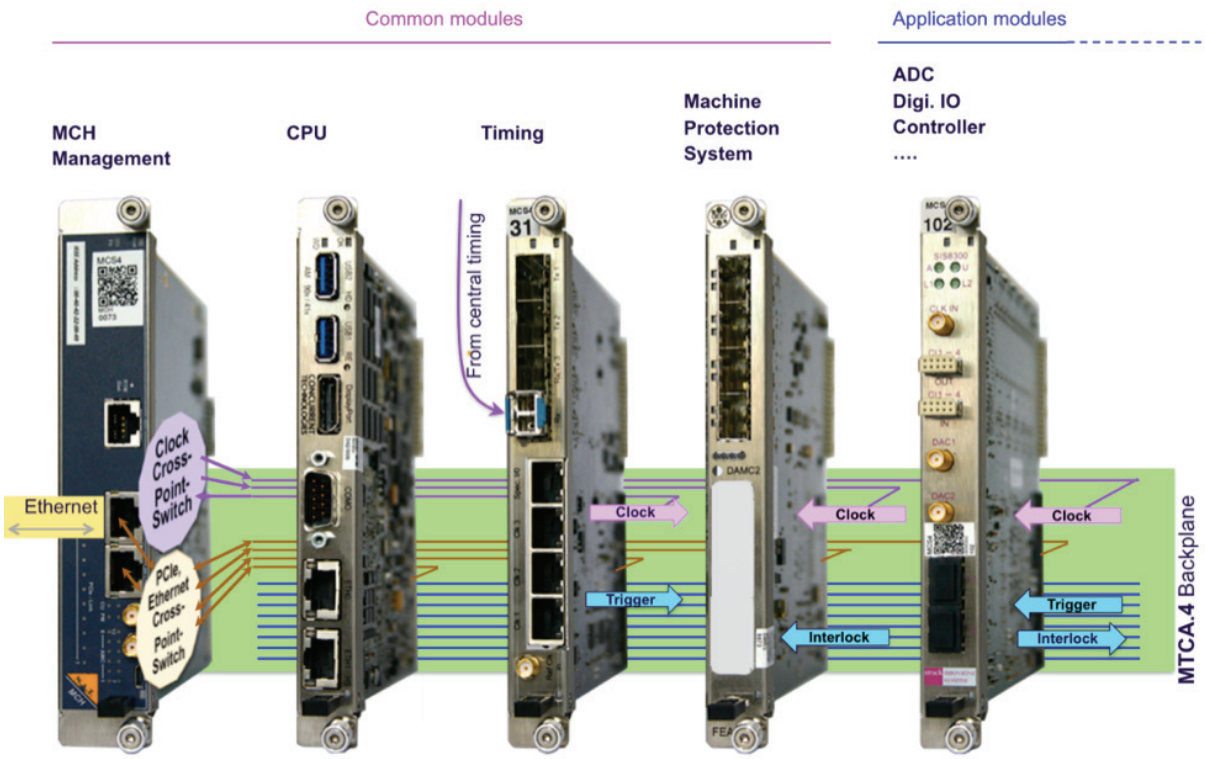
1. List of used abbreviations

Abbreviation	Description
AMC	Advanced Mezzanine Card
ATCA	Advanced Telecommunications Computing Architecture
FCLK	Fabric Clock
FPGA	Field Programmable Gate Array
I²C	Inter-Integrated Circuit
I/O	Input/Output
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
µTCA, MTCA, MicroTCA	Micro Telecommunications Computing Architecture
MUX	Multiplexing Unit
PCB	Printed Circuit Board
PHY	Physical Layer Device
SerDes	Serializer/Deserializer
SGMII	Serial GMII
SPI	Serial Peripheral Interface
PCIe	PCIexpress
x2Timer	former name of NAMC-psTimer
NAMC-psTimer	Timer with picosecond resolution in AMC form factor from N.A.T.

1. Introduction

NAMC-psTimer is an AMC based Fast Timing System with ps resolution.

The NAMC-psTimer is designed as timing systems for large installations such as the European XFEL (X-Ray Free Electron Laser) in Hamburg, Germany, but it can be used in a single stand-alone setup as well. Clocks and triggers are programmed and generated by a master module and distributed in a multi-star topology. All triggers within the entire timing system are synchronized with a jitter of approximately 10ps.



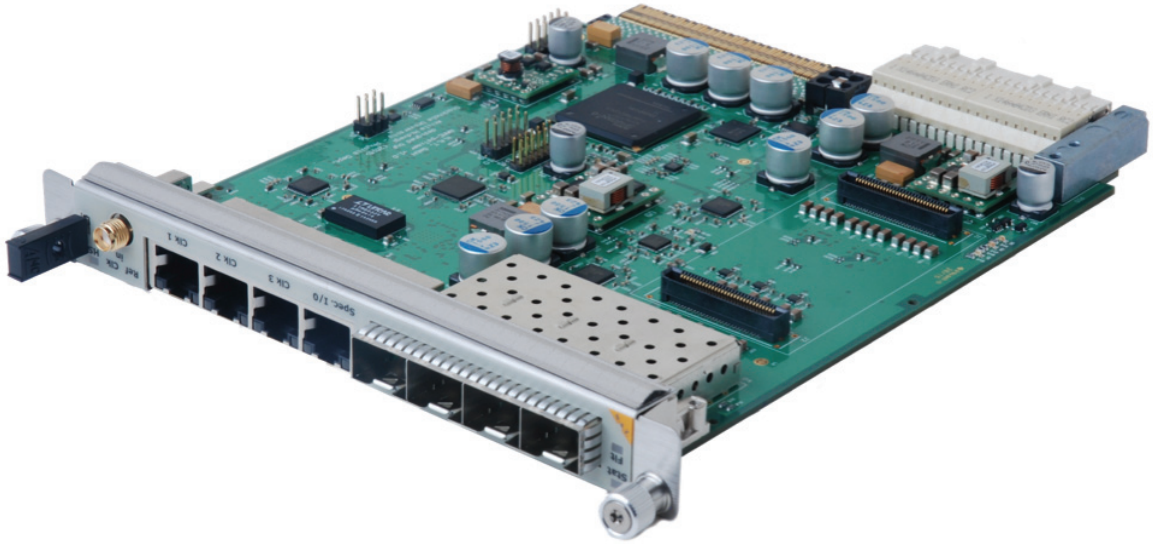
1. Figure: NAMC-psTimer use case of XFEL

In addition to the distribution of triggers and clocks the system is able to distribute data words and tables through its fiber distribution network. A precision 1.3GHz clock with modulated data is used on the fiber links. Receivers can recover both clock and data. Synchronized dividers are used to generate local clocks at the receivers. The receiver has 23 programmable outputs:

- Trigger with delay
- Immediate or delayed trigger events
- Gates between trigger events
- Slow clocks
- Two different slow data protocols
- Fast data protocol

1.1. NAMC-psTimer - Hardware Description

The NAMC-psTimer is a double width, mid-size AMC board for usage in the MicroTCA.4 architecture. Its main purpose is to output triggers and clock signals which may be based on local Stand-Alone configuration or information provided by a global timing system installation.



2. Figure: NAMC-psTimer – Product Photo

The NAMC-psTimer can work in transmittter, receiver and gateway mode and adapted to different timer requirements of master clocks and configurations.

The NAMC-psTimer provides up to six trigger and 3 clock signals at front panel.

The NAMC-psTimer can extend the number of output triggers and clock signals by adding one of the following Rear Transition Modules:

- NAMC-psTimer-RTM-C (copper)
  - with 9 Lemo connectors
  - in full production
-
- NAMC-psTimer-RTM-F (fiber)
  - with 9 SFP cages
  - full production will start depending on demand
-
- NAMC-psTimer-RTM-ST (ST connector)
  - currently only available from Desy

The former name of NAMC-psTimer was x2Timer. The name was changed to reflect the resolution of picosecond in the product name and the new manufacturer N.A.T. , who optimises continually the design for better productivity and signal quality.

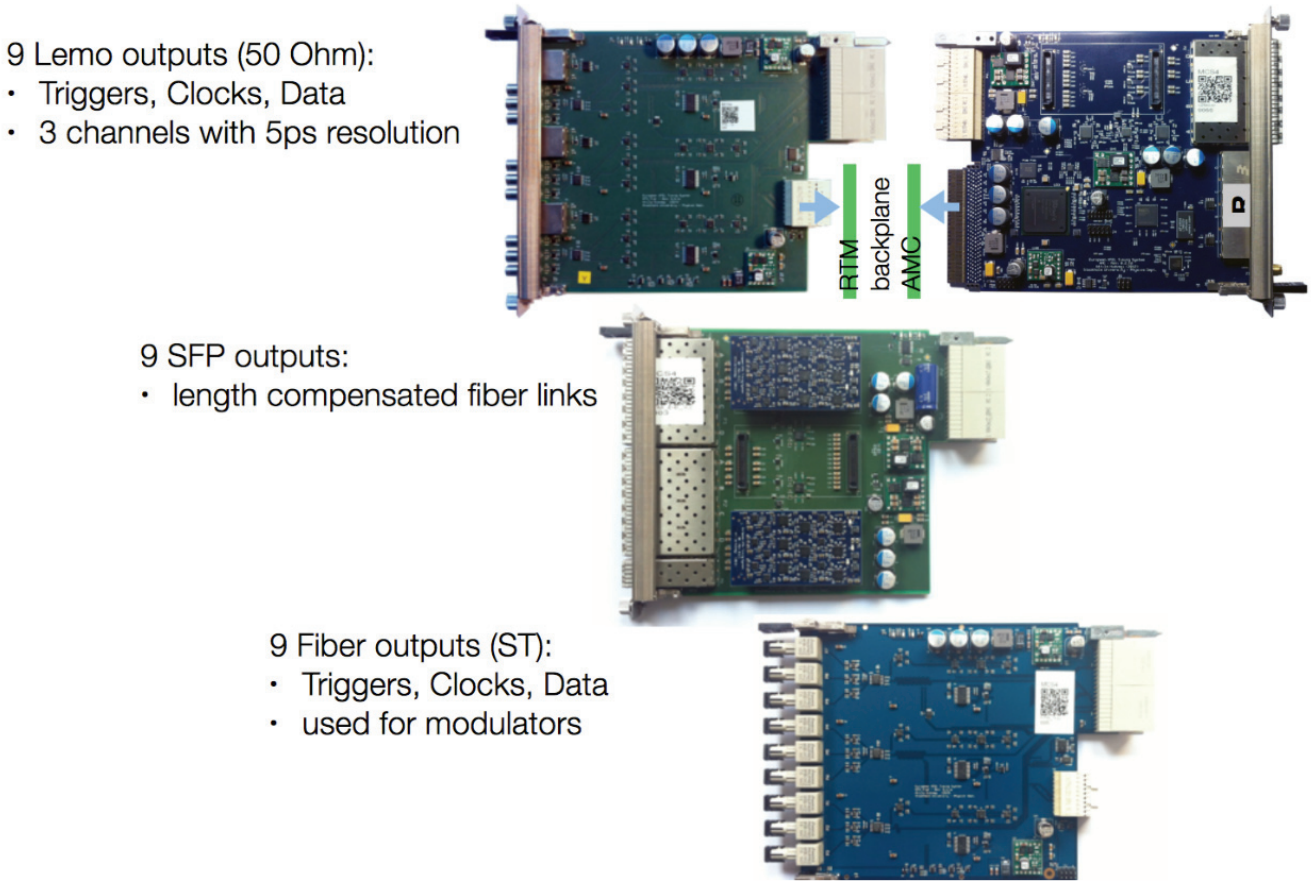
2. Overview

2.1. Major Features of NAMC-psTimer

- can be used as a transmitter or receiver or gateway module
- delivers precision clocks on TCLKA and TCLKB
- provides triggers, gates, clocks or data on M-LVDS ports 17 - 20
- 3x RJ45 outputs at front panel
  - with 2 triggers and one precision clock as LVDS signals
  - trigger position: 0 .. 160ms delay, 1ns resolution
  - trigger width: 0 .. 160ms, 10ns resolution
  - up to 255 trigger event numbers
  - precision clocks: 2.5 .. 650MHz
  - clock and trigger jitter: ~10ps RMS
- 4x SFP outputs at front panel
  - 3 transmitter channel implemented as piggy back module
    - NAMC-psTimer-P1
      - 3 channels without drift compensation
    - or NAMC-psTimer-P2
      - 3 channels with drift compensation
  - Out of the is three channels the 3rd channel can be configured as transmitter or receiver
  - 4th channel is configured as receiver

- Optional RTMs:
  - NAMC-psTimer-RTM-C (copper) with 9 Lemo connectors
  - NAMC-psTimer-RTM-F (fiber) with 9 SFP cages (optional drift compensation)
  - NAMC-psTimer-RTM-ST with 9 ST connectors

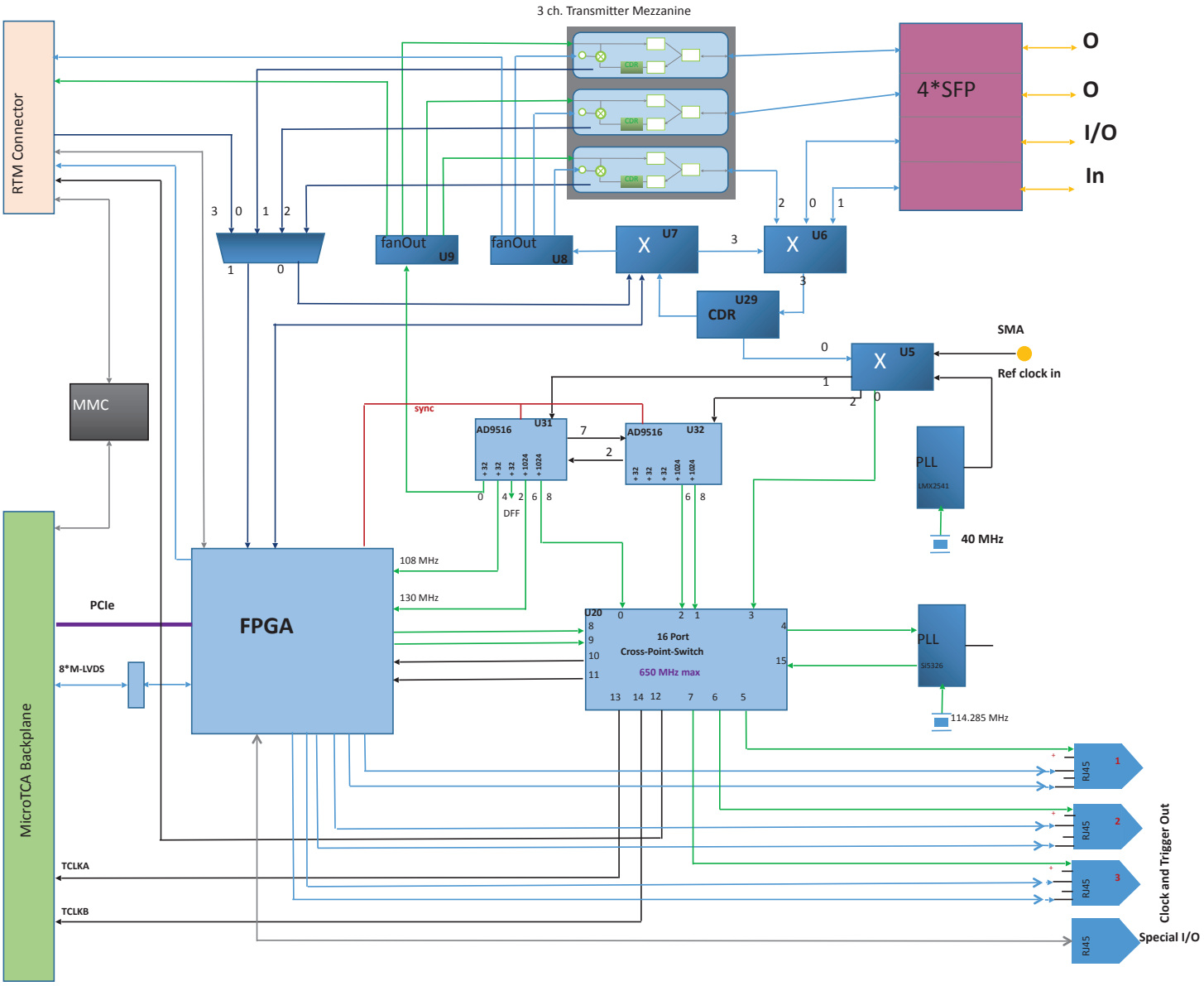
The figure 2 shows the NAMC-psTimer with the three RTM modules.



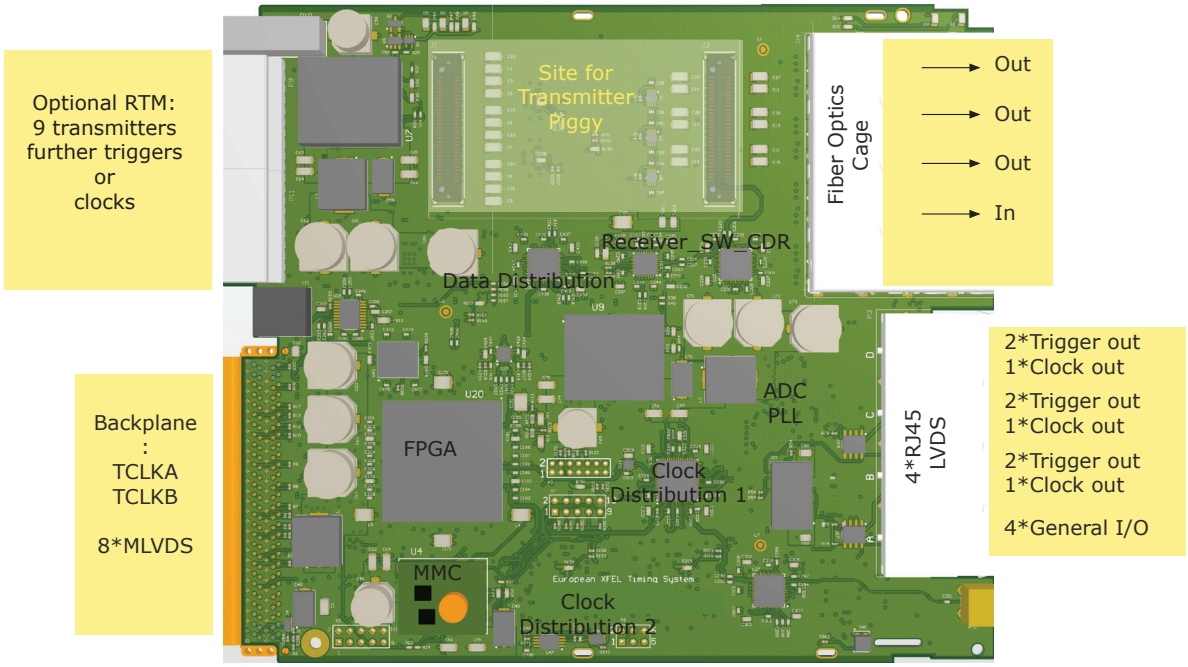
3. Figure: NAMC-psTimer with NAMC-psTimer-RTM-C, NAMC-psTimer-RTM-F, NAMC-psTimer-RTM-ST

2.2. Block Diagram

The following figure shows a block diagram of the **NAMC-psTimer** with the piggyback module **NAMC-psTimer-P2** and in figure 4 the location of the block diagram components on the **PCB.**



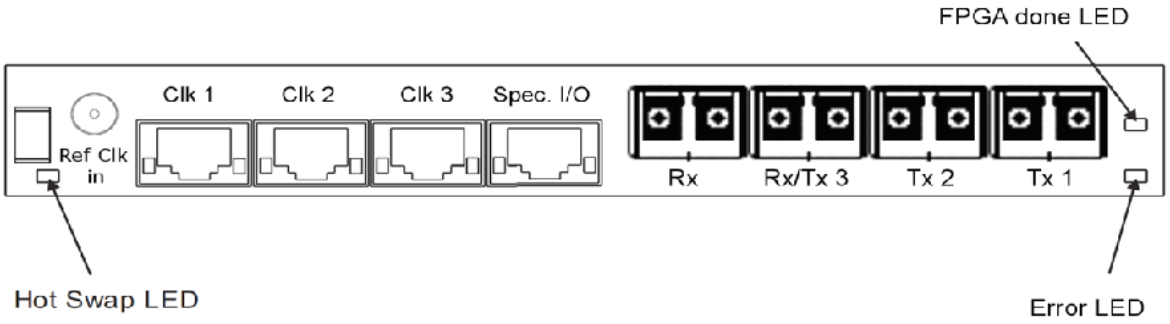
4. Figure: NAMC-psTimer – Block Diagram – Overview



5. Figure: NAMC-psTimer – PCB – Overview

2.3. Front Connector

The main clock signal (also called 'base frequency'), to which all on-board generated clocks and triggers are phase-stable, may be provided optically from another psTimer-AMC, electrically via a front SMA connector or generated locally via an onboard PLL. The clock frequency has to be between 500MHz and 1.4Ghz[1]. If provided electrically by an external clock source, the input voltage must be in range 0V < VIL < 0.8V and 0.9V < VIH < 2.5V.



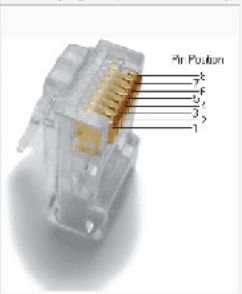
6. Figure: NAMC-psTimer Front Panel

2.3.1. SFP Connectors

The NAMC-psTimer has 4 Small Form-factor Pluggable (SFP) connectors on its front panel. SFP modules with a bandwidth of at least 1.25GBaud are supported. Connector labelled 'Rx' may receive a 500-1.400MHz modulated timing signal from another (master-)psTimer or is unused in stand alone mode. 'Rx/Tx3' labelled connector is configurable either as redundant input (same functionality as 'Rx' connector) or as an output of a 500-1.400MHz modulated timing signal. Both connectors 'Tx3' and 'Tx4' will output a 500-1.400MHz modulated timing signal if a 'piggy-back' or 'daughter-board' is installed on the NAMC-psTimer. Functionality of the piggy-back board will be described in section NAMC-psTimer-P1 and NAMC-psTimer-P2 in a later revision of this manual.

2.3.2. Special Input/Output connector

The RJ45 connector labelled 'Spec. I/O' on the AMC front panel contains 4 pairs of M-LVDS[2] signals which are connected to the onboard FPGA. Depending on the FPGA firmware, each pair can be used as input or output independently. With the currently available firmware, all pairs are configured as inputs. They can be used for external trigger inputs and routed directly or combined (AND, OR, Gate) with other triggers to any other trigger output on the front, backplane or RTM. Each pair could also be configured to temporarily inhibit the generation of any trigger output channel. The polarity of any input signal can be inverted in the configuration. An external adapter for converting single-ended TTL signal to LVDS signals is available.

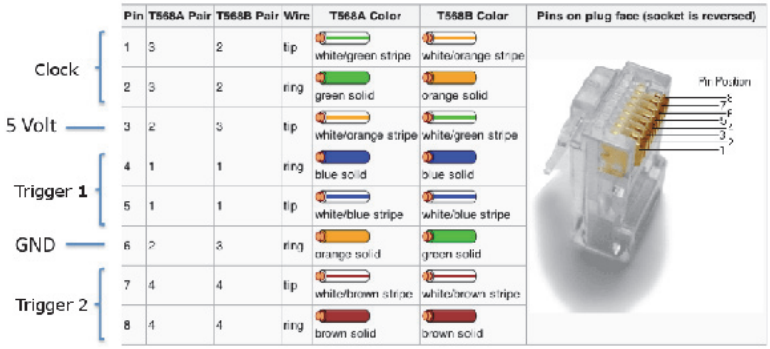
	Pin	T568A Pair	T568B Pair	Wire	T568A Color	T568B Color	Pins on plug face (socket is reversed)
Spec I/O 1	1	3	2	tip	white/green stripe	white/orange stripe	
	2	3	2	ring	green solid	orange solid	
Spec I/O 4	3	2	3	tip	white/orange stripe	white/green stripe	
Spec I/O 2	4	1	1	ring	blue solid	blue solid	
	5	1	1	tip	white/blue stripe	white/blue stripe	
Spec I/O 4	6	2	3	ring	orange solid	green solid	
Spec I/O 3	7	4	4	tip	white/brown stripe	white/brown stripe	
	8	4	4	ring	brown solid	brown solid	

7. Figure: Special I/O RJ45 Front Connector Pinout

[2] Multipoint Low Voltage Differential Signal

2.3.3. Clk1, Clk2, Clk3 Trigger output connectors

Each of the RJ45 connectors labelled 'Clk1', 'Clk2' and 'Clk3' contains a switchable 5 Volt power supply line and 3 pairs of LVDS signals. The first output is a high precision clock line which can be configured to output any frequency that can be generated from the main clock frequency by integer division. The other two output channels can be configured to output deliverying any signal generated by the onboard FPGA. Currently triggers, clocks (main clock frequency/24 divided by an integer), bunch pattern (special pattern generated by a master timing system) or any of the Special I/O input signals.



Pin	T568A Pair	T568B Pair	Wire	T568A Color	T568B Color
1	3	2	tip	white/green stripe	white/orange stripe
2	3	2	ring	green solid	orange solid
3	2	3	tip	white/orange stripe	white/green stripe
4	1	1	ring	blue solid	blue solid
5	1	1	tip	white/blue stripe	white/blue stripe
6	2	3	ring	orange solid	green solid
7	4	4	tip	white/brown stripe	white/brown stripe
8	4	4	ring	brown solid	brown solid

8. Figure: Special I/O RJ45 Front Connector Pinout

2.3.4. AMC backplane connector

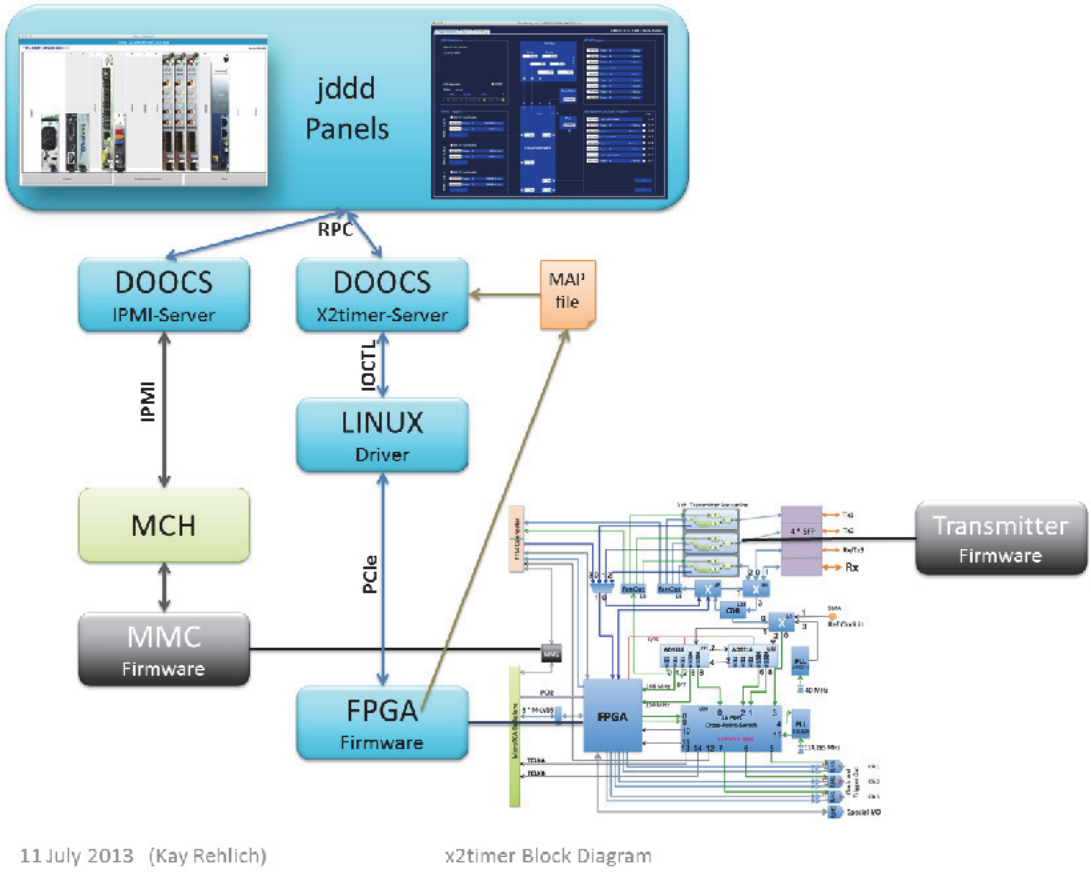
Port 1, 2, 3, 5 - 11, 14, 15, 16 are not connected. Port 0, 4, 12 and 13 are connected to the onboard FPGA high speed interfaces. With the current firmware only Port 4 is used as PCIe communication interface with the host CPU. Port 17 - 20 are connected to the onboard FPGA M-LVDS connections and can be configured as trigger input or output independently. TCLKA/B can output any frequency up to 150 MHz in phase with the main clock.

2.3.5. Rear Transition Module connector

The RTM Zone3 connector contains connections for 9 triggers, high frequency modulated timing signal, PDE programming interface, interrupts and IIC interfaces. For a detailed description please contact DESY or NAT.

3. Software Installation

The following shows the software building blocks of the NAMC-psTimer.



9. Figure: NAMC-psTimer Software Interface Diagram

3.1. Prerequisites

Before downloading and installing the software environment for using the NAMC-psTimer, please verify that the module has been correctly identified on the PCIe bus. Type `lspci` on the Linux command line and check that a device `xx:yy.z Communication synchronizer: Xilinx Corporation Device 0020` is displayed. If the device is missing in the device list, check that your MCH is configured correctly and look at the troubleshooting section.

3.2. DOOCS Environment and Driver Installation

Currently only a user interface based on DESYs DOOCS environment is available. A basic installation guide can be found online at
`https://ttfinfo.desy.de/DOOCSWiki/Wiki.jsp?page=DOOCSStandaloneInstallation#section-DOOCSStandaloneInstallation-InitialSetupUbuntu`.

Follow the instructions up to the point where you edit
`/export/doocs/server/ENS_auth/ens_server.conf`.

Add this entry at the bottom of the file:

host: "LOCALHOST"
device: "X2TIMER"
server: "TEST.DOOCS/X2TIMER"
libprog: 610489682
__addserver__

Restart the ENS server and continue with the instructions. You only need to install x1timer driver with

```
apt-get install x1timer-dkms
```

and x2timer server with

```
apt-get install doocs-x2timer-server.
```

When all packages are installed, `x2timers[]` should be visible in `/dev`.

Open the config file

```
/export/doocs/server/x2timer_server/x2timer_server.conf
```

and change these lines:

opergid: 999
SVR.FACILITY: "TEST.DOOCS"
SVR.DEVICE: "X2TIMER"
eq_fct_name: "UBUNTU.0"
NAME: "UBUNTU.0"
SLOT: [AMC slot number of x2timer AMC]

The line `oper_gid` sets the permissions to the x2timer server. The value depends on which users should be able to do any changes to the server configuration. You can get the group id of any users with the command `id` on the command line. This is the same for the watchdog server. If you get a "'permission denied"' in the jddd-panels later, please change the values in the config file accordingly and restart the servers as described in the online manual. Continue with the installation of Java DOOCS Data Display and the Java Runtime Environment.

4. Configuration

4.1. JDDD

JDDD - or Java DOOCS Data Display - is a graphical Java-based editor for control system panels developed and maintained at Deutsches Elektronen-Synchrotron. With JDDD it is very simple to create your own graphical panels for configuring the NAMC-psTimer or use the panel that are distributed by DESY. The latest version can be downloaded at `http://jddd.desy.de/`. During installation you should already have downloaded JDDD. You can either run it from the web or from a command line with the command `jddd`.

4.2. Watchdog Setup

During installation of the driver and server you already downloaded a package with the most important panels to configure the watchdog server (which will automatically launch the x2timer_server after a reboot) and the NAMC-psTimer itself. Choose "'File"'"'Open Local File..."' in jddd and select
`/usr/share/jddd/panels/global/LocalWatchdogOverview.xml`.

Click "'Run Active Panel"'. Scroll down to the entry "'SVR.X2TIMER"' and click the "'control"'-button. Click on the "'Start and Online"'-button and after that the "'On"'-checkbox in the upper right corner. The watchdog server is now configured to automatically start the x2timer server. Close the windows and select "'File"'"'Open Local File..."' in jddd and select
`/usr/share/jddd/panels/global/timing/x2timer/SlaveTiming.xml`.

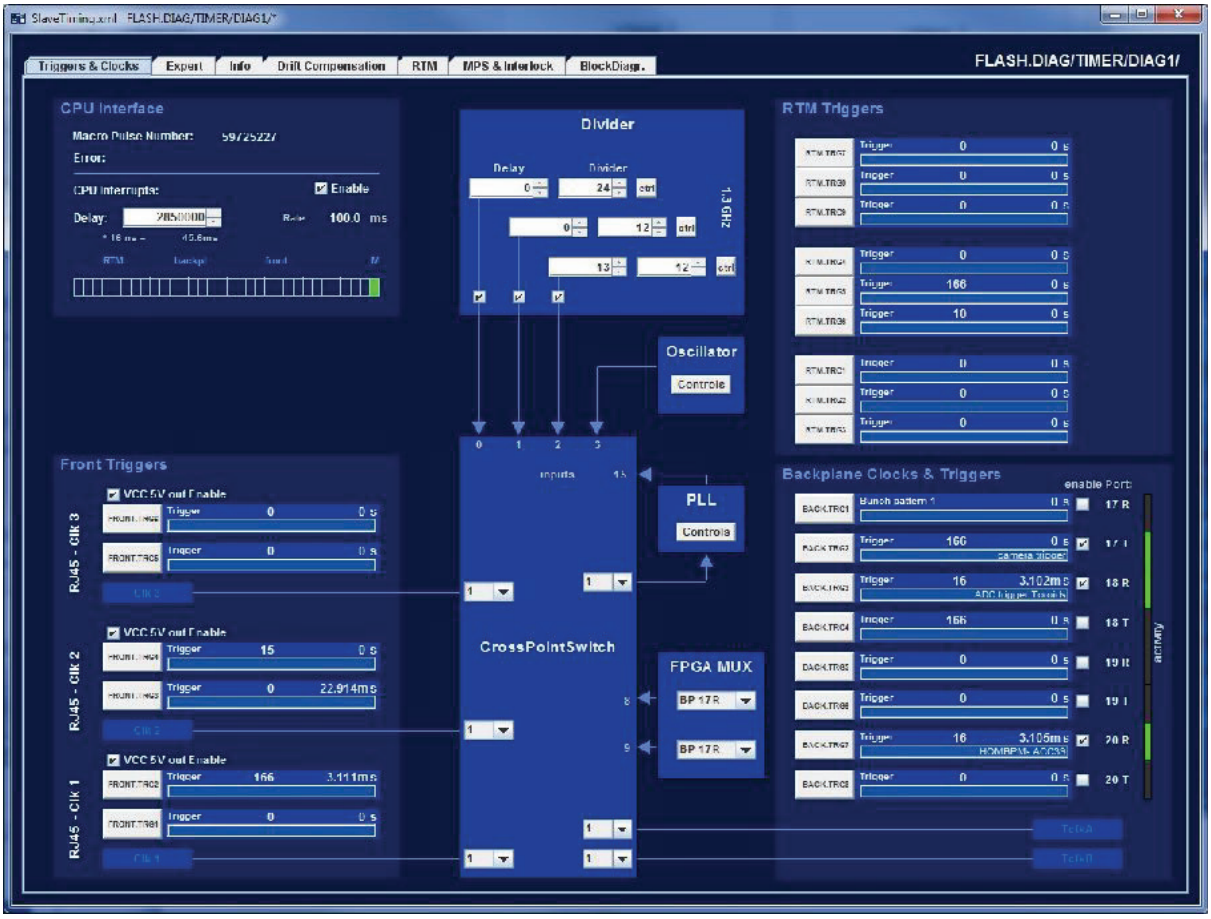
Before running that panel, enter "'TEST.DOOCS/X2TIMER/UBUNTU.0/"' in the "'adr"'-property on the right and press enter. Now run the active panel. Once the psTimer is configured, the same configuration will be loaded to the hardware after a power cycle through the server. If you wish to change the configuration frequently, you can save the panel anywhere in your home directory.

4.3. NAMC-ps-Timer Configuration

In figure 6 an overview of all output channels of the NAMC-psTimer is shown. It is divided into these parts:

- top left: CPU interface - CPU interrupts can be enabled and disable here. Each output channel can generate it's own interrupt at the moment it is triggered. Only one bit should be enabled in the register.
- bottom left: output configuration for each front output (3*RJ45 connector: 2* trigger + 1* low jitter clock per connector). Click the button "FRONT.TRGx" on the left side of a channel to configure the output.
- top right: output configuration for each rear transition module output. Click the button "FRONT.TRGx" on the left side of a channel to configure the output.
- bottom right: output configuration for each AMC connector output. Click the button "FRONT.TRGx" on the left side of a channel to configure the output. Enable the checkbox on the right side to enable the output driver.

- mid top: low jitter clock dividers - Enter the divider (1.300MHz/x) and the delay and mark the according checkbox below to enable the output driver of the divider channel. Only enable one output to reduce noise and crosstalk.



10. Panel: Output Configuration Panel

- mid bottom: low jitter crosspoint switch - mark the checkbox and enter the input number for any output channel.

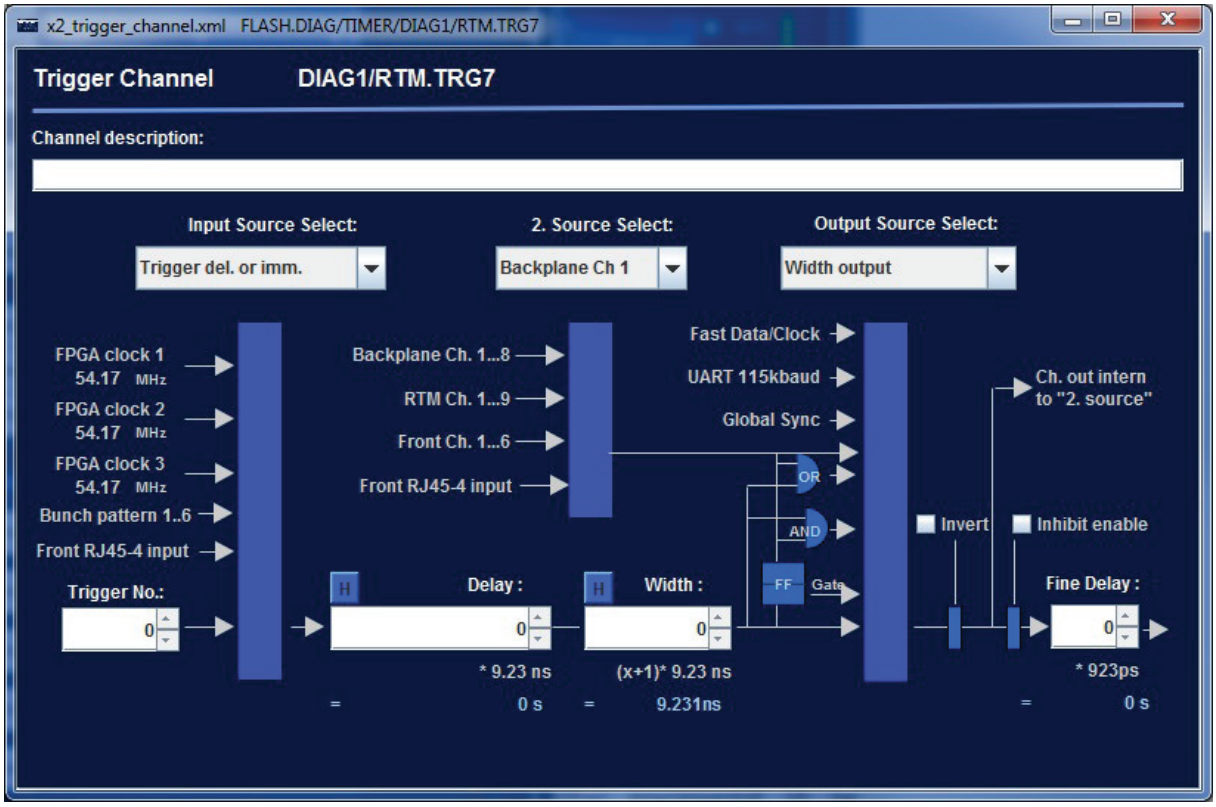
4.3.1. Clock Distribution

In the middle of panel 9 the low-jitter clock distribution is visible. In the upper part, 3 independent dividers are configurable. The input clock to these dividers is the main clock. Each output of the dividers is connected to the low-jitter crosspoint switch which is visible in the lower part. From here, the user can select, where to route the clock signals. They can be output at each RJ45 output connector at the front panel, to an internal PLL to generate different frequencies, or to the TCLKA/B lines at the AMC backplane connector.

4.3.2. Trigger Output Configuration

In panel 10 the configuration panel for one channel is shown. A channel description should be entered in the top row. As input these option can be selected:

- Trigger delayed - a Event generated by the MicroTCA timing master.
- Trigger immediate - an asynchronous Event coming from the old Timing System or from an external input to the MicroTCA timing master.
- Trigger delayed or immediate - Output is triggered both at delayed of immediate events
- Bunch pattern (1-6) - Output is triggered at occurance of a bunch pattern which can be masked in the **Panel 11** of the Slave Timing Panel.
- FPGA clock (1-3) - FPGA clock configured in **Panel 11** will be connected to output



11. Panel: Single Channel Configuration Panel

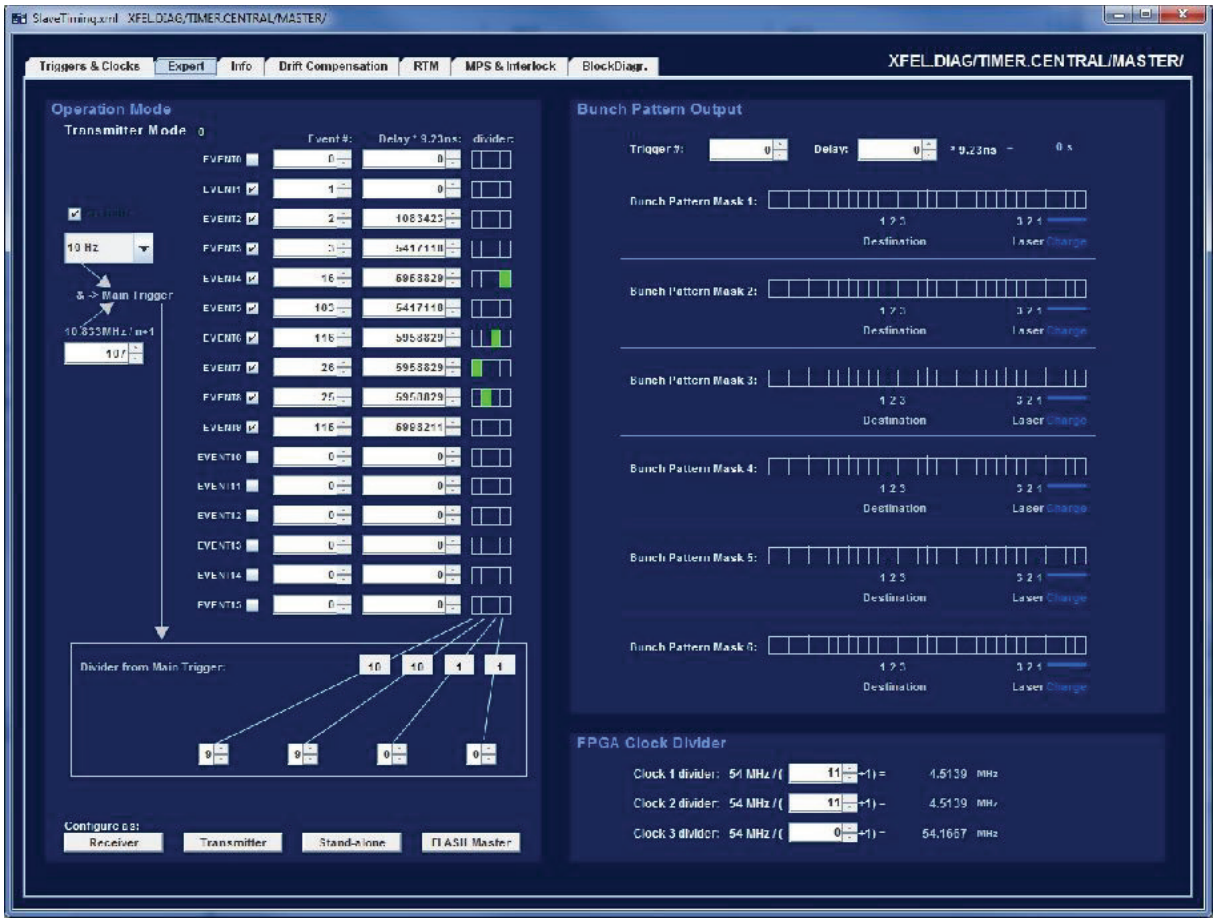
- RJ45 input (1-4) - The signal connected to RJ45 Special I/O connector at the AMC front panel will be output

For more flexibility, each configured channel can be combined with a second channel before it is connected to the RJ45 connector/backplane/RTM. The second channel can be selected in the second drop-down list. Combinations of the two channel can be

- Width output - ignore second source, directly connect channel to output
- Clock 108MHz - ignore both sources, connect 108MHz clock from FPGA to output

- Data 108MHz - ignore both sources, connect 108MHz data link containing timing protocol from FPGA to output
- UART 115k - ignore both sources, connect 115kBit Beckhoff signal from FPGA to output
- Gate - first source channel starts trigger output, second source channel ends trigger output
- 2. Channel - output the same signal that is already configured at some other output channel
- AND 2. channel - both source channels have to be triggered to generate a trigger at the output
- OR 2. channel - either of both source channels may be triggered to generate a trigger at the output
- other (may be used for debug purposes)

In the bottom line the event number on which will be triggered, the local delay, the pulse width of the output signal and a local fine delay can be entered.



12. Panel: Output Configuration Expert Panel

4.3.3. Expert Tab

In panel 11 the advanced configuration of the NAMC-psTimer is shown. It's split into

these parts:

- left: Operation mode - Set the configuration mode: Stand-Alone, Transmitter or Receivers
- top right: bunch pattern mask configuration-
- bottom right: FPGA clock divider: FPGA can generate 3 phase stable frequencies, generated from 54,167 MHz. A divider for each clock can be entered here. Each FPGA clock can be connected to any output.

Each NAMC-psTimer = x2timer can be configured to run as stand-alone system (using internal PLL to generate main clock), transmitter system (using front SMA connector as main clock) or as receiver (main clock is generated in the timing master). If it is configured as stand-alone or transmitter, events can be configured here. The main repetition rate is selected from a dropdown menu. For each event an integer divider may be configured, so that e.g. one event is output at 10 Hz, another event at 5 Hz and a third event at 2 Hz. If the NAMC-psTimer runs as a receiver, events are generated by the timing master and must be configured there.

4.3.4. Chapters planned for future manual revisions

- bunch pattern generation
- firmware update mechanism

5. Hardware

5.1. AMC Port Definition *(needs to be reviewed)*

2. AMC Port Mapping Strategy

	Port #	AMC Port Mapping Strategy	Ports used as
Basic Connector	CLK1	Clocks	Reference Clock 1 / TCLKA
	CLK2		Reference Clock 2 / TCLKB
	CLK3		Reference Clock 3 / FCLKA
	0	Common Options Region	unassigned
	1		unassigned
	2		unassigned
	3		unassigned
	4	Fat Pipes	PCIe Lane 0
	5		unassigned
	6		unassigned
	7		unassigned
Extended Connector	8	Region	unassigned
	9		unassigned
	10		unassigned
	11		unassigned
	12	Extended Options Region	AMC MLVDS
	13		AMC MLVDS
	14		To be verified unassigned?
	15		To be verified unassigned?
	16		TCLKC / TCLKD
	17		AMC MLVDS
	18		AMC MLVDS
	19		AMC MLVDS
	20		AMC MLVDS

5.2. Front Panel and LEDs

The **NAMC-psTimer** module is equipped with various LED to display an overview real time status of the most important board functions.

A detailed description of these will follow in a later version of this manual.

5.3. Connector

S1: AMC Connector (needs to reviewed and corrected)

3. S1: AMC Connector – Pin-Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	GND	GND	170
2	PWR	TDI	169
3	/PS1	TDO	168
4	PWR_IPMB	/TRST	167
5	GA0	TMS	166
6	RESVD	TCK	165
7	GND	GND	164
8	RESVD	PORT20_TX_P	163
9	PWR	PORT20_TX_N	162
10	GND	GND	161
11	PORT0_TX_P	PORT20_RX_P	160
12	PORT0_TX_N	PORT20_RX_N	159
13	GND	GND	158
14	PORT0_RX_P	PORT19_TX_P	157
15	PORT0_RX_N	PORT19_TX_N	156
16	GND	GND	155
17	GA1	PORT19_RX_P	154
18	PWR	PORT19_RX_N	153
19	GND	GND	152
20	NC	PORT18_TX_P	151
21	NC	PORT18_TX_N	150
22	GND	GND	149
23	NC	PORT18_RX_P	148
24	NC	PORT18_RX_N	147
25	GND	GND	146
26	GA2	PORT17_TX_P	145

Pin #	AMC-Signal	AMC-Signal	Pin #
27	PWR	PORT17_TX_N	144
28	GND	GND	143
29	NC	PORT17_RX_P	142
30	NC	PORT17_RX_N	141
31	GND	GND	140
32	NC	TCLKD_P	139
33	NC	TCLKD_N	138
34	GND	GND	137
35	NC	TCLKC_P	136
36	NC	TCLKC_N	135
37	GND	GND	134
38	NC	NC	133
39	NC	NC	132
40	GND	GND	131
41	/ENABLE	NC	130
42	PWR	NC	129
43	GND	GND	128
44	PORT4_TX_P	RESVD	127
45	PORT4_TX_N	NC	126
46	GND	GND	125
47	PORT4_RX_P	NC	124
48	PORT4_RX_N	NC	123
49	GND	GND	122
50	NC	PORT13_TX_P	121
51	NC	PORT13_TX_N	120
52	GND	GND	119
53	NC	PORT13_RX_P	118
54	NC	PORT13_RX_N	117
55	GND	GND	116
56	IPMB_SCL	PORT12_TX_P	115

Pin #	AMC-Signal	AMC-Signal	Pin #
57	PWR	PORT12_TX_N	114
58	GND	GND	113
59	NC	PORT12_RX_P	112
60	NC	PORT12_RX_N	111
61	GND	GND	110
62	NC	NC	109
63	NC	NC	108
64	GND	GND	107
65	NC	NC	106
66	NC	NC	105
67	GND	GND	104
68	NC	NC	103
69	NC	NC	102
70	GND	GND	101
71	IPMB_SDA	NC	100
72	PWR	NC	99
73	GND	GND	98
74	TCLKA_P	NC	97
75	TCLKA_N	NC	96
76	GND	GND	95
77	TCLKB_P	NC	94
78	TCLKB_N	NC	93
79	GND	GND	92
80	FCLKA_P	NC	91
81	FCLKA_N	NC	90
82	GND	GND	89
83	/PS0	NC	88
84	PWR	NC	87
85	GND	GND	86

6. Board Specification

6.1. Board Specification

4. NAMC-psTimer Specification – Overview

AMC-Module	Standard Advanced Mezzanine Card, double width, full-size
Front-I/O	4 RJ45, 4 SPF cages, 1 SMA
Main Memory	-
FPGA	Spartan-6
Firmware	Desy-Timing-Image
Power Consumption	12V, 2.5A
Operating Temperature	0°C – +55°C with forced cooling
Storage Temperature	-40°C - +85°C
Humidity	10% – 90% rh non-condensing
Standards compliance	PICMG AMC.0 Rev. 2.0 PICMG AMC.2 Rev. 1.0 (Type E2) IPMI Specification v2.0 Rev. 1.0 PICMG µTCA.0 Rev. 1.0

7. Hardware Installation

7.1. Safety Note

To ensure proper functioning of the **NAMC-psTimer** during its usual lifetime take the following precautions before handling the board:

CAUTION
Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime!

- Before installing or uninstalling the **NAMC-psTimer** read this installation section
- Before installing or uninstalling the **NAMC-psTimer**, read the Installation Guide and the User's Manual of the carrier board used, or of the uTCA system the board will be plugged into.
- Before installing or uninstalling the **NAMC-psTimer** on a carrier board or both in a rack:
- Check all installed boards and modules for steps that you have to take before turning on or off the power
- Take those steps
- Finally turn on or off the power if necessary
- Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAMC-psTimer** is connected to the carrier board or to the uTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
- is bolted the front panel or rack
- and shielded by closed housing

7.2. Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements!

7.2.1. Requirements

The installation requires only:

1. µTCA backplane for connecting the **NAMC-psTimer**
2. power supply
3. cooling devices

7.2.2. Power supply

The power supply for the **NAMC-psTimer** must meet the following specifications:

4. required for the module: +12V / 2.5A max.

7.2.3. Automatic Power Up

In the following situations the **NAMC-psTimer** will automatically be reset and proceed with a normal power up:

5. The voltage sensor generates a reset
6. when +12V voltage level drops below 10V
7. when +3.3V voltage level drops below 3.00V
8. The carrier board / backplane signals a PCIe-Reset.

7.3. Statement on Environmental Protection

7.3.1. Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.3.2. Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.
If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on

"Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.3.3. Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can be found on the PCB.

7.3.4. Product Safety

The board complies with EN60950 and UL1950.

7.3.5. Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

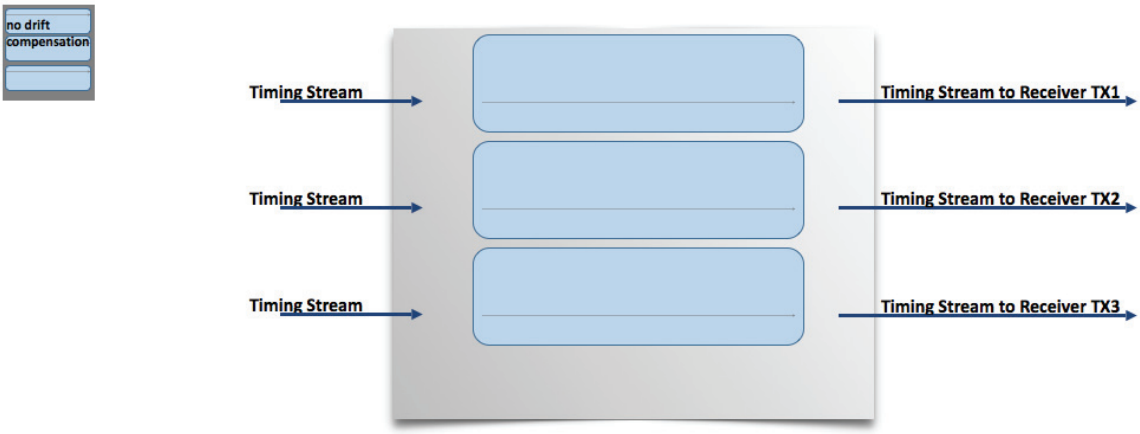
8. Known Bugs / Restrictions of Hardware and Software

none

Appendix A: NAMC-psTimer-P1, NAMC-psTimer-2

NAMC-psTimer-P1
3 channel transmitter mezzanine
without drift compensation

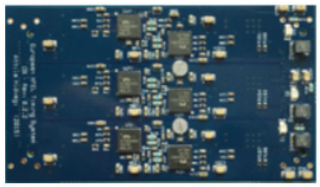
all three channels shown ->

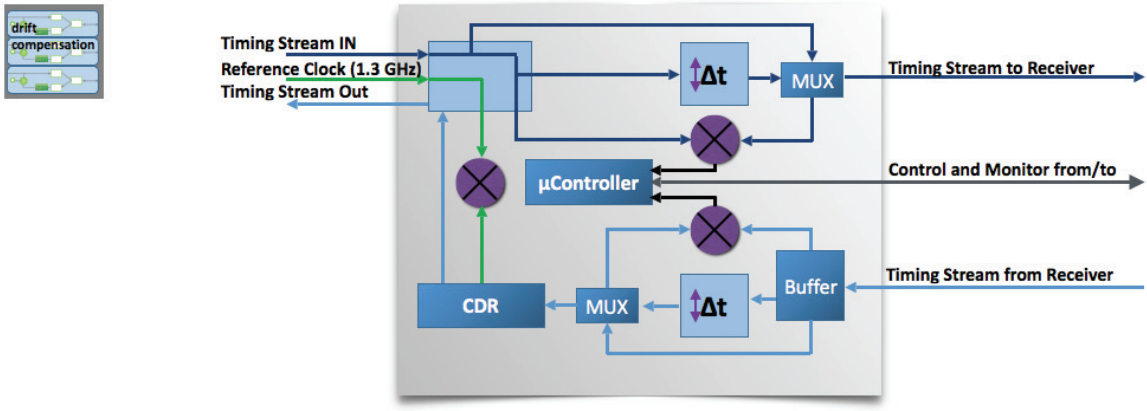


13. Block Diagram: NAMC-psTimer-P1

NAMC-psTimer-P2
3 channel transmitter mezzanine
with drift compensation

one channel out of three shown ->

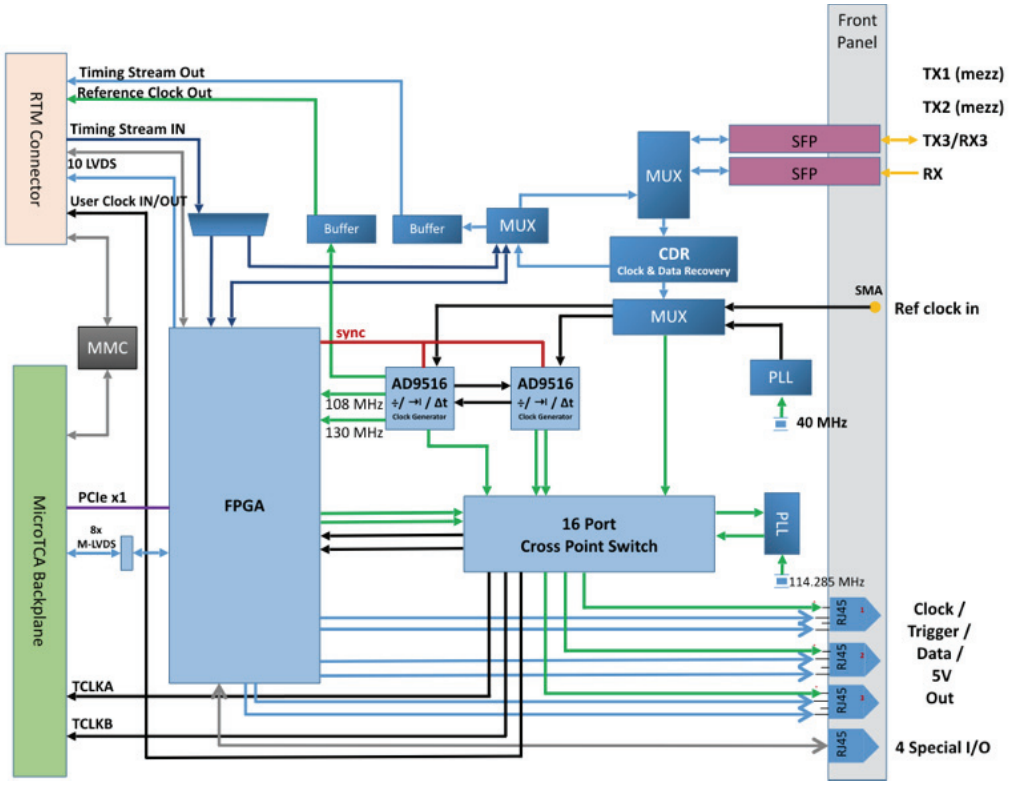




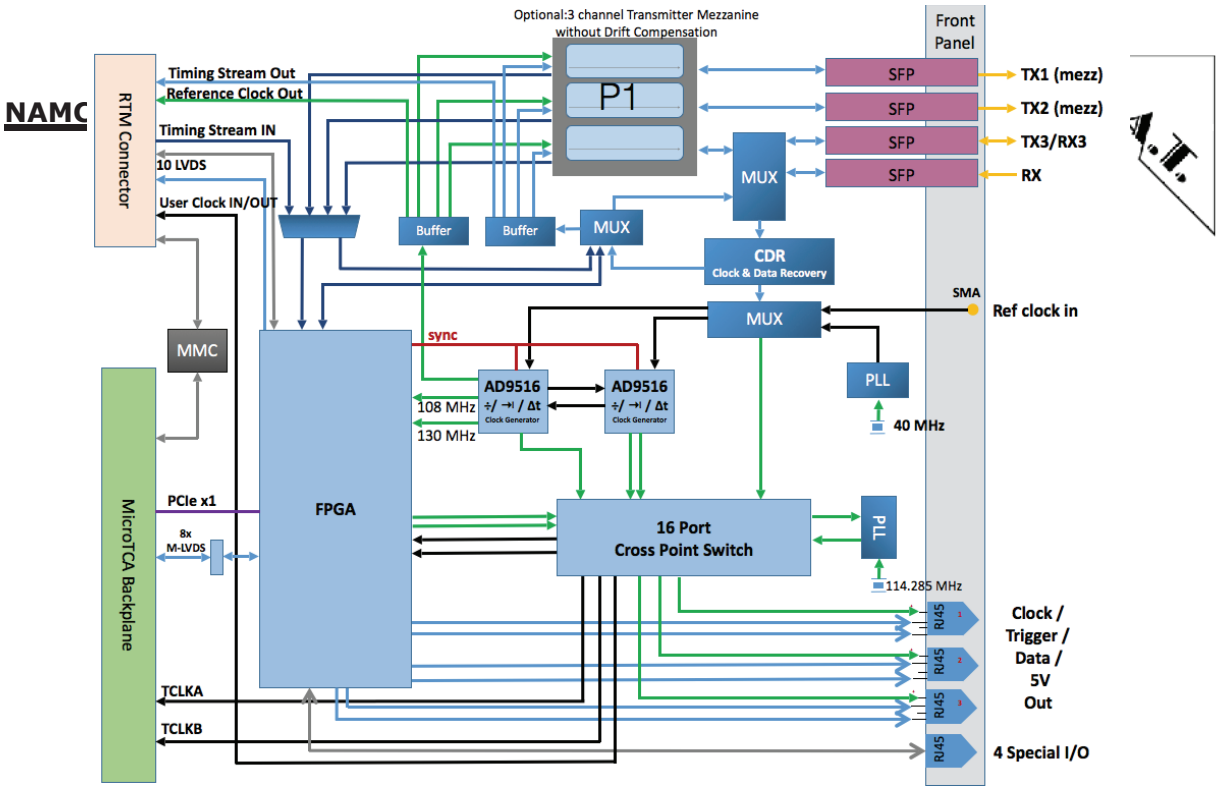
14. Block Diagram: NAMC-psTimer-P2

The next block diagrams show the NAMC-psTimer populated

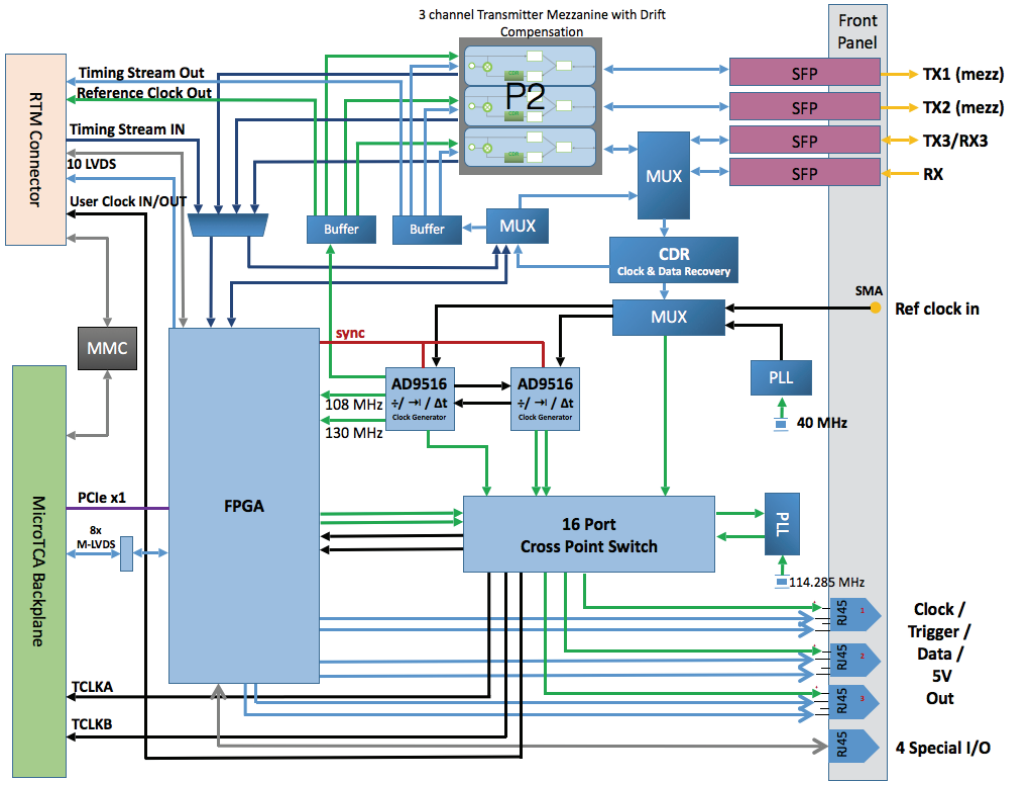
- without any piggy-back module,
- with the NAMC-psTimer-P1 piggy-back module with no drift compensation
- with the NAMC-psTimer-P2 piggy-back module with drift compensation



15.Block Diagram: NAMC-psTimer without mezzanine P1 or P2



*16.Block Diagram: NAMC-psTimer **with** NAMC-psTimer-**P1** (**no** Drift Compensation)*

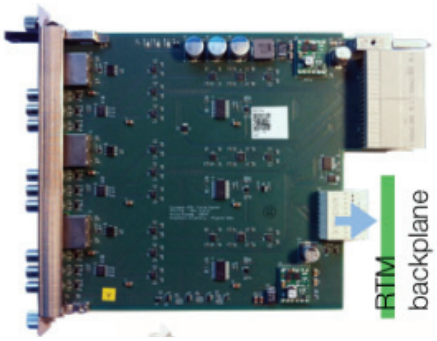


*17.Block Diagram: NAMC-psTimer **with** NAMC-psTimer-**P2** (Drift Compensation)*

Appendix B: NAMC-psTimer-RTM-C, …-RTM-F

NAMC-psTimer-RTM-C was called before x2Timer-RTM-Trg1 and routes triggers, clocks and data coming from the Zone-3 connector of the NAMC-psTimer to 9 Lemo connectors. Three of nine channels offer a 5ps resolution.

9 Lemo outputs (50 Ohm):
- Triggers, Clocks, Data
- 3 channels with 5ps resolution

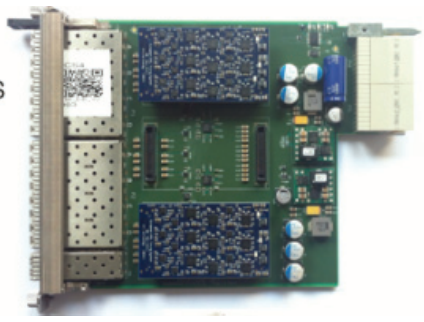


Then NAMC-psTimer-RTM-C adds nine additional outputs to the NAMC-psTimer.

More technical details will be made on request by Desy.

NAMC-psTimer-RTM-F was called before x2Timer-RTM-Trg2 and routes triggers, clocks and data coming from the Zone-3 connector of the NAMC-psTimer to 9 SFP cages, which can be populated with SFP modules with different optical wave length. Common are 850nm and 1120nm.

9 SFP outputs:
- length compensated fiber links



Then NAMC-psTimer-RTM-F adds nine additional optical outputs to the NAMC-psTimer.

Can be equipped with 3x NAMC-psTimer-P1 with no drift compensation or 3x NAMC-psTimer-P2 mezzanine providing drift compensation

More technical details will be made on request.

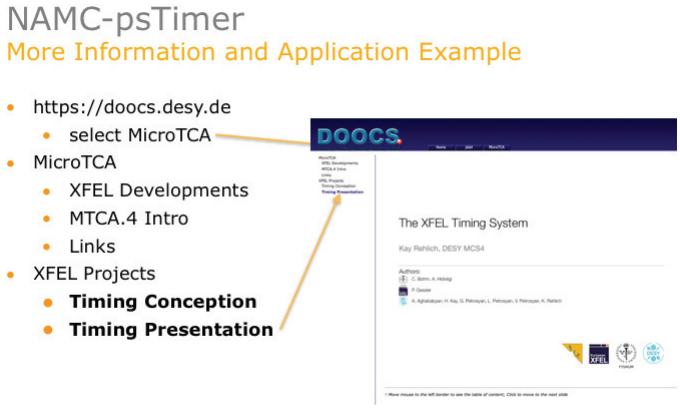
Appendix C: Reference Documentation

[1] http://tesla.desy.de/doocs/doocs.html
(click on the MTCA-tab beside home and jddd)
[2] http://tesla.desy.de/doocs/Timing/CDRv2.2short.pdf
[3] To dig deeper in the Timing and other Control Mechanism at Desy, please open

http://tesla.desy.de/doocs/doocs.html

Klick on µTCA Development on the left column below European XFEL.

and then on „Timing Presentation“



Appendix D: Document's History

Revision	Date	Description	Author
0.1	01.03.2016	initial release	cs (Desy)
1.0	25.05.2016	Transfer to NAT template, add hardware information	vd
1.1	13.12.2016	Formatting and add new front panel picture, add in chapter 3.2 some configuration parameter	vd
1.2	14.12.2017	Rework introduction chapter, include compatible RTM and piggy-back modules. Update broken reference links, add references of timing background at Appendix A	vd
1.3	14.12.2017	replaced block diagram of NAMC-psTimer by a higher resolution block diagram	vd

Appendix E: Known Manual Errors

Revision	Date	Description	Author
1.1	15.12.2016	Figure numbering needs correction caused by the usage of another author tool	vd
1.2	14.12.2017	Missing detailed description of NAMC-psTimer-RTM-C, NAMC-psTimer-F, NAMC-psTimer-P1 and NAMC-psTimer-P2	vd