NAMC-TCK7
Data Processing AMC Module
Technical Reference Manual V1.1
HW Revision 1.x

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by 0x. The following table gives a list of the abbreviations used in this document.

Table 1: List of used abbreviations

Abbreviation	Description
ADC	Analog-Digital-Converter
AMC	Advanced Mezzanine Card
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
DDR SDRAM	Double Data Rate Synchronous Dynamic RAM
DESY	Deutsches Elektronen-Synchrotron
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
GTX	Gigabit Transceiver
JTAG	Joint Test Action Group
IPMI	Intelligent Platform Management Interface
LED	Light Emitting Diode
LLL	Low Latency Links
LLRF	Low Latency Radio Frequency
(M)-LVDS	(Multipoint) Low Voltage Differential Signaling
MMC	Module Management Controller
µTCA/MTCA/MicroTCA	Micro Telecommunications Computing Architecture
PCIe	Peripheral Component Interconnect Express
PLL	Phase-Locked Loop
RAM	Random Access Memory
RTM	Rear Transition Module
SFP(+)	Small Form-Factor Pluggable
SPI (FLASH)	Serial Peripheral Interface (FLASH)
SMB	SubMiniature version B
UART	Universal Asynchronous Receiver/Transmitter
(Micro)-USB	(Micro) Universal Serial Bus

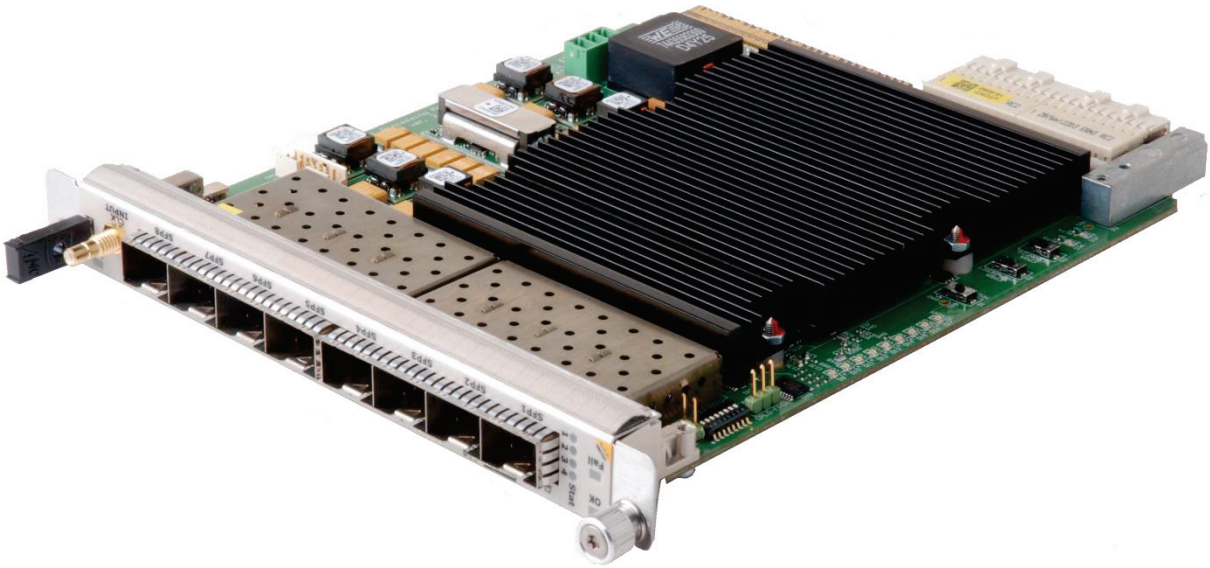
1 Introduction

The **NAMC-TCK7** is a general purpose high-performance low-latency data processing AMC module providing processing power, data memory, communication links, and reference clock signals. Originally designed as a LLRF (Low Level Radio Frequency) cavity field stabilizing controller, the application field is much wider.

The XILINX Kintex-7 FPGA (XC7K355T or XC7420T) delivers computing power and memory for low-latency digital signal processing. It supports a number of LLLs (Low Latency Links) available on the front plate, at the backplane, and via a RTM (Rear Transition Module), working with several Gbps throughput. In-System firmware upgrade via IPMI and fast serial link is supported.

The following figure shows a photo of the **NAMC-TCK7.**

Figure 1: NAMC-TCK7



2 Overview

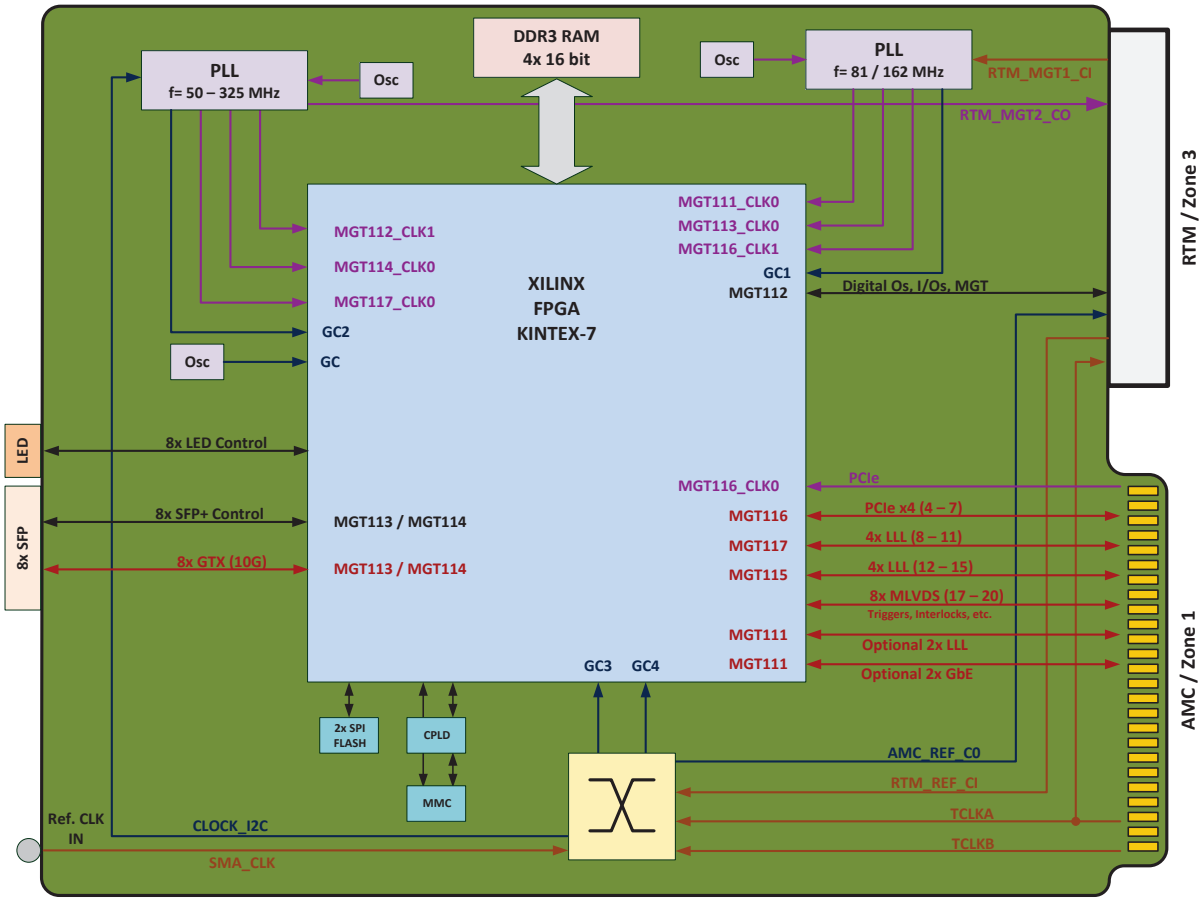
2.1 Major Features

- XILINX XILINX-7 FPGA
- DDR3 Memory
- CPLD
- Quad SPI FLASH memory
- Clock
- Connectivity
  - Front Panel
  - Backplane (Zone 1) AMC
  - Backplane (Zone 3) RTM

2.2 Block Diagram

The following figure shows a block diagram of the **NAMC-TCK7**.

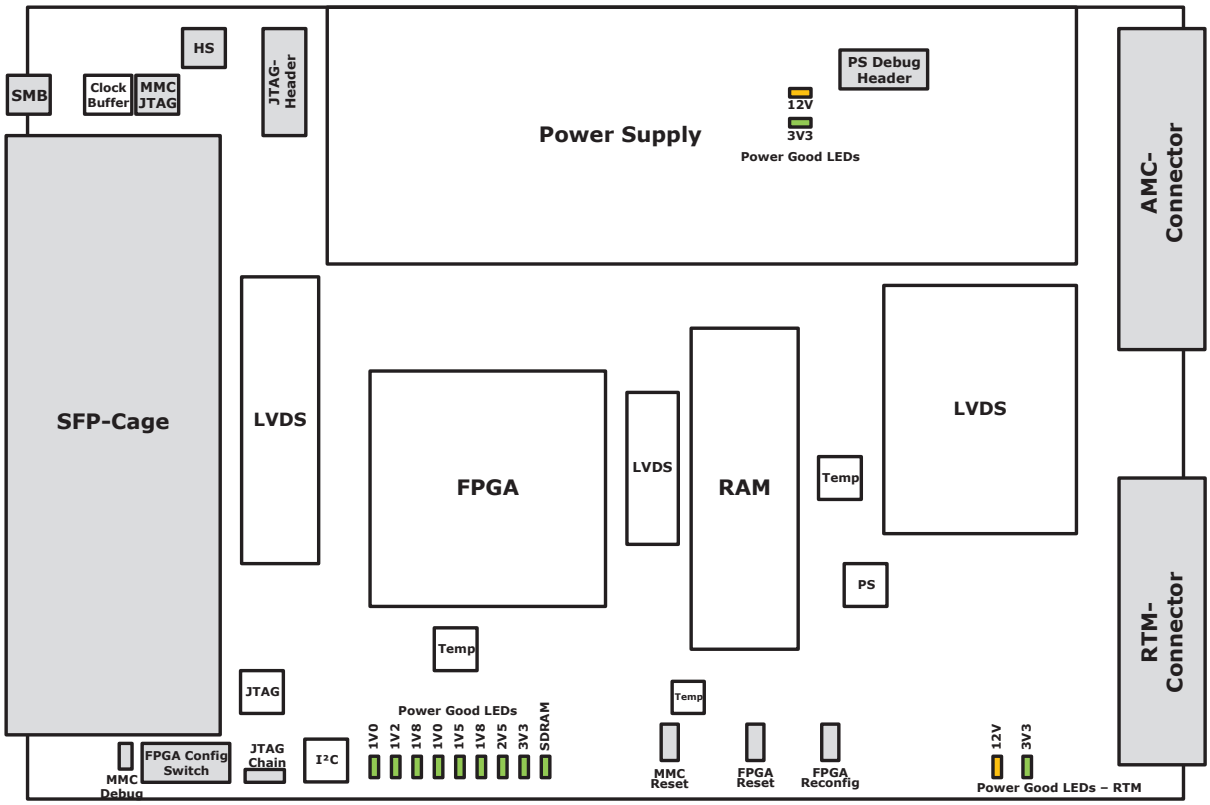
Figure 2: NAMC-TCK7 – Block Diagram

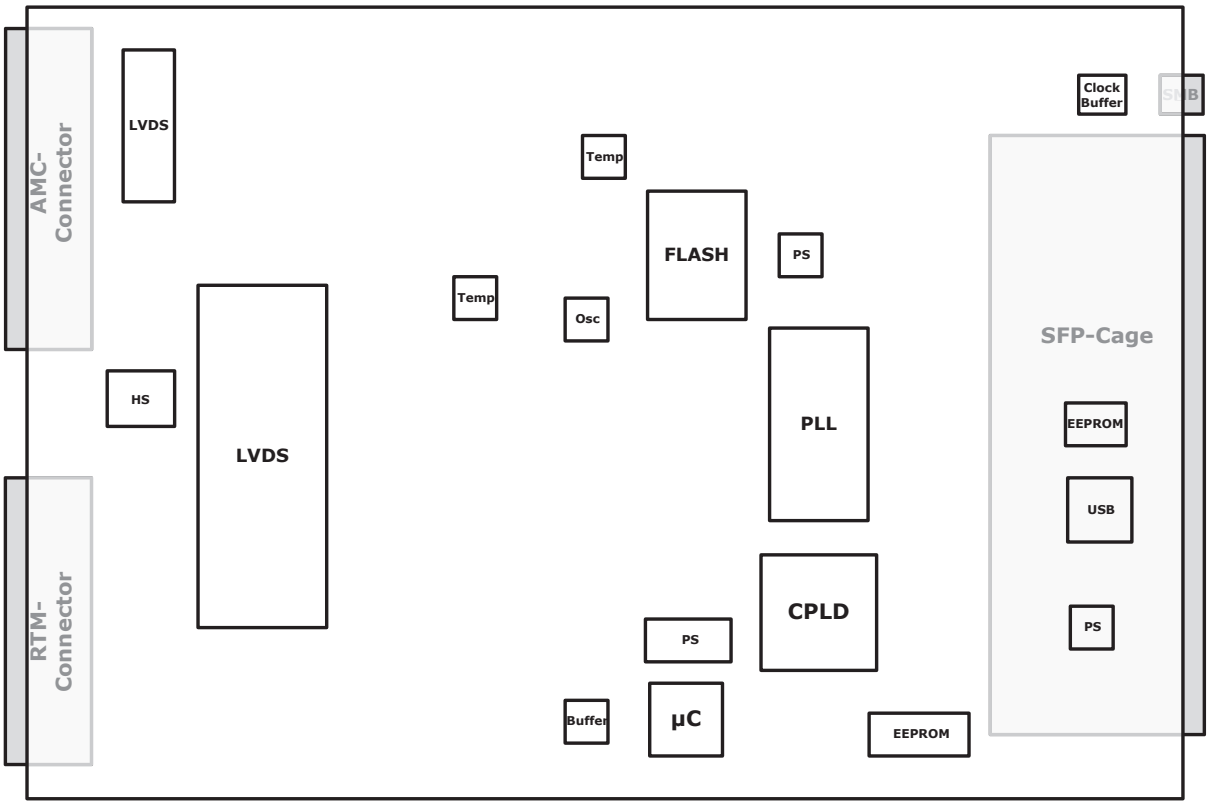


2.3 Location Diagram

The following figure shows a location diagram of the **NAMC-TCK7**.

Figure 3: NAMC-TCK7 – Location Diagram




AMC-Connector
LVDS
Temp
FLASH
PS
Clock Buffer
SNB
Temp
Osc
SFP-Cage
HS
LVDS
PLL
EEPROM
USB
CPLD
PS
PS
RTM-Connector
Buffer
µC
EEPROM

3 Board Features

The **NAMC-TCK7** can be divided into a number of functional blocks, which are described in the following paragraphs.

3.1 FPGA

The **NAMC-TCK7** hosts a XILINX Kintex-7 FPGA; XC7K355T (default) or XC7K420T (option). In default assembly option the FPGA offers 24 multi-gigabit transceivers, which support bit-rates up to 12.5 Gb/s. Hardware support for PCIe Gen2 communication is contained as well, hence the implemented x4 link can reach throughput of 20 Gb/s.

3.1.1 GTX-Transceiver-Assignment

Each GTX-Quad is allocated to a dedicated FPGA-Bank. The following table shows the assignment for the different FPGA-types.

Table 2: Assignment GTX-Transceiver to FPGA-Bank on XC7K355T

# GTX-Transceiver	# FPGA Bank
X0Y0 – X0Y3	112
X0Y4 – X0Y7	113
X0Y8 – X0Y11	114
X0Y12 – X0Y15	115
X0Y16 – X0Y19	116
X0Y20 – X0Y23	117

Table 3: Assignment GTX-Transceiver to FPGA-Bank on XC7K420T

# GTX-Transceiver	# FPGA Bank
X0Y0 – X0Y3	111
X0Y4 – X0Y7	112
X0Y8 – X0Y11	113
X0Y12 – X0Y15	114
X0Y16 – X0Y19	115
X0Y20 – X0Y23	116
X0Y24 – X0Y27	117

For further information on the XILINX Kintex-7, please refer to Appendix A.

3.2 DDR3 Memory

For temporary data storage the **NAMC-TCK7** features four SDRAM DDR3 memory chips, each with a capacity of 4Gb (16 Gb in total), operating with a data rate of 1066 Mbit/s and a width of 64 bit. The memory circuits share the address and control buses.

3.3 CPLD

The **NAMC-TCK7** features a XILINX XC2C256 CoolRunner-II CPLD. This device is used for support functions like multiplexing and switching of SPI and JTAG lines, as well as for driving status LED.

For further information on the XILINX CPLD, please refer to Appendix A.

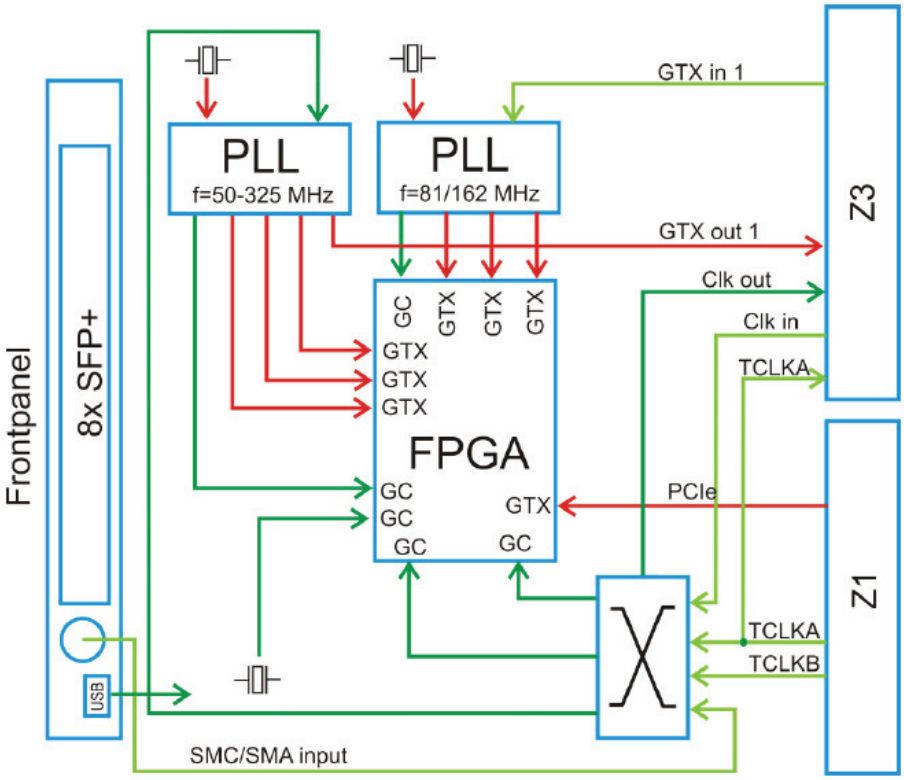
3.4 SPI FLASH Memory

For permanent data storage, the **NAMC-TCK7** is equipped with a Quad SPI FLASH containing the FPGA bit stream; the memory space beyond the bit stream is available for user application.

3.5 Clock

The XILINX Kintex-7 FPGA requires external signals for GTX transceivers, PCIe, GbE interface, and digital logic (Global Clock FPGA Signals). The clock distribution of the **NAMC-TCK7** is shown below.

Figure 4: NAMC-TCK7 – Clock Distribution



The clock distribution circuit provides a broad range of reference frequencies for high-speed serial interfaces. The following table shows an example of reference frequencies that can be generated by the on-board PLL circuits.

Table 4: Reference Frequencies for selected high-speed serial interfaces

Interface Type	Frequency [MHz]
DESY LLRF	81.25 or 160.5
PCI Express	100
Fibre Channel	106.25
Infiniband	125
GigE	125
10 GigE	156.25
10-G Fibre Channel	159.375
12 GigE	187.5
10GBASE-R, 10GBASE-X, XGMII	312.5

The PCIe clock is delivered from the AMC backplane (f = 100 MHz). The reference clock for the GTX transceivers can be provided by the RTM (e.g. f = 81.25 MHz). A programmable PLL allows multiplying the frequency (e.g. x1, x2, etc.) and then the signal is connected to the GTX transceivers and the FPGA logic.

3.6 Connectivity

3.6.1 Front Panel

The front panel provides MTCA.4 standard compliant retention devices, handle, and three IPMI LEDs as well as four LEDs for FPGA application free use. Please see chapter 4.3 Front Panel & LEDs for details.

For low-latency connections towards various LLRF components via optical fibre eight SFP+-Bays can be used.

A reference clock signal can be received via a SMB connector. Please see chapter 3.5 Clock for details.

The **NAMC-TCK7** features a MicroUSB connector which provides access to diagnostic UARTs (RS232-via-USB). The debug interface allows for performing low-speed data transmissions to the MMC and FPGA circuits.

3.6.2 Backplane (Zone 1) AMC

The Zone 1 connector provides eight low-latency communication links to the ADC boards, a PCIe interface to the controlling CPU, M-LVDS bus signals, and other signal required by the AMC standard. The two 1 GbE-channels and LLL on ports 2 and 3 are available for the XC7K420T-FPGA only.

The connector is compatible with the double-row B+-Connector specified in the AMC base specification with extensions required by PICMG MTCA.4.

3.6.3 Backplane (Zone 3) RTM

The Zone 3 connection provides low-latency links to the RTM (in case of a LLRF-System it is a vector modulator), general purpose parallel bus (LVDS levels), output signals (interlocks), reference clock inputs and outputs for GTX, and digital logic and other signals required by MTCA.4. The **NAMC-TCK7** can be connected to a RTM using two 30-pair ADF connectors.

4 Hardware

4.1 AMC Port Definition

Table 5: AMC Port Definition

Port	Signal	Characteristic	Description
0	1GbE 1000Base-X	Single lane	AMC.2
1	1GbE 1000Base-X	Single lane	AMC.2
2	LLL (Xilinx)	P2P connection, single lane	Custom
3	LLL (Xilinx)	P2P connection, single lane	Custom
4	PCIe x4 (lane 0)	1 or 4 lanes	AMC.1
5	PCIe x4 (lane 1)		
6	PCIe x4 (lane 2)		
7	PCIe x4 (lane 3)		
8	LLL (Xilinx)	P2P connection, single lane	Custom
9	LLL (Xilinx)	P2P connection, single lane	Custom
10	LLL (Xilinx)	P2P connection, single lane	Custom
11	LLL (Xilinx)	P2P connection, single lane	Custom
12	LLL (Xilinx)	P2P connection, single lane	Custom
13	LLL (Xilinx)	P2P connection, single lane	Custom
14	LLL (Xilinx)	P2P connection, single lane	Custom
15	LLL (Xilinx)	P2P connection, single lane	Custom
17_RxD	BusDClock	Bidirectional	Custom
17_TxD	BusData	Bidirectional	Custom
18_RxD	StartTrigger	Bidirectional	Custom
18_TxD	PreTrigger	Bidirectional	Custom
19_RxD	RESET (AppTrigger)	Bidirectional	Custom
19_TxD	INTERLOCK0 Receiver/Transmitter	Input / Bidirectional	Custom
20_RxD	INTERLOCK1 Receiver/Transmitter	Input / Bidirectional	Custom
20_TxD	INTERLOCK2 Receiver/Transmitter	Bidirectional	Custom
TCLKA	f = 108 MHz	Input	General purpose Fast clock
TCLKB	f = 4.514 MHz	Input	General purpose Slow clock
FCLKA	f = 100 MHz	Input	Synchronization clock for PCIe
N/A	JTAG	Voltage levels translated to 3.3V (output)	JTAG chain for programmable devices
N/A	IPMI	With pull-up	IPMI for MMC (SCL/SDA)
N/A	PS0, PS1	With pull-up and low-pass-filter	Presence detection

Port	Signal	Characteristic	Description
N/A	GA0 / GA1 / GA2	With pull-up controlled by MMC	Geographical address
N/A	Enable_n	With pull-up	Enable
N/A	MP +3V3	0.15A / 150µF max.	Management power
N/A	PP +12V	7.4A / 800µF max.	Payload Power

4.2 RTM Channel Definition

Table 6: RTM Channel Definition

Channel	Signal	Characteristic	Description
J30 Zone3 Connector			
J30-3A/3B	Clock (f = configurable)	LVDS / output	General purpose clock from PLL Generated by AMC
J30-4A/4B	Clock TCKLA	LVDS / output	TCLKA from AMC backplane From MCH
J30-3C/3D	Clock (f = 81.25 / 162.5 MHz)	LVDS / input	General purpose clock derived from MO Generated by RTM
J30-3E/3F	nc	LVDS / output	-
J30-4C/4D	Interlock 0	LVDS / output	Non-programmable interlock logic Hardwired to MLVDS bus
J30-4E/4F	Interlock 1	LVDS / output	Non-programmable interlock logic Hardwired to MLVDS bus
J30-5A to 10F	Digital I/Os	LVDS / programmable via FPGA	General purpose digital I/Os Clock capable pins: 5A/5B, 6A/6B, 9A/9B, 10A/10B
J31 Zone 3 Connector			
J31-1A-6F, 7A-8B	Digital I/Os	LVDS / programmable via FPGA	General purpose digital I/Os Clock capable pins: 7A/7B, 8A/8B
J31-10C/10D/10E/10F	LLL (Xilinx GTX)	CML (according to Xilinx spec.)	LLL to FPGA Channel 0
J31-9C/9D/9E/9F	LLL (Xilinx GTX)	CML (according to Xilinx spec.)	LLL to FPGA Channel 1
J31-8C/8D/8E/8F	LLL (Xilinx GTX)	CML (according to Xilinx spec.)	LLL to FPGA Channel 2

Channel	Signal	Characteristic	Description
J31-7C/7D/7E/7F	LLL (Xilinx GTX)	CML (according to Xilinx spec.)	LLL to FPGA Channel 3
J31-9A/9B	Clock (Xilinx GTX)	LVDS / input	Reference clock for GTX transceiver Generated by RTM, connected to GTX tile
J31-10A/10B	Clock (Xilinx GTX)	LVDS / output	Reference clock for GTX transceiver Generated by AMC, output from PLL
IPMI Signals			
J30-1A/1B/2A/2B	PP +12V	RTM power supply	Payload power 3A max.
J30-2C	MP +3V3	RTM power supply	Management power 30 mA max.
J30-1C	RTM_Presence	LVCMOS (3.3V)	Presence detection (negative) MMC
J30-1D/2D	I²C	LVCMOS (3.3V)	MAIN IPMI bus (SCL/SDA) MMC
J30-1E/1F/2E/2F	JTAG	LVCMOS (3.3V)	JTAG signals for FPGA and PROM Switch shorting TDO/TDI controlled my MMC

4.3 Front Panel & LEDs

The **NAMC-TCK7** is equipped with the standard AMC LEDs and additionally features two indicator LEDs at each SFP+-Bay. For further explanation see table below.

Figure 5: NAMC-TCK7 – Front Panel

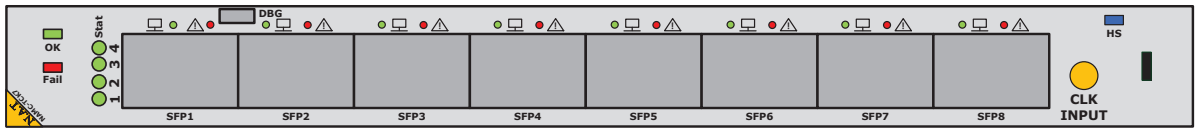


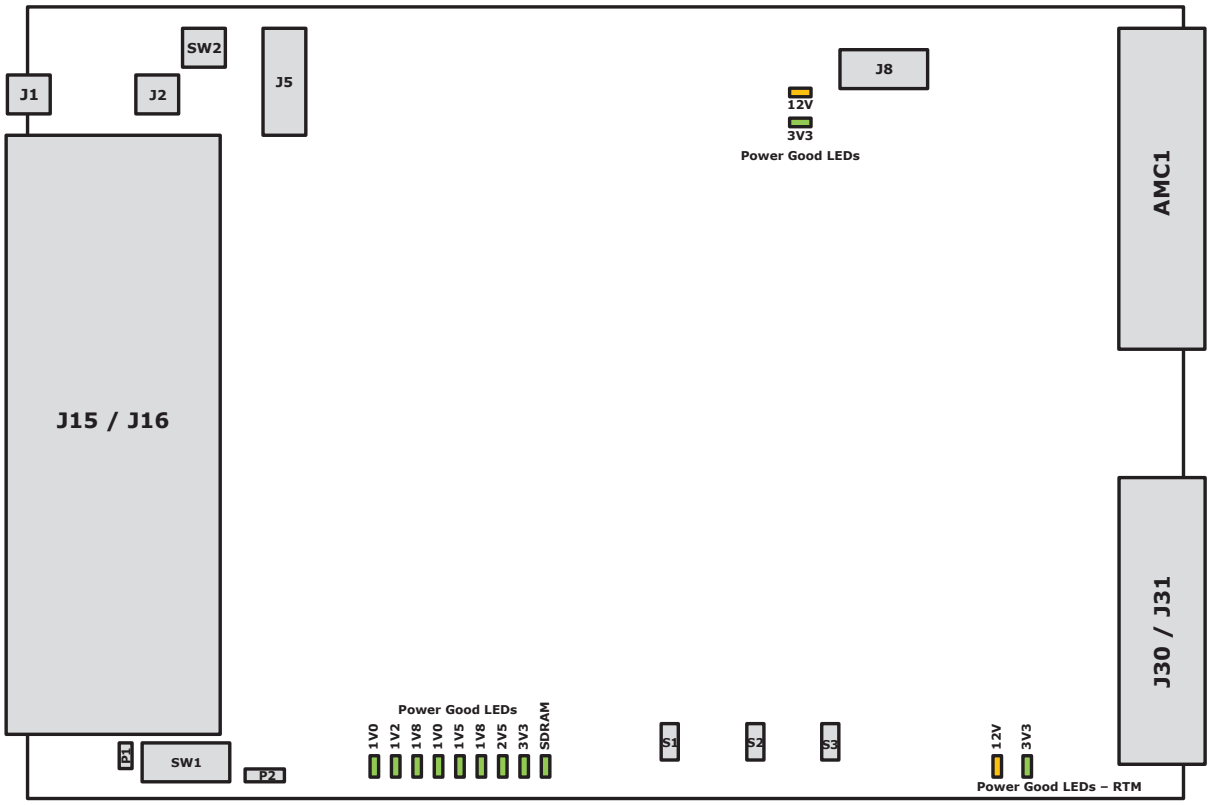
Table 7: LED Description

LED	Colour	Function	Control
SFP+1..8	green	Link presence	FPGA
SFP+1..8	red	Fault indication	FPGA
OK	green	Board status	IPMI
Fail	red	Board fault indication	IPMI
HS	blue	Hot-Swap status	IPMI
Stat1..4	green	Application free use	FPGA

4.4 Connectors, Switches and on-board LEDs

The following figure shows a connector diagram of the **NAMC-TCK7**.

Figure 6: NAMC-TCK7 – Connector Diagram



4.4.1 AMC1: AMC Connector

Table 8: AMC1: AMC Connector – Pin-Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	GND	GND	170
2	VCC+12V	TDI	169
3	PS1	TDO	168
4	VCC+3V3_MP	TRST’	167
5	GA0	TMS	166
6	RSRVD6	TCK	165
7	GND	GND	164
8	RSRVD8	AMC_INTERLOCK2_P	163
9	VCC+12V	AMC_INTERLOCK2_N	162
10	GND	GND	161
11	AMC_LLL0_TX_P	AMC_INTERLOCK1_P	160
12	AMC_LLL0_TX_N	AMC_INTERLOCK1_N	159
13	GND	GND	158
14	AMC_LLL0_RX_P	AMC_INTERLOCK0_P	157
15	AMC_LLL0_RX_N	AMC_INTERLOCK0_N	156
16	GND	GND	155
17	GA1	AMC_CRYO_OK_P	154
18	VCC+12V	AMC_CRYO_OK_N	153
19	GND	GND	152
20	AMC_LLL1_TX_P	AMC_CLK_AUX_P	151
21	AMC_LLL1_TX_N	AMC_CLK_AUX_N	150
22	GND	GND	149
23	AMC_LLL1_RX_P	AMC_TRGREADOUT_P	148
24	AMC_LLL1_RX_N	AMC_TRGREADOUT_N	147
25	GND	GND	146
26	GA2	AMC_TRGEND_P	145
27	VCC+12V	AMC_TRGEND_N	144
28	GND	GND	143
29	AMC_LLL2_TX_P	AMC_TRGSTART_P	142
30	AMC_LLL2_TX_N	AMC_TRGSTART_N	141
31	GND	GND	140
32	AMC_LLL2_RX_P	TCLKD_P	139
33	AMC_LLL2_RX_N	TCLKD_N	138
34	GND	GND	137
35	AMC_LLL3_TX_P	TCLKC_P	136
36	AMC_LLL3_TX_N	TCLKC_N	135
37	GND	GND	134
38	AMC_LLL3_RX_P	AMC_LLL15_TX_P	133
39	AMC_LLL3_RX_N	AMC_LLL15_TX_N	132
40	GND	GND	131
41	ENABLE_N	AMC_LLL15_RX_P	130
42	VCC+12V	AMC_LLL15_RX_N	129
43	GND	GND	128
44	AMC_PCIE1_TX_P	AMC_LLL14_TX_P	127
45	AMC_PCIE1_TX_N	AMC_LLL14_TX_N	126

Pin #	AMC-Signal	AMC-Signal	Pin #
46	GND	GND	125
47	AMC_PCIE1_RX_P	AMC_LLL14_RX_P	124
48	AMC_PCIE1_RX_N	AMC_LLL14_RX_N	123
49	GND	GND	122
50	AMC_PCIE2_TX_P	AMC_LLL13_TX_P	121
51	AMC_PCIE2_TX_N	AMC_LLL13_TX_N	120
52	GND	GND	119
53	AMC_PCIE2_RX_P	AMC_LLL13_RX_P	118
54	AMC_PCIE2_RX_N	AMC_LLL13_RX_N	117
55	GND	GND	116
56	SCL_L	AMC_LLL12_TX_P	115
57	VCC+12V	AMC_LLL12_TX_N	114
58	GND	GND	113
59	AMC_PCIE3_TX_P	AMC_LLL12_RX_P	112
60	AMC_PCIE3_TX_N	AMC_LLL12_RX_N	111
61	GND	GND	110
62	AMC_PCIE3_RX_P	AMC_LLL11_TX_P	109
63	AMC_PCIE3_RX_N	AMC_LLL11_TX_N	108
64	GND	GND	107
65	AMC_PCIE4_TX_P	AMC_LLL11_RX_P	106
66	AMC_PCIE4_TX_N	AMC_LLL11_RX_N	105
67	GND	GND	104
68	AMC_PCIE4_RX_P	AMC_LLL10_TX_P	103
69	AMC_PCIE4_RX_N	AMC_LLL10_TX_N	102
70	GND	GND	101
71	SDA_L	AMC_LLL10_RX_P	100
72	VCC+12V	AMC_LLL10_RX_N	99
73	GND	GND	98
74	TCLK_A_P	AMC_LLL9_TX_P	97
75	TCLK_A_N	AMC_LLL9_TX_N	96
76	GND	GND	95
77	TCLK_B_P	AMC_LLL9_RX_P	94
78	TCLK_B_N	AMC_LLL9_RX_N	93
79	GND	GND	92
80	FCLK_P	AMC_LLL8_TX_P	91
81	FCLK_N	AMC_LLL8_TX_N	90
82	GND	GND	89
83	PS0	AMC_LLL8_RX_P	88
84	VCC+12V	AMC_LLL8_RX_N	87
85	GND	GND	86

4.4.2 J1: Reference Clock Input

SMB Connector J1 features a reference clock input.

Table 9: J1: Reference Clock Input – Pin Assignment

Pin #	Signal	Signal	Pin #
1	RF_Ref_CLK_IN	GND	2

4.4.3 J2: MMC JTAG Header

Pin Header J2 connects to the JTAG-programming-port of the Atmel µC device.

Table 10: J2: MMC JTAG Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	MMC_TCK	GND	2
3	MMC_TDO	VCC+3V3_MMC	4
5	MMC_TMS	MMC_RESET_N	6
7	nc	nc	8
9	MMC_TDI	GND	10

4.4.4 J5: Main JTAG Header

Pin Header J5 offers a standard XILINX programming interface to access the FPGA and CPLD via JTAG.

Table 11: J5: Main JTAG Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	VCC+3V3	2
3	GND	JTAG_CONN_TMS	4
5	GND	JTAG_CONN_TCK	6
7	GND	JTAG_CONN_TDO	8
9	GND	JTAG_CONN_TDI	10
11	GND	nc	12
13	GND	nc	14

4.4.5 J8: Power Supply Debug Connector

Pin Header J8 features a power supply option if the **NAMC-TCK7** is operated outside a chassis.

Table 12: J8: Power Supply Debug Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	VCC+12V	GND	2
3	VCC+3V3	-	-

4.4.6 J15/16: SFP Connectors

Connectors J15/J16 offer low-latency connections via optical fibre.

Table 13: J3: SFP Connector J15/J16 – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	TX_FAULT	2
3	TX_DISABLE	SDA	4
5	SCL	MOD_ABS	6
7	RS0	RX_LOS	8
9	RS1	GND	10
11	GND	RX_N	12
13	RX_P	GND	14
15	VCCR	VCCT	16
17	GND	TX_P	18
19	TX_N	GND	20

4.4.7 J30: RTM Connector

Table 14: J30: RTM Connector – Pin-Assignment

	a	b	ab	c	d	cd	e	f	ef
1	PWR+12V	PWR+12V	GND	MP+3.3V	RTM_SDA	GND	TCKL	TDO	GND
2	PWR+12V	PWR+12V	GND	GND	RTM_SCL	GND	TDI	TMS	GND
3	AMC_CLK_P	AMC_CLK_N	GND	RTM_CLK_P	RTM_CLK_N	GND	nc	nc	GND
4	AMC_TCLK_P	AMC_TCLK_N	GND	INT_0_P	INT_0_N	GND	INT_1_P	INT_1_N	GND
5	IO1_CC_P	IO1_CC_N	GND	IO2_P	IO2_N	GND	IO3_P	IO3_N	GND
6	IO4_CC_P	IO4_CC_N	GND	IO5_P	IO5_N	GND	IO6_P	IO6_N	GND
7	IO7_P	IO7_N	GND	IO8_P	IO8_N	GND	IO9_P	IO9_N	GND
8	IO10_P	IO10_N	GND	IO11_P	IO11_N	GND	IO12_P	IO12_N	GND
9	IO13_CC_P	IO13_CC_N	GND	IO14_P	IO14_N	GND	IO15_P	IO15_N	GND
10	IO16_CC_P	IO16_CC_N	GND	IO17_P	IO17_N	GND	IO18_P	IO18_N	GND

4.4.8 J31: RTM Connector

Table 15: J31: RTM Connector – Pin-Assignment

	a	b	ab	c	d	cd	e	f	ef
1	IO1_P	IO1_N	GND	IO2_P	IO2_N	GND	IO3_P	IO3_N	GND
2	IO4_P	IO4_N	GND	IO5_P	IO5_N	GND	IO6_P	IO6_N	GND
3	IO7_P	IO7_N	GND	IO8_P	IO8_N	GND	IO9_P	IO9_N	GND
4	IO10_P	IO10_N	GND	IO11_P	IO11_N	GND	IO12_P	IO12_N	GND
5	IO13_P	IO13_N	GND	IO14_P	IO14_N	GND	IO15_P	IO15_N	GND
6	IO16_P	IO16_N	GND	IO17_P	IO17_N	GND	IO18_P	IO18_N	GND
7	IO19_CC_P	IO19_CC_N	GND	MGT3_TX_P	MGT3_TX_N	GND	MGT3_RX_P	MGT3_RX_N	GND
8	IO20_CC_P	IO20_CC_N	GND	MGT2_TX_P	MGT2_TX_N	GND	MGT2_RX_P	MGT2_RX_N	GND
9	RTM_MGT_P	RTM_MGT_N	GND	MGT1_TX_P	MGT1_TX_N	GND	MGT1_RX_P	MGT1_RX_N	GND
10	AMC_MGT_P	AMC_MGT_N	GND	MGT0_TX_P	MGT0_TX_N	GND	MGT0_RX_P	MGT0_RX_N	GND

4.4.9 P1: MMC Debug Header

Shortening the Pins of P1 enables the MMC for operation outside a chassis – for debugging purposes only.

4.4.10 P2: JTAG Chain Header

The configuration of JTAG Chain Header P2 determines which device is addressed.

Pin 1-2 connected – FPGA
Pin 2-3 connected – CPLD

4.4.11 S1: MMC Reset Switch

S1 resets the MMC.

4.4.12 S2: FPGA Reset Switch

S2 resets the FPGA.

4.4.13 S3: FPGA Configuration Switch

S3 reloads the FPGA.

4.4.14 SW1: FPGA Configuration Switch

This DIP switch is connected to FPGA Bank17 pins and can be used for any FPGA design specific functionality.

Table 16: SW1 DIP-Switch Configuration

	ON	OFF
SW1-1	tbd	tbd
SW1-2	tbd	tbd
SW1-3	tbd	tbd
SW1-4	tbd	tbd
SW1-5	tbd	tbd
SW1-6	tbd	tbd
SW1-7	tbd	tbd
SW1-8	tbd	tbd

4.4.15 SW2: Hot Swap Switch

Switch SW2 is used to support Hot-Swapping of the module. It conforms to PICMG AMC.0.

5 Board Specification

Table 17: NAMC-TCK7 – Features – Overview

FPGA	XILINX Kintex-7 FPGA (XC7K355T or XC7420T)
AMC-Module	Advanced Mezzanine Card, double width, mid-size with full-size-option
RAM	DDR3 SDRAM (256M x 64 bit)
PROM	QSPI FLASH (2x 256 Mbit)
Firmware	na
Power Consumption	12V / 6.5A
Operating Temperature	0°C – +50°C with forced cooling
Storage Temperature	-40°C - +90°C
Humidity	5% – 90% rh non-condensing
Standards compliance	AMC.0, AMC.1, AMC.2, MTCA.4 IMPI V2.0 MMC V1.0 compatible

6 Installation

6.1 Safety Note

To ensure proper functioning of the **NAMC-TCK7** during its usual lifetime take the following precautions before handling the board.

CAUTION
Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime!

- Before installing or uninstalling the **NAMC-TCK7** read this installation section
- Before installing or uninstalling the **NAMC-TCK7**, read the Installation Guide and the User's Manual of the carrier board used, or of the µTCA system the board will be plugged into.
- Before installing or uninstalling the **NAMC-TCK7** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps
  - Finally turn on or off the power if necessary.
  - Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAMC-TCK7** is connected to the carrier board or to the µTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

6.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements!

6.2.1 Requirements

The installation requires only
- an ATCA carrier board, or a µTCA backplane for connecting the **NAMC-TCK7** power supply
- cooling devices

6.2.2 Power supply

The power supply for the **NAMC-TCK7** must meet the following specifications:
- required for the module:
  - +12V / 6.5A max.

6.2.3 Automatic Power Up

In the following situations the **NAMC-TCK7** will automatically be reset and proceed with a normal power up:
- The voltage sensor generates a reset
  - when +12V voltage level drops below 8V
  - when +3.3V voltage level drops below 3.08V
- The carrier board / backplane signals a PCIe Reset.

6.3 Statement on Environmental Protection

6.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

6.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

6.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

6.3.4 Product Safety

The board complies with EN60950 and UL1950.

6.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

7 Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1] XILINX 7 Series FPGAs Data Sheet, DS180 (v2.6) 02/2018
[2] XILINX XC2C256 CoolRunner-II CPLD, DS094 (v3.2) 03/2007

Appendix B: Document's History

Revision	Date	Description	Author
1.0	21.06.2018	Initial Release	se
1.1	11.09.2018	Block diagram updated Information on GTX-Transceiver-Assignment added Minor changes on layout	se