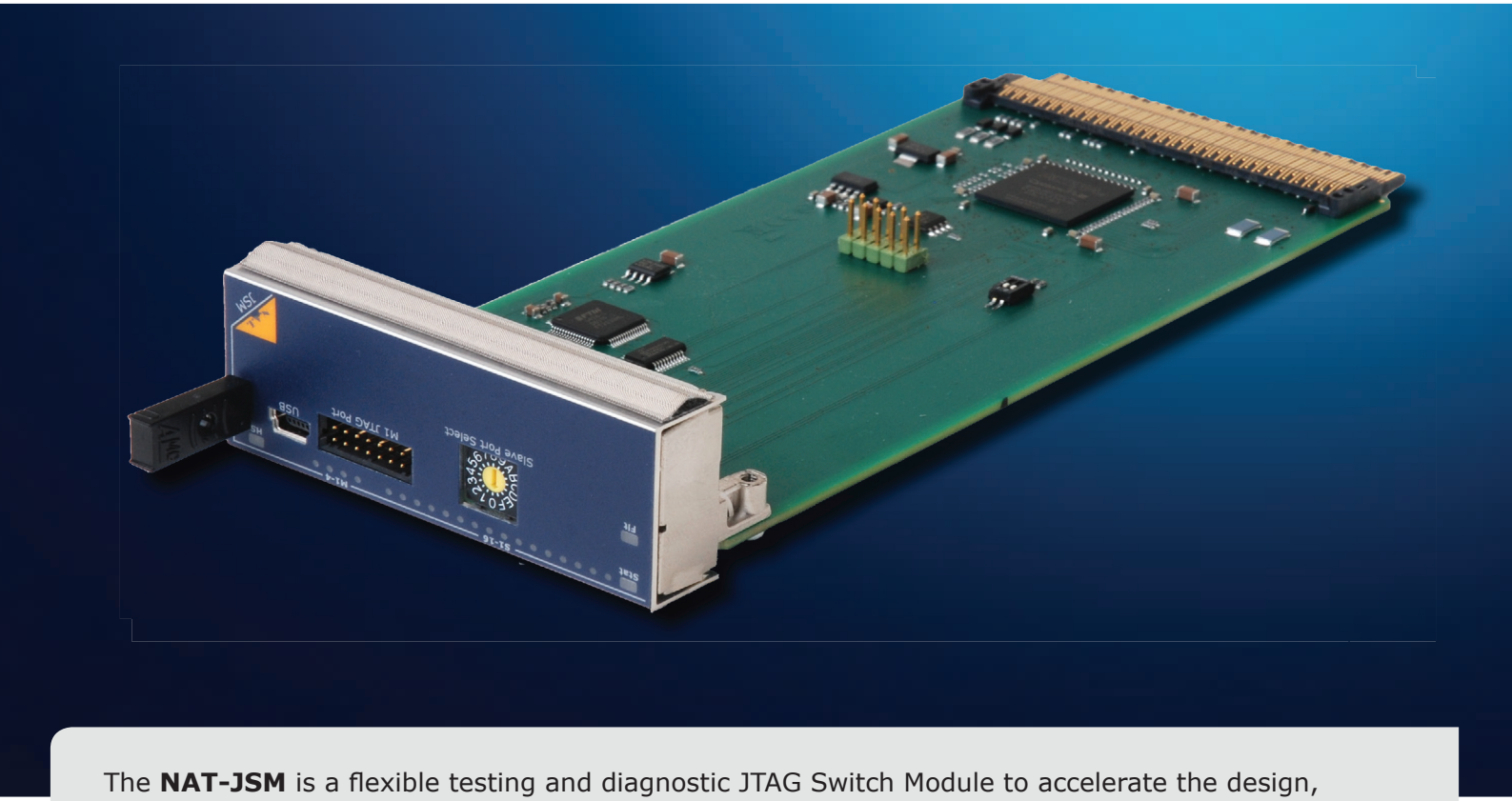
NAT-JSM JTAG Switch

Testing & Diagnostics Module



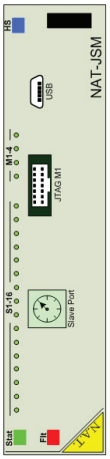
The **NAT-JSM** is a flexible testing and diagnostic JTAG Switch Module to accelerate the design, prototyping and operation of your MicroTCA (MTCA) embedded computing system. It provides JTAG vector testing of all slots in a system using just one module. By default, the NAT-JSM automatically arbitrates the JTAG master port, the slave port is selected by the TAP controller (default) or by a rotary switch or a web interface. You can configure the NAT-JSM manually using the onboard FPGA through the front panel or the NAT-MCH to suit almost any existing JSM system connector, as long as it is based on the AMC connector layout. The module can detect whether it has been inserted into an AMC, MCH or JSM slot and only turns on its output drivers if it detects a JSM slot.

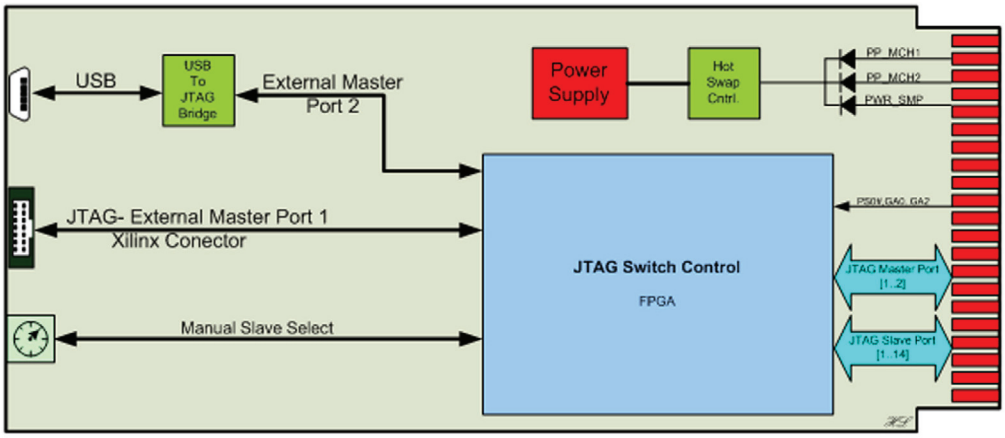
Key features

- JTAG download via MCH through Ethernet
- JTAG programming connector at front panel
- Automatic arbitration between JTAG Masters
- Overrule of automatic operation and dedicated selection of JTAG target by front panel elements
- Target selection through JTAG information
- Multiple JSM pinout configurations via FPGA

Technical Data

NAT-JSM





Overview

The **NAT-JSM** from N.A.T. provides a JTAG interface to all slots in a MicroTCA system using just one module to provide prototyping/debugging and software updates. Its flexible design makes it compatible with most MicroTCA systems that provide a JSM slot.

It can be configured using the onboard FPGA through the front panel to suit almost any existing JSM system connector, as long as it is based on the AMC connector layout.

There are four arbitrated master ports and the NAT-JSM supports up to 16 secondary ports. The module provides transparent communication between the master and a selected secondary port.

The NAT-JSM module front panel features a standard JTAG programming header and mini USB connector for maximum compatibility and to improve the flexibility of your design process.

A hexadecimal rotary switch on the front panel enables you to select the programming target when using one of these interfaces, providing a manual override of the automatic arbitration of the JTAG slave. The same can be achieved by configuring the NAT-JSM through the web interafce of the NAT-MCH.

You can also program the NAT-JSM using a server side application on the NAT-MCH, which supports the Xilinx Virtual Cable (XVC) protocol as used by the Xilinx Vivado or ISE design suites.

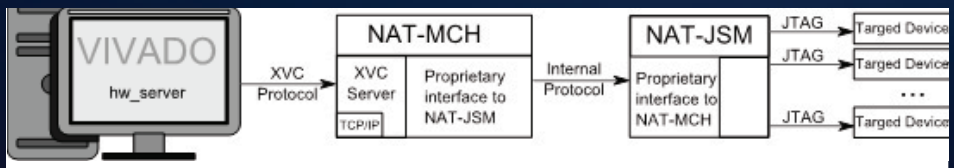
Front Panel

On the front panel, 4 green LEDs (M1-M4) show the selected JTAG master port and 16 green LEDs (S1-S16) indicate the chosen JTAG slave port.

The front panel module also includes standard AMC LEDs consisting of a red fault indication LED, a general purpose status LED and the hot-swap handle with the corresponding blue LED.

The fault indication LED turns on if a fault condition occurs. When the fault condition clears, the LED switches off again.

The general purpose LED will glow steady green when in idle/ready state, blink green during data transfer and orange if a JTAG failure occurs.



XVC Topology for Programming the NAT-JSM from the NAT-MCH

Key Features

Physical Dimemsions

- Single-width AMC module: width 73.5 mm (2.89 in), depth: 180.6 mm (7.11 in)

Subsystem Processor

- Altera Cyclone® III FPGA

Interface: Backplane

- **TCP/IP:** Protocol as used by the Xilinx Vivado or ISE design suites supports the XVC protocol, which allows JTAG commands to pass over IP to an embedded system so that a target Xilinx FPGA can be programmed and/or debugged. The NAT-MCH parses the IP packets with a TCP/IP connection and converts the packets into JTAG commands. After the packets are processed, the NAT-MCH communicates with the NAT-JSM over an internal protocol. The NAT-JSM switches the connection to the target device and provides logical connection between the XVC server and the target FPGA.

Interfaces: Front panel

- **JTAG Header:** The NAT-JSM provides a XILINX compatible 14-pin programming header on the front panel. With a standard XILINX programming adapter, you can program or debug the resources in a MTCA system. The Interface has been tested successfully with the Xilinx Platform Cable USB II. You select the programming target using the rotary switch on the front panel or through the web interface of the NAT-MCH.
- **Mini USB:** A mini USB connector on the front panel provides a direct connection to the on-board USB-to-JTAG bridge for common programming adapters from various vendors. To use this programming interface, the software driver of the respective tool should support programming interfaces based on the FTDI FT2232 USB-to-JTAG chip. The interface has been tested successfully with Lattice Diamond Programmer 3.0. You select the programming target using the rotary switch on the front panel or through the web interface of the NAT-MCH.

Environmental Conditions

Temperature (operating):

- 0ºC to +50ºC with forced air cooling

Temperature (storage):

- -40ºC to +85ºC

Relative Humidity:

- 10% to 90% at +55ºC (non-condensing)

Power Consumption

- Power is to be supplied through the backplane connector, the onboard power converter has a range from +5V to +12V. Current draw is not more than 200mA.

Standard Compliance

- µTCA.0 Revision 1