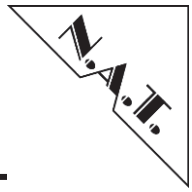
NAMC-ZYNQ-FMC
FMC AMC Module
Technical Reference Manual V1.2
HW Revision 1.x

powerBridge Computer

Ehlbeek 15a
30938 Burgwedel
fon 05139-9980-0
fax 05139-9980-49

www.powerbridge.de
info@powerbridge.de



The NAMC-ZYNQ-FMC has been designed by:

N.A.T. GmbH
Konrad-Zuse-Platz 9
53227 Bonn

Phone: +49 / 228 / 965 864 - 0

Internet: http://www.nateurope.com

Disclaimer

The following documentation, compiled by N.A.T. GmbH (henceforth called N.A.T.), represents the current status of the product´s development. The documentation is updated on a regular basis. Any changes which might ensue, including those necessitated by updated specifications, are considered in the latest version of this documentation. N.A.T. is under no obligation to notify any person, organization, or institution of such changes or to make these changes public in any other way.

We must caution you, that this publication could include technical inaccuracies or typographical errors.

N.A.T. offers no warranty, either expressed or implied, for the contents of this documentation or for the product described therein, including but not limited to the warranties of merchantability or the fitness of the product for any specific purpose.

In no event will N.A.T. be liable for any loss of data or for errors in data utilization or processing resulting from the use of this product or the documentation. In particular, N.A.T. will not be responsible for any direct or indirect damages (including lost profits, lost savings, delays or interruptions in the flow of business activities, including but not limited to, special, incidental, consequential, or other similar damages) arising out of the use of or inability to use this product or the associated documentation, even if N.A.T. or any authorized N.A.T. representative has been advised of the possibility of such damages.

The use of registered names, trademarks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations (patent laws, trade mark laws, etc.) and therefore free for general use. In no case does N.A.T. guarantee that the information given in this documentation is free of such third-party rights.

Neither this documentation nor any part thereof may be copied, translated, or reduced to any electronic medium or machine form without the prior written consent from N.A.T. GmbH.

This product (and the associated documentation) is governed by the N.A.T. General Conditions and Terms of Delivery and Payment.

Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

Table of Contents

List of Tables

List of Figures

Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by *0x*. The following table gives a list of the abbreviations used in this document:

Table 1: List of used abbreviations

Abbreviation	Description
AMC	Advanced Mezzanine Card
ARM	Processor Architecture with reduced instruction set
ASSP	Application Specific Standard Parts
ATCA	Advanced Telecommunications Computing Architecture
BSP	Board Support Package
CPU	Central Processing Unit
DAP	Debugging Access Port
DDR (SDRAM)	Double Data Rate Synchronous Dynamic Random Access Memory
DPLL	Digital Phase Locked Loop
DSP	Digital Signal Processor
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
HPC	High Pincount Connector
I²C	Inter-Integrated Circuit
I/O	Input/Output
IPMI	Intelligent Platform Management Interface
JTAG	Joint Test Action Group
LED	Light Emitting Diode
µC	Microcontroller
µTCA / MicroTCA	Micro Telecommunications Computing Architecture
MMC	Module Management Controller
MCU	Micro Controller Unit
PCIe	Peripheral Component Interconnect (Express)
PMBUS	Power Management Bus
PL	Programmable Logic
PS	Processing System
RF	Radio Frequency
SD Card	Secure Digital Memory Card
SoC	System On A Chip
SPI (FLASH)	Serial Peripheral Interface (FLASH)
SRIO	Serial Rapid I/O
(JTAG) TAP	JTAG Test Access Port
TCXO	Temperature Compensated Crystal Oscillator
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
XAUI	10 GbE (via 4x 3.125 GB/s)

1 Introduction

The **NAMC-ZYNQ-FMC** is an AdvancedMC (AMC) featuring a Xilinx ZYNQ®-7000 FPGA and an FPGA mezzanine card (FMC) slot. This single-width, mid-size AMC is designed for data acquisition and processing applications and computing nodes.

This module combines that performance with the ability to add functionality through a wide range of off-the-shelf FMCs, including analog-to-digital and digital-to-analog converters, digital I/O, and RF modules.

The following figures show photos of the **NAMC-ZYNQ-FMC.**

Figure 1: NAMC-ZYNQ-FMC – Carrier

Figure 2: NAMC-ZYNQ-FMC – Carrier with Heat Sink and attached FMC

2 Overview

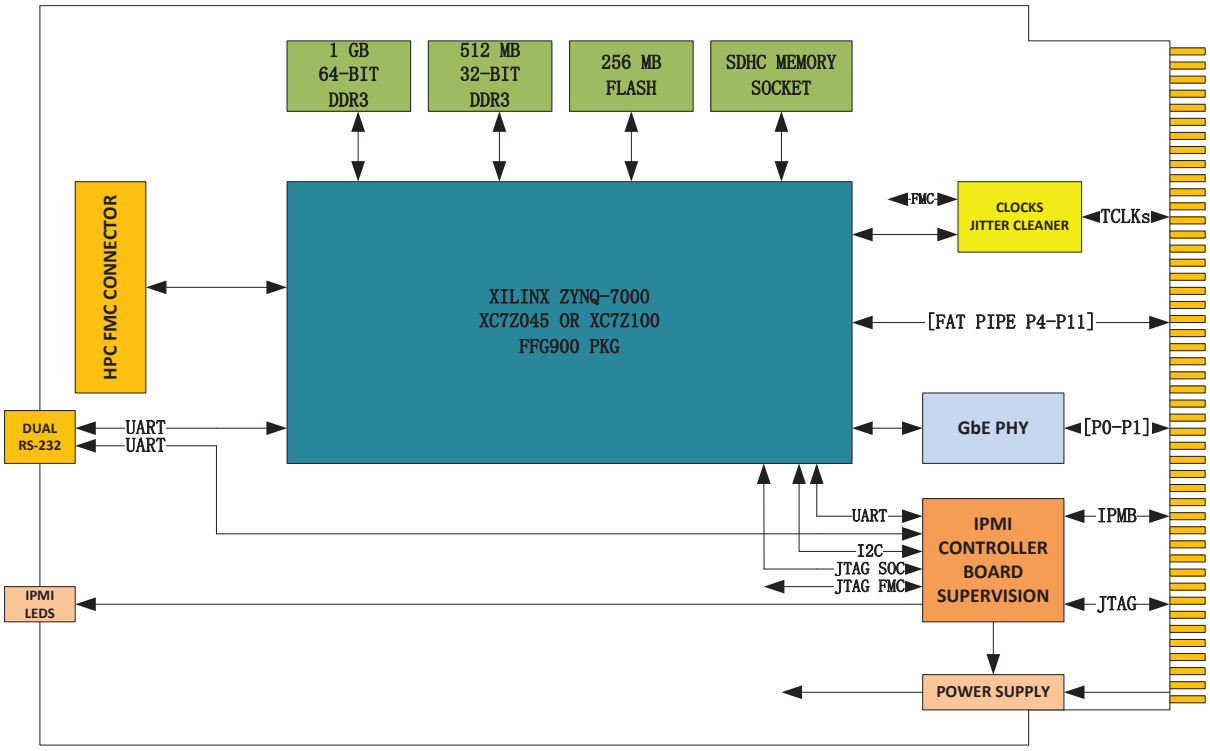
2.1 Major Features

- XILINX ZYNQ-7000 FPGA
- Dual banks of DDR3 memory
- 256MB NOR Quad SPI FLASH memory
- MicroSD Card Slot
- JTAG access over backplane
- High pin-count FMC-Slot complies with VITA 57.1
- Interfaces
- Clocks Management
- Power Management
- Board Support Package

2.2 Block Diagram

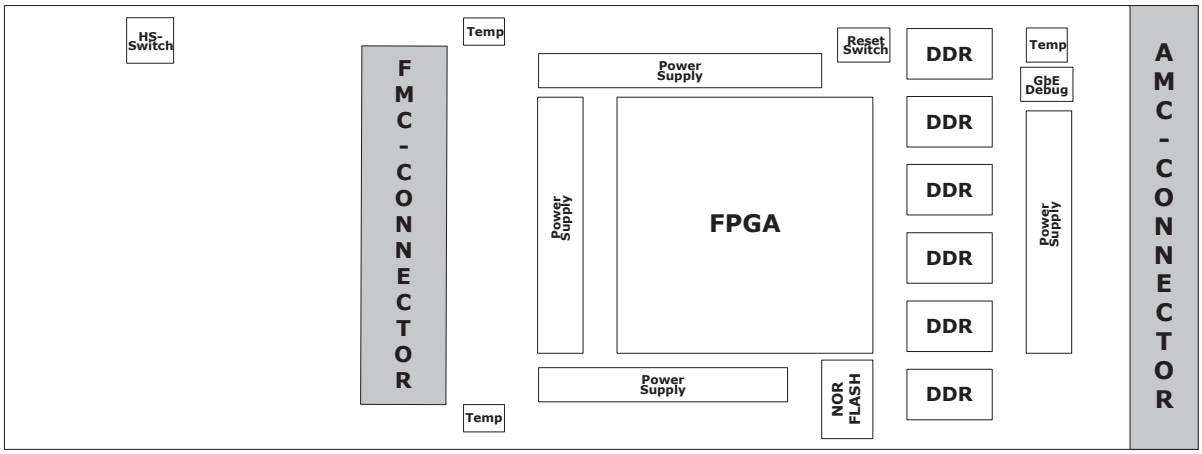
The following figure shows a detailed block diagram of the **NAMC-ZYMQ-FMC**.

Figure 3: NAMC-ZYNQ-FMC – Block Diagram

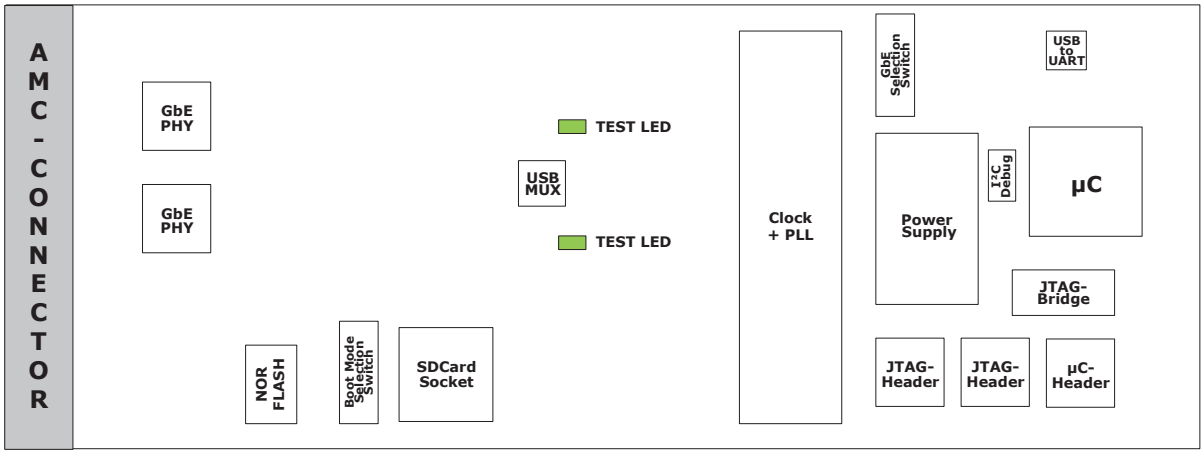


2.3 Location Diagram

Figure 4: NAMC-ZYNQ-FMC – Location Diagram



Top View



Bottom View

3 Board Features

The **NAMC-ZYNQ-FMC** can be divided into a number of functional blocks, which are described in the following paragraphs.

3.1 FPGA

The **NAMC-ZYNQ-FMC** is equipped with an on-board reconfigurable System-On-Chip XILINX ZYNQ-7000 FPGA (XC7Z045 or XC7Z100). This SoC combines an FPGA section (PL) with a dual core ARM Cortex A9 processor (PS) and thus provides the software programmability of an ARM®-based processor with the hardware programmability of an FPGA, enabling key analytics and hardware acceleration while integrating CPU, DSP, ASSP, and mixed signal functionality on a single device.

The SoC interfaces directly to the FMC-Slot via a high pin count connector and to the µTCA-Backplane offering PCIe, SRIO, or XAUI.

For further information on the XILINX ZYNQ-7000, please refer to Appendix A.

3.2 DDR3 Memory

The **NAMC-ZYNQ-FMC** features two banks of DDR3 memory:

- 1GB, 64bit wide – accessible by the SoC's FPGA section
- 512MB, 32bit wide – accessible by the SoC's processor section

This allows for large buffer sizes and queuing during processing.

3.3 SPI FLASH Memory

The **NAMC-ZYNQ-FMC** contains two Quad-SPI NOR-flash memory devices wired up in 128 MB stacked mode. This flash device can be used for storage of the FPGA bitstream, bootloader and linux file system or bare metal applications.

The device part number of the flash device is N25Q00AA13GSF40F which belongs to the Micron N25Q (1Gb, 3V) Serial NOR flash memory family.

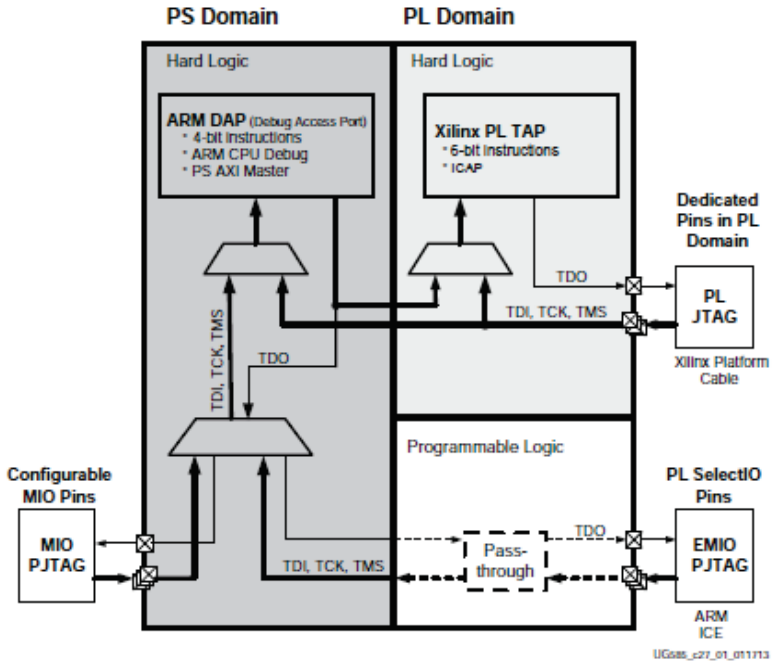
3.4 MicroSD Card Slot

A 4GB MicroSD Card can be used for storage and application.

3.5 JTAG

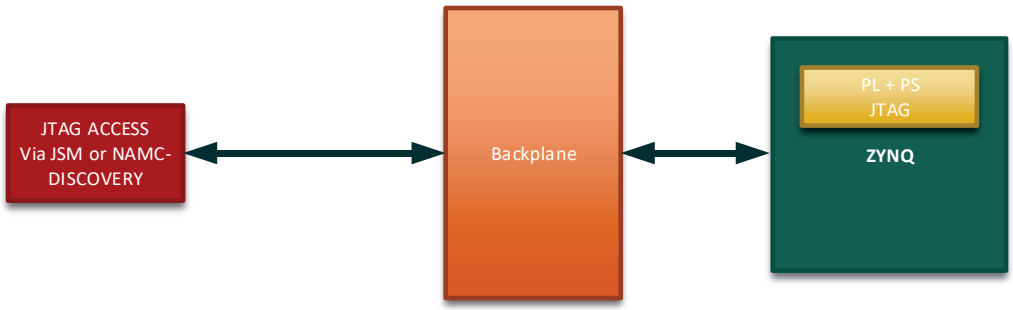
As shown on the figure below, the ZYNQ-FPGA on the **NAMC-ZYNQ-FMC** implements both an ARM debug access port (DAP) inside the Processing System (PS) as well as a standard JTAG test access port (TAP) controller inside the Programmable Logic (PL). The ARM DAP as part of ARM CoreSight debug architecture allows the user to leverage industry standard third-party debug tools.

Figure 5: NAMC-ZYNQ-FMC – JTAG System Block Diagram



The **NAMC-ZYNQ-FMC** provides debug accesses via standard JTAG (IEEE 1149.1) debug interface in the following figure.

Figure 6: NAMC-ZYNQ-FMC – JTAG Architecture Block Diagram



The **NAMC-ZYNQ-FMC** PS and PL JTAG Ports can be accessed using the MircoTCA Backplane JTAG signalling. In order to terminate the JTAG signals on the Host Side a JSM (JTAG switch module) is needed. For debugging and standalone debugging also a NAMC-DISCOVERY can be used to access the JTAG port.

3.6 Interfaces

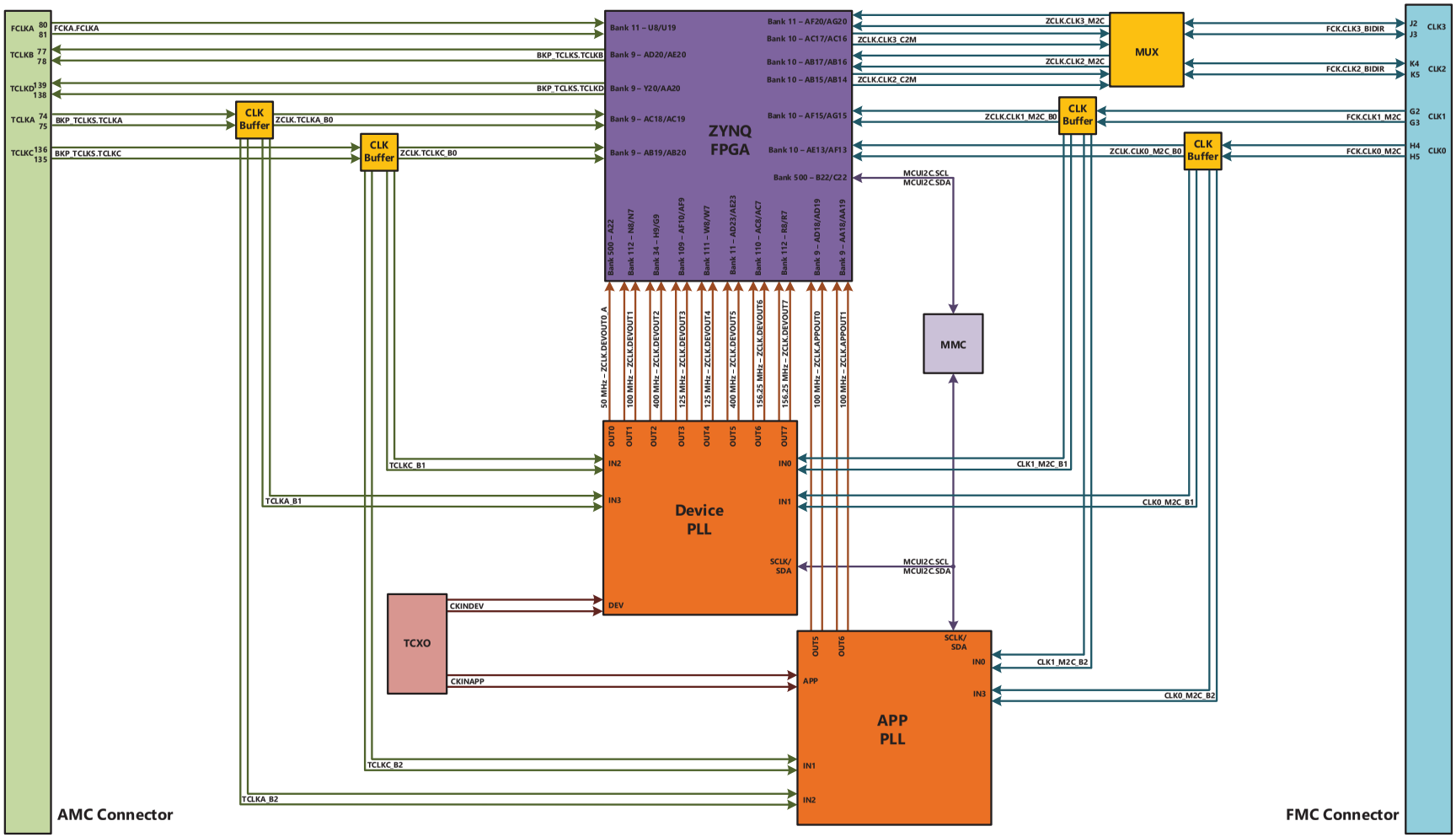
- AMC.1, AMC.2, and AMC.4 programmable via FPGA
- Dual GbE
- Telecom Clocks
- IPMI 2.0
- High-Pin Count Vita 57.1 Slot
- USB to MMC's UART
- USB to ARM's UART
- LED Status

3.7 Clocking Architecture

Various clocking signals from/to the MTCA backplane and the FMC mezzanine are connected directly to the Zynq-FPGA; others are processed by the Device PLL or APP PLL.

The clocking is illustrated in the following figure.

Figure 7: NAMC-ZYNQ-FMC – Clocking Architecture



3.8 Power Management

The **NAMC-ZYNQ-FMC** owns high efficiency PMBUS converters.

3.9 Software

The Board Support Package (BSP) of the **NAMC-ZYNQ-FMC** includes an MMC configuration, PetaLinux, and an FPGA Reference Design.

4 Hardware

4.1 AMC Port Definition

Table 2: AMC Port Definition

	Port #	AMC Port Mapping Strategy	Ports used as
Basic Connector	CLK1/TCLKA	Clocks	Reference Clock 1
	CLK2/TCLKB		Reference Clock 2
	CLK3/FCLKA		Connected to reference clock 0 input of transceiver block (MGT111)
	0	Common Options Region	1000BaseX Ethernet Channel 0
	1		1000BaseX Ethernet Channel 1
	2		Unassigned
	3		Unassigned
	4	Fat Pipes	FPGA Transceiver Port (MGT112)
	5		FPGA Transceiver Port (MGT112)
	6		FPGA Transceiver Port (MGT112)
	7		FPGA Transceiver Port (MGT112)
Extended Connector	8	Region	FPGA Transceiver Port (MGT111)
	9		FPGA Transceiver Port (MGT111)
	10		FPGA Transceiver Port (MGT111)
	11		FPGA Transceiver Port (MGT111)
	12	Extended Options Region	unassigned
	13		unassigned
	14		unassigned
	15		Unassigned
	TCLKC/D		Reference Clock 3 / 4
	17		Unassigned
	18		Unassigned
	19		Unassigned
	20		Unassigned

4.2 Front Panel and LEDs

The front panel includes the standard AMC IPMI LEDs that show hot-swap status and general card health as well as payload LEDs. It also provides a cut-out to enclose the FMC's bezel and MicroUSB connector.

Figure 8: NAMC-ZYNQ-FMC – Front Panel

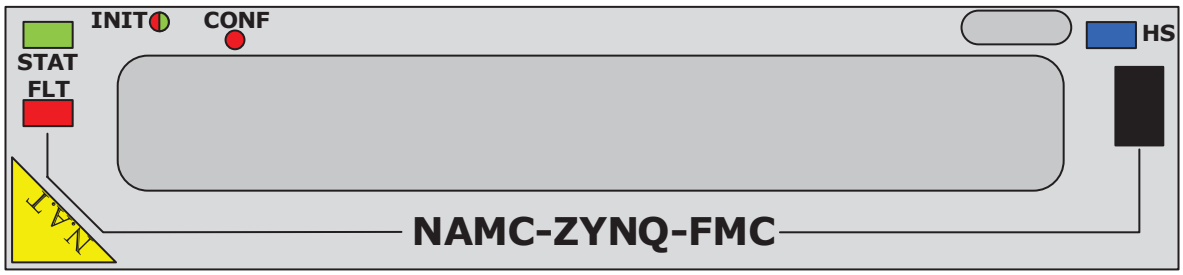
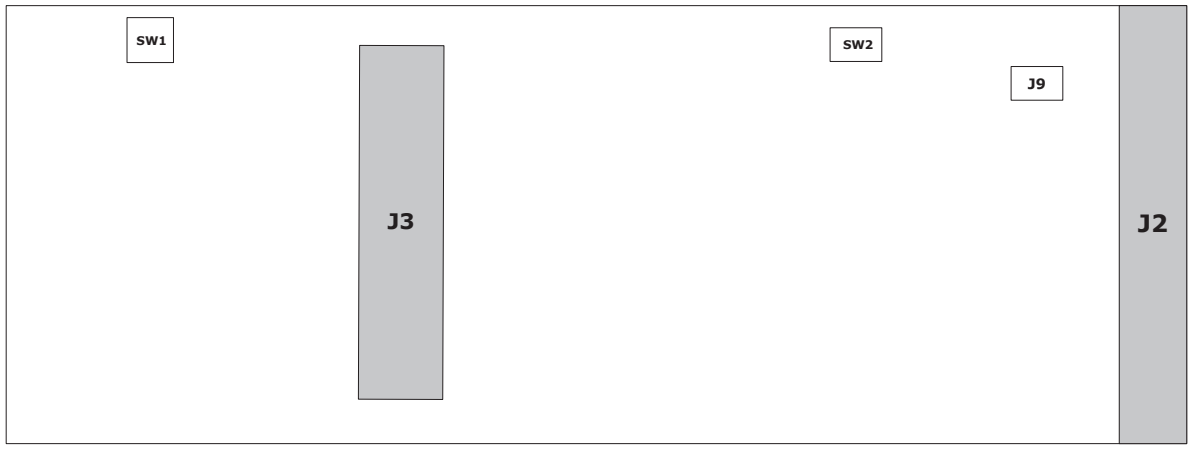


Table 3: NAMC-ZYNQ-FMC - LED Functionality

LED	Function	OFF	ON	BLINK
HS [BLUE]	IPMI	Card Active	OK to remove	Hot-Swap / Power Transitioning
STAT [GREEN]		No Payload Power	Payload Power OK	FMC VADJ Configuration Needed
FLT [RED]		No Fault	Payload Power Fault	N/A
INIT [GREEN/RED]	SoC PL	N/A	Red: Reset State / Error Green: OK	N/A
CONF [RED]		Normal Operation	Conf. Sequence Completed	N/A

4.3 Connectors and Switches

Figure 9: NAMC-ZYNQ-FMC – Connector and Switch Location – Overview



Top View

Bottom View

Please refer to the following tables to look up the connector pin assignment of the **NAMC-ZYNQ-FMC**.

4.3.1 J1: Debug Connector

J1 provides a MicroUSB connector to connect through a dual USB-to-UART Bridge to the MCU of the Module Management Controller (MMC) and to the ARM Processors of the ZYNQ.

The USB port complies with specification 2.0, full-speed (12 MHz).

Table 4: J1: Debug Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	PDI_DATA	+3.3V	2
3	nc	/PROG_ENABLE*	4
5	PDI_CLK	GND	6

4.3.2 J2: AMC Connector

Table 5: J2: AMC Connector – Pin-Assignment

Pin #	AMC-Signal	AMC-Signal	Pin #
1	GND	GND	170
2	+12V	TDI	169
3	PS1	TDO	168
4	MP	\TRS	167
5	GA0	TMS	166
6	RSRVD6	TCLK	165
7	GND	GND	164
8	RSRVD8	TX20+	163
9	+12V	TX20-	162
10	GND	GND	161
11	TX0+	RX20+	160
12	TX0-	RX20-	159
13	GND	GND	158
14	RX0+	TX19+	157
15	RX0-	TX19-	156
16	GND	GND	155
17	GA1	RX19+	154
18	+12V	RX19-	153
19	GND	GND	152
20	TX1+	TX18+	151
21	TX1-	TX18-	150
22	GND	GND	149
23	RX1+	RX18+	148
24	RX1-	RX18-	147
25	GND	GND	146
26	GA2	TX17+	145
27	+12V	TX17-	144
28	GND	GND	143
29	TX2+	RX17+	142
30	TX2-	RX17-	141

Pin #	AMC-Signal	AMC-Signal	Pin #
31	GND	GND	140
32	RX2+	TCLKD+	139
33	RX2-	TCLKD-	138
34	GND	GND	137
35	TX3+	TCLKC+	136
36	TX3-	TCLKC-	135
37	GND	GND	134
38	RX3+	TX15+	133
39	RX3-	TX15-	132
40	GND	GND	131
41	ENABL	RX15+	130
42	+12V	RX15-	129
43	GND	GND	128
44	TX4+	TX14+	127
45	TX4-	TX14-	126
46	GND	GND	125
47	RX4+	RX14+	124
48	RX4-	Rx14-	123
49	GND	GND	122
50	TX5+	TX13+	121
51	TX5-	TX13-	120
52	GND	GND	119
53	RX5+	RX13+	118
54	RX5-	RX13-	117
55	GND	GND	116
56	SCL	TX12+	115
57	+12V	TX12-	114
58	GND	GND	113
59	TX6+	RX12+	112
60	TX6-	RX12-	111
61	GND	GND	110
62	RX6+	TX11+	109
63	RX6-	TX11-	108
64	GND	GND	107
65	TX7+	RX11+	106
66	TX7-	RX11-	105
67	GND	GND	104
68	RX7+	TX10+	103
69	RX7-	TX10-	102
70	GND	GND	101
71	SDA	RX10+	100
72	+12V	RX10-	99
73	GND	GND	98
74	TCLKA+	TX9+	97
75	TCLKA-	TX9-	96
76	GND	GND	95
77	TCKLB+	RX9+	94
78	TCKLB-	Rx9-	93
79	GND	GND	92

Pin #	AMC-Signal	AMC-Signal	Pin #
80	FCLKA+	TX8+	91
81	FCLKA-	TX8-	90
82	GND	GND	89
83	PS0	RX8+	88
84	+12V	RX8-	87
85	GND	GND	86

4.3.3 FAT Pipes Pin Mapping

The following table shows the mapping of the FAT pipes from the AMC-Connector J2 to the FPGA.

Table 6: FAT pipes FPGA Pin Assignment

J2 LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
RX4+	P4.RX4_P	112	MGT	GTX	MGTXRXP3_112	P6	Module-to-Carrier Multi-Gigabit Data Signal Pair (+)
RX4-	P4.RX4_N				MGTXRXN3_112	P5	Module-to-Carrier Multi-Gigabit Data Signal Pair (-)
RX5+	P5.RX5_P	112	MGT	GTX	MGTXRXP2_112	T6	Module-to-Carrier Multi-Gigabit Data Signal Pair (+)
RX5-	P5.RX5_N				MGTXRXN2_112	T5	Module-to-Carrier Multi-Gigabit Data Signal Pair (-)
RX6+	P6.RX6_P	112	MGT	GTX	MGTXRXP1_112	U4	Module-to-Carrier Multi-Gigabit Data Signal Pair (+)
RX6-	P6.RX6_N				MGTXRXN1_112	U3	Module-to-Carrier Multi-Gigabit Data Signal Pair (-)
RX7+	P7.RX7_P	112	MGT	GTX	MGTXRXP0_112	V6	Module-to-Carrier Multi-Gigabit Data Signal Pair (+)
RX7-	P7.RX7_N				MGTXRXN0_112	V5	Module-to-Carrier Multi-Gigabit Data Signal Pair (-)
RX8+	P8.RX8_P	111	MGT	GTX	MGTXRXP3_111	AA4	Module-to-Carrier Multi-Gigabit Data Signal Pair (+)
RX8-	P8.RX8_N				MGTXRXN3_111	AA3	Module-to-Carrier Multi-Gigabit Data Signal Pair (-)

J2 LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
RX9+	P9.RX9_P	111	MGT	GTX	MGTXRXP2_111	Y6	Module-to-Carrier Multi-Gigabit Data Signal Pair (+)
RX9-	P9.RX9_N				MGTXRXN2_111	Y5	Module-to-Carrier Multi-Gigabit Data Signal Pair (-)
RX10+	P10.RX10_P	111	MGT	GTX	MGTXRXP1_111	AB6	Module-to-Carrier Multi-Gigabit Data Signal Pair (+)
RX10-	P10.RX10_N				MGTXRXN1_111	AB5	Module-to-Carrier Multi-Gigabit Data Signal Pair (-)
RX11+	P11.RX11_P	111	MGT	GTX	MGTXRXP0_111	AC4	Module-to-Carrier Multi-Gigabit Data Signal Pair (+)
RX11-	P11.RX11_N				MGTXRXN0_111	AC3	Module-to-Carrier Multi-Gigabit Data Signal Pair (-)
FCLKA+	FCKA.FCLKA_P	111	MGT	GTX	MGTREFCLK0P_111	U8	Module-to-Carrier LVDS Signal Pair (+)
FCLKA-	FCKA.FCLKA_N				MGTREFCLK0N_111	U7	Module-to-Carrier LVDS Signal Pair (-)
TX4+	P4.TX4_P	112	MGT	GTX	MGTXTXP3_112	N4	Module-to-Carrier Multi-Gigabit Data Signal Pair (+)
TX4-	P4.TX4_N				MGTXTXN3_112	N3	Module-to-Carrier Multi-Gigabit Data Signal Pair (-)

J2 LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
TX5+	P5.TX5_P	112	MGT	GTX	MGTXTXP2_112	P2	Module-to-Carrier Multi-Gigabit Data Signal Pair (+)
TX5-	P5.TX5_N				MGTXTXN2_112	P1	Module-to-Carrier Multi-Gigabit Data Signal Pair (-)
TX6+	P6.TX6_P	112	MGT	GTX	MGTXTXP1_112	R4	Module-to-Carrier Multi-Gigabit Data Signal Pair (+)
TX6-	P6.TX6_N				MGTXTXN1_112	R3	Module-to-Carrier Multi-Gigabit Data Signal Pair (-)
TX7+	P7.TX7_P	112	MGT	GTX	MGTXTXP0_112	T2	Module-to-Carrier Multi-Gigabit Data Signal Pair (+)
TX7-	P7.TX7_N				MGTXTXN0_112	T1	Module-to-Carrier Multi-Gigabit Data Signal Pair (-)
TX8+	P8.TX8_P	111	MGT	GTX	MGTXTXP3_111	V2	Module-to-Carrier Multi-Gigabit Data Signal Pair (+)
TX8-	P8.TX8_N				MGTXTXN3_111	V1	Module-to-Carrier Multi-Gigabit Data Signal Pair (-)
TX9+	P9.TX9_P	111	MGT	GTX	MGTXTXP2_111	W4	Module-to-Carrier Multi-Gigabit Data Signal Pair (+)
TX9-	P9.TX9_N				MGTXTXN2_111	W3	Module-to-Carrier Multi-Gigabit Data Signal Pair (-)
TX10+	P10.TX10_P	111	MGT	GTX	MGTXTXP1_111	Y2	Module-to-Carrier Multi-Gigabit Data Signal Pair (+)
TX10-	P10.TX10_N				MGTXTXN1_111	Y1	Module-to-Carrier Multi-Gigabit Data Signal Pair (-)
TX11+	P11.TX11_P	111	MGT	GTX	MGTXTXP0_111	AB2	Module-to-Carrier Multi-Gigabit Data Signal Pair (+)
TX11-	P11.TX11_N				MGTXTXN0_111	AB1	Module-to-Carrier Multi-Gigabit Data Signal Pair (-)

4.3.4 J3: FMC Connector

The **NAMC-ZYNQ-FMC** provides an HPC connector at J3, which is compliant with the VITA 57.2 specification. This connector provides expansion from the FPGA on the carrier board to I/O mezzanine board such as the N.A.T. FMC430x, FMC1200 or other compatible boards.

The FMC, at the opposite of the carrier, is not hot-swappable. The MMC needs to be re-configured whenever a new FMC is mounted or removed, unless the FMC is a supported N.A.T.'s FMC in which case the configuration will be automatic. The configuration of the MMC is performed through JX using the MMC's configuration application software.

NOTE:
The design loaded into the FPGA shall match the pin-out of the mounted FMC and the MMC shall has been configured correctly to use the mounted FMC, or damages to the carrier and/or mezzanine board may occur.

Damages resulting of a wrong configuration are not covered under the N.A.T. warranty so make sure of the compatibility between the FPGA image on the board and the FMC prior to mounting.

Table 7: J3: FMC Connector ROW A – Pin-Assignment

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
A1	GND	GND	--	--	--	--	--	Logic Ground
A2	DP1_M2C_P	FDP.DP1_M2C_P	109	MGT	GTX	MGTXRXP1_109	AJ8	Module-to-Carrier Multi-Gigabit Data Signal Pair 1 (+)
A3	DP1_M2C_N	FDP.DP1_M2C_N				MGTXRXN1_109	AJ7	Module-to-Carrier Multi-Gigabit Data Signal Pair 1 (-)
A4	GND	GND	--	--	--	--	--	Logic Ground
A5	GND	GND	--	--	--	--	--	Logic Ground
A6	DP2_M2C_P	FDP.DP2_M2C_P	109	MGT	GTX	MGTXRXP2_109	AG8	Module-to-Carrier Multi-Gigabit Data Signal Pair 2 (+)
A7	DP2_M2C_N	FDP.DP2_M2C_N				MGTXRXN2_109	AG7	Module-to-Carrier Multi-Gigabit Data Signal Pair 2 (-)
A8	GND	GND	--	--	--	--	--	Logic Ground
A9	GND	GND	--	--	--	--	--	Logic Ground
A10	DP3_M2C_P	FDP.DP3_M2C_P	109	MGT	GTX	MGTXRXP3_109	AE8	Module-to-Carrier Multi-Gigabit Data Signal Pair 3 (+)
A11	DP3_M2C_N	FDP.DP3_M2C_N				MGTXRXN3_109	AE7	Module-to-Carrier Multi-Gigabit Data Signal Pair 3 (-)
A12	GND	GND	--	--	--	--	--	Logic Ground
A13	GND	GND	--	--	--	--	--	Logic Ground
A14	DP4_M2C_P	FDP.DP4_M2C_P	110	MGT	GTX	MGTXRXP0_110	AH6	Module-to-Carrier Multi-Gigabit Data Signal Pair 4 (+)
A15	DP4_M2C_N	FDP.DP4_M2C_N				MGTXRXN0_110	AH5	Module-to-Carrier Multi-Gigabit Data Signal Pair 4 (-)
A16	GND	GND	--	--	--	--	--	Logic Ground
A17	GND	GND	--	--	--	--	--	Logic Ground

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
A18	DP5_M2C_P	FDP.DP4_M2C_P	110	MGT	GTX	MGTXRXP1_110	AG4	Module-to-Carrier Multi-Gigabit Data Signal Pair 5 (+)
A19	DP5_M2C_N	FDP.DP4_M2C_N				MGTXRXN1_110	AG3	Module-to-Carrier Multi-Gigabit Data Signal Pair 5 (-)
A20	GND	GND	--	--	--	--	--	Logic Ground
A21	GND	GND	--	--	--	--	--	Logic Ground
A22	DP1_C2M_P	FDP.DP1_C2M_P	109	MGT	GTX	MGTXTXP1_109	AK6	Carrier-to-Module Multi-Gigabit Data Signal Pair 1 (+)
A23	DP1_C2M_N	FDP.DP1_C2M_N				MGTXTXN1_109	AK5	Carrier-to-Module Multi-Gigabit Data Signal Pair 1 (-)
A24	GND	GND	--	--	--	--	--	Logic Ground
A25	GND	GND	--	--	--	--	--	Logic Ground
A26	DP2_C2M_P	FDP.DP2_C2M_P	109	MGT	GTX	MGTXTXP2_109	AJ4	Carrier-to-Module Multi-Gigabit Data Signal Pair 2 (+)
A27	DP2_C2M_N	FDP.DP2_C2M_N				MGTXTXN2_109	AJ3	Carrier-to-Module Multi-Gigabit Data Signal Pair 2 (-)
A28	GND	GND	--	--	--	--	--	Logic Ground
A29	GND	GND	--	--	--	--	--	Logic Ground
A30	DP3_C2M_P	FDP.DP3_C2M_P	109	MGT	GTX	MGTXTXP3_109	AK2	Carrier-to-Module Multi-Gigabit Data Signal Pair 3 (+)
A31	DP3_C2M_N	FDP.DP3_C2M_N				MGTXTXN3_109	AK1	Carrier-to-Module Multi-Gigabit Data Signal Pair 3 (-)
A32	GND	GND	--	--	--	--	--	Logic Ground
A33	GND	GND	--	--	--	--	--	Logic Ground
A34	DP4_C2M_P	FDP.DP4_C2M_P	110	MGT	GTX	MGTXTXP0_110	AH2	Carrier-to-Module Multi-Gigabit Data Signal Pair 4 (+)
A35	DP4_C2M_N	FDP.DP4_C2M_N				MGTXTXN0_110	AH1	Carrier-to-Module Multi-Gigabit Data Signal Pair 4 (-)

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
A36	GND	GND	--	--	--	--	--	Logic Ground
A37	GND	GND	--	--	--	--	--	Logic Ground
A38	DP5_C2M_P	FDP.DP5_C2M_P	110	MGT	GTX	MGTXTXP1_110	AF2	Carrier-to-Module Multi-Gigabit Data Signal Pair 5 (+)
A39	DP5_C2M_N	FDP.DP5_C2M_N				MGTXTXN1_110	AF1	Carrier-to-Module Multi-Gigabit Data Signal Pair 5 (-)
A40	GND	GND	--	--	--	--	--	Logic Ground

Table 8: J3: FMC Connector ROW B – Pin-Assignment

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
B1	CLK_DIR	FSIG.CLK_DIR	--	--	--	--	--	Set the direction of the CLK2/3_BIDIR: = 0 ➔ CLK2/3_BIDIR are driven from FMC to the Carrier = 1 ➔ CLK2/3_BIDIR are driven from the Carrier to FMC
B2	GND	GND	--	--	--	--	--	Logic Ground
B3	GND	GND	--	--	--	--	--	Logic Ground
B4	DP9_M2C_P	NC	--		--	--	--	--
B5	DP9_M2C_N	NC	--		--	--	--	--
B6	GND	GND	--	--	--	--	--	Logic Ground
B7	GND	GND	--	--	--	--	--	Logic Ground
B8	DP8_M2C_P	NC	--		--	--	--	--
B9	DP8_M2C_N	NC	--		--	--	--	--
B10	GND	GND	--	--	--	--	--	Logic Ground
B11	GND	GND	--	--	--	--	--	Logic Ground
B12	DP7_M2C_P	FDP.DP7_M2C_P	110	MGT	GTX	MGTXRXP3_110	AD6	Module-to-Carrier Multi-Gigabit Data Signal Pair 7 (+)
B13	DP7_M2C_N	FDP.DP7_M2C_N				MGTXRXN3_110	AD5	Module-to-Carrier Multi-Gigabit Data Signal Pair 7 (-)
B14	GND	GND						Logic Ground
B15	GND	GND						Logic Ground

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
B16	DP6_M2C_P	FDP.DP6_M2C_P	110	MGT	GTX	MGTXRXP2_110	AF6	Module-to-Carrier Multi-Gigabit Data Signal Pair 6 (+)
B17	DP6_M2C_N	FDP.DP6_M2C_N				MGTXRXP2_110	AF5	Module-to-Carrier Multi-Gigabit Data Signal Pair 6 (-)
B18	GND	GND						Logic Ground
B19	GND	GND						Logic Ground
B20	GBTCLK1_M2C_P	FGC.CLK1_M2C_P	110	MGT	GTX	MGTREFCLK0P_110	AA8	Module-to-Carrier Multi-Gigabit Reference Clock Pair 1 (+)
B21	GBTCLK1_M2C_N	FGC.CLK1_M2C_N				MGTREFCLK0N_110	AA7	Module-to-Carrier Multi-Gigabit Reference Clock Pair 1 (-)
B22	GND	GND	--	--	--	--	--	Logic Ground
B23	GND	GND	--	--	--	--	--	Logic Ground
B24	DP9_C2M_P	NC	--	--	--	--	--	--
B25	DP9_C2M_N	NC	--	--	--	--	--	--
B26	GND	GND	--	--	--	--	--	Logic Ground
B27	GND	GND	--	--	--	--	--	Logic Ground
B28	DP8_C2M_P	NC	--	--	--	--	--	--
B29	DP8_C2M_N	NC	--	--	--	--	--	--
B30	GND	GND	--	--	--	--	--	Logic Ground
B31	GND	GND	--	--	--	--	--	Logic Ground
B32	DP7_C2M_P	FDP.DP7_C2M_P	110	MGT	GTX	MGTXTXP3_110	AD2	Carrier-to-Module Multi-Gigabit Data Signal Pair 7 (+)
B33	DP7_C2M_N	FDP.DP7_C2M_N				MGTXTXN3_110	AD1	Carrier-to-Module Multi-Gigabit Data Signal Pair 7 (-)
B34	GND	GND	--	--	--	--	--	Logic Ground

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
B35	GND	GND	--	--	--	--	--	Logic Ground
B36	DP6_C2M_P	FDP.DP6_C2M_P	110	MGT	GTX	MGTXTXP2_110	AE4	Carrier-to-Module Multi-Gigabit Data Signal Pair 6 (+)
B37	DP6_C2M_N	FDP.DP6_C2M_N				MGTXTXN2_110	AE3	Carrier-to-Module Multi-Gigabit Data Signal Pair 6 (-)
B38	GND	GND	--	--	--	--	--	Logic Ground
B39	GND	GND	--	--	--	--	--	Logic Ground
B40	RES0	NC	--	--	--	--	--	--

Table 9: J3: FMC Connector ROW C – Pin-Assignment

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
C1	GND	GND	--	--	--	--	--	Logic Ground
C2	DP0_C2M_P	FDP.DP0_C2M_P	109	MGT	GTX	MGTXTXP0_109	AK10	Carrier-to-Module Multi-Gigabit Data Signal Pair 0 (+)
C3	DP0_C2M_N	FDP.DP0_C2M_N				MGTXTXN0_109	AK9	Carrier-to-Module Multi-Gigabit Data Signal Pair 0 (-)
C4	GND	GND	--	--	--	--	--	Logic Ground
C5	GND	GND	--	--	--	--	--	Logic Ground
C6	DP0_M2C_P	FDP.DP0_M2C_P	109	MGT	GTX	MGTXRXP0_109	AH10	Module-to-Carrier Multi-Gigabit Data Signal Pair 0 (+)
C7	DP0_M2C_N	FDP.DP0_M2C_N				MGTXRXN0_109	AH9	Module-to-Carrier Multi-Gigabit Data Signal Pair 0 (-)
C8	GND	GND	--	--	--	--	--	Logic Ground
C9	GND	GND	--	--	--	--	--	Logic Ground
C10	LA06_P	LA.LA06_P	10	VADJ	User Selected	IO_L9P_T1_DQS_10	AD14	Bank LA User Defined Signal Pair 6 (+)
C11	LA06_N	LA.LA06_N				IO_L9P_T1_DQS_10	AD13	Bank LA User Defined Signal Pair 6 (-)
C12	GND	GND	--	--	--	--	--	Logic Ground
C13	GND	GND	--	--	--	--	--	Logic Ground
C14	LA10_P	LA.LA10_P	10	VADJ	User Selected	IO_L10P_T1_10	AG12	Bank LA User Defined Signal Pair 10 (+)
C15	LA10_N	LA.LA10_N				IO_L10N_T1_10	AH12	Bank LA User Defined Signal Pair 10 (-)
C16	GND	GND	--	--	--	--	--	Logic Ground
C17	GND	GND	--	--	--	--	--	Logic Ground

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
C18	LA14_P	LA.LA14_P	10	VADJ	User Selected	IO_L5P_T0_10	AJ15	Bank LA User Defined Signal Pair 14 (+)
C19	LA14_N	LA.LA14_N				IO_L5N_T0_10	AK15	Bank LA User Defined Signal Pair 14 (-)
C20	GND	GND	--	--	--	--	--	Logic Ground
C21	GND	GND	--	--	--	--	--	Logic Ground
C22	LA18_P_CC	LA.LA18_CC_P	11	VADJ	User Selected	IO_L12P_T1_MRCC_11	AE22	Bank LA User Defined Signal Pair 18 (+) – Clock Preferable
C23	LA18_N_CC	LA.LA18_CC_N				IO_L12N_T1_MRCC_11	AF22	Bank LA User Defined Signal Pair 18 (-) – Clock Preferable
C24	GND	GND	--	--	--	--	--	Logic Ground
C25	GND	GND	--	--	--	--	--	Logic Ground
C26	LA27_P	LA.LA27_P	11	VADJ	User Selected	IO_L5P_T0_11	AH23	Bank LA User Defined Signal Pair 27 (+)
C27	LA27_N	LA.LA27_N				IO_L5N_T0_11	AH24	Bank LA User Defined Signal Pair 27 (-)
C28	GND	GND	--	--	--	--	--	Logic Ground
C29	GND	GND	--	--	--	--	--	Logic Ground
C30	SCL	FSIG.SCL	--	--	--	--	--	System Management I2C Clock
C31	SDA	FSIG.SDA	--	--	--	--	--	System Management I2C Data
C32	GND	GND	--	--	--	--	--	Logic Ground
C33	GND	GND	--	--	--	--	--	Logic Ground
C34	GA0	FSIG.GA0	--	--	--	--	--	Geographical Address bit 0
C35	12POV	12POV	--	--	--	--	--	+12 V Power Supply
C36	GND	GND	--	--	--	--	--	Logic Ground
C37	12POV	12POV	--	--	--	--	--	+12 V Power Supply

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
C38	GND	GND	--	--	--	--	--	Logic Ground
C39	3P3V	3P3V	--	--	--	--	--	+3.3 V Power Supply
C40	GND	GND	--	--	--	--	--	Logic Ground

Table 10: J3: FMC Connector ROW D – Pin-Assignment

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
D1	PG_C2M	FSIG.PG_C2M	--	--	--	--	--	To be asserted high by the Carrier when Power Supplies VADJ, 12POV and 3P3V are within tolerance.
D2	GND	GND	--	--	--	--	--	Logic Ground
D3	GND	GND	--	--	--	--	--	Logic Ground
D4	GBTCLK0_M2C_P	FGC.CLK0_M2C_P	109	MGT	GTX	MGTREFCLK0P_109	AD10	Module-to-Carrier Multi-Gigabit Reference Clock Pair 0 (+)
D5	GBTCLK0_M2C_N	FGC.CLK0_M2C_N				MGTREFCLK0N_109	AD9	Module-to-Carrier Multi-Gigabit Reference Clock Pair 0 (-)
D6	GND	GND	--	--	--	--	--	Logic Ground
D7	GND	GND	--	--	--	--	--	Logic Ground
D8	LA01_P_CC	LA.LA01_CC_P	10	VADJ	User Selected	IO_L12P_T1_MRCC_10	AF14	Bank LA User Defined Signal Pair 1 (+) – Clock Preferable
D9	LA01_N_CC	LA.LA01_CC_N				IO_L12N_T1_MRCC_10	AG14	Bank LA User Defined Signal Pair 1 (-) – Clock Preferable
D10	GND	GND	--	--	--	--	--	Logic Ground
D11	LA05_P	LA.LA05_P	10	VADJ	User Selected	IO_L16P_T2_10	AE16	Bank LA User Defined Signal Pair 5 (+)
D12	LA05_N	LA.LA05_N				IO_L16N_T2_10	AE15	Bank LA User Defined Signal Pair 5 (-)
D13	GND	GND	--	--	--	--	--	Logic Ground

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
D14	LA09_P	LA.LA09_P	10	VADJ	User Selected	IO_L8P_T1_10	AH14	Bank LA User Defined Signal Pair 9 (+)
D15	LA09_N	LA.LA09_N				IO_L8N_T1_10	AH13	Bank LA User Defined Signal Pair 9 (-)
D16	GND	GND	--	--	--	--	--	Logic Ground
D17	LA13_P	LA.LA13_P	10	VADJ	User Selected	IO_L3P_T0_DQS_10	AJ14	Bank LA User Defined Signal Pair 13 (+)
D18	LA13_N	LA.LA13_N				IO_L3N_T0_DQS_10	AJ13	Bank LA User Defined Signal Pair 13 (-)
D19	GND	GND	--	--	--	--	--	Logic Ground
D20	LA17_P_CC	LA.LA17_CC_P	11	VADJ	User Selected	IO_L13P_T2_MRCC_11	AG21	Bank LA User Defined Signal Pair 17 (+) – Clock Preferable
D21	LA17_N_CC	LA.LA17_CC_N				IO_L13N_T2_MRCC_11	AH21	Bank LA User Defined Signal Pair 17 (-) – Clock Preferable
D22	GND	GND	--	--	--	--	--	Logic Ground
D23	LA23_P	LA.LA23_P	11	VADJ	User Selected	IO_L15P_T2_DQS_11	AJ20	Bank LA User Defined Signal Pair 23 (+)
D24	LA23_N	LA.LA23_N				IO_L15N_T2_DQS_11	AK20	Bank LA User Defined Signal Pair 23 (-)
D25	GND	GND	--	--	--	--	--	Logic Ground
D26	LA26_P	LA.LA26_P	11	VADJ	User Selected	IO_L4P_T0_11	AJ23	Bank LA User Defined Signal Pair 26 (+)
D27	LA26_N	LA.LA26_N				IO_L4N_T0_11	AJ24	Bank LA User Defined Signal Pair 26 (-)
D28	GND	GND	--	--	--	--	--	Logic Ground
D29	TCK	FMC_JTAG.TCK	--	--	--	--	--	JTAG Test Clock
D30	TDI	FMC_JTAG.TDI	--	--	--	--	--	JTAG Test Data In
D31	TDO	FMC_JTAG.TDO	--	--	--	--	--	JTAG Test Data Out

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
D32	3P3VAUX	3P3VAUX	--	--	--	--	--	3.3V Management Power Supply
D33	TMS	FMC_JTAG.TMS	--	--	--	--	--	JTAG Test Mode Select
D34	TRST_L	FMC_JTAG.TRST_L	--	--	--	--	--	JTAG Test Reset
D35	GA1	FSIG.GA1	--	--	--	--	--	Geographical Address bit 0
D36	3P3V	3P3V	--	--	--	--	--	+3.3 V Power Supply
D37	GND	GND	--	--	--	--	--	Logic Ground
D38	3P3V	3P3V	--	--	--	--	--	+3.3 V Power Supply
D39	GND	GND	--	--	--	--	--	Logic Ground
D40	3P3V	3P3V	--	--	--	--	--	+3.3 V Power Supply

Table 11: J3: FMC Connector ROW E – Pin-Assignment

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
E1	GND	GND	--	--	--	--	--	Logic Ground
E2	HA01_P_CC	HA.HA01_CC_P	12	VADJ	User Selected	IO_L11P_T1_SRCC_12	AB27	Bank HA User Defined Signal Pair 1 (+) – Clock Preferable
E3	HA01_N_CC	HA.HA01_CC_N				IO_L11N_T1_SRCC_12	AC27	Bank HA User Defined Signal Pair 1 (-) – Clock Preferable
E4	GND	GND	--	--	--	--	--	Logic Ground
E5	GND	GND	--	--	--	--	--	Logic Ground
E6	HA05_P	HA.HA05_P	12	VADJ	User Selected	IO_L3P_T0_DQS_12	Y26	Bank HA User Defined Signal Pair 5 (+)
E7	HA05_N	HA.HA05_N				IO_L3N_T0_DQS_12	Y27	Bank HA User Defined Signal Pair 5 (-)
E8	GND	GND	--	--	--	--	--	Logic Ground
E9	HA09_P	HA.HA09_P	12	VADJ	User Selected	IO_L2P_T0_12	AB29	Bank HA User Defined Signal Pair 9 (+)
E10	HA09_N	HA.HA09_N				IO_L2N_T0_12	AB30	Bank HA User Defined Signal Pair 9 (-)
E11	GND	GND	--	--	--	--	--	Logic Ground
E12	HA13_P	HA.HA13_P	12	VADJ	User Selected	IO_L10P_T1_12	AD25	Bank HA User Defined Signal Pair 13 (+)
E13	HA13_N	HA.HA13_N				IO_L10N_T1_12	AE26	Bank HA User Defined Signal Pair 13 (-)
E14	GND	GND	--	--	--	--	--	Logic Ground

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
E15	HA16_P	HA.HA16_P	11	VADJ	User Selected	IO_L1P_T0_11	AJ25	Bank HA User Defined Signal Pair 16 (+)
E16	HA16_N	HA.HA16_N				IO_L1N_T0_11	AK25	Bank HA User Defined Signal Pair 16 (-)
E17	GND	GND	--	--	--	--	--	Logic Ground
E18	HA20_P	HA.HA20_P	12	VADJ	User Selected	IO_L22P_T3_12	AK27	Bank HA User Defined Signal Pair 20 (+)
E19	HA20_N	HA.HA20_N				IO_L22N_T3_12	AK28	Bank HA User Defined Signal Pair 20 (-)
E20	GND	GND	--	--	--	--	--	Logic Ground
E21	HB03_P	HB.HB03_P	13	VIO_B_M2C	User Selected	IO_L24P_T3_13	V23	Bank HB User Defined Signal Pair 3 (+)
E22	HB03_N	HB.HB03_N				IO_L24N_T3_13	W24	Bank HB User Defined Signal Pair 3 (-)
E23	GND	GND	--	--	--	--	--	Logic Ground
E24	HB05_P	HB.HB05_P	13	VIO_B_M2C	User Selected	IO_L11P_T1_SRCC_13	U25	Bank HB User Defined Signal Pair 5 (+)
E25	HB05_N	HB.HB05_N				IO_L11N_T1_SRCC_13	V26	Bank HB User Defined Signal Pair 5(-)
E26	GND	GND	--	--	--	--	--	Logic Ground
E27	HB09_P	HB.HB09_P	13	VIO_B_M2C	User Selected	IO_L8P_T1_13	W29	Bank HB User Defined Signal Pair 9 (+)
E28	HB09_N	HB.HB09_N				IO_L8N_T1_13	W30	Bank HB User Defined Signal Pair 9 (-)
E29	GND	GND	--	--	--	--	--	Logic Ground

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
E30	HB13_P	HB.HB13_P	13	VIO_B_M2C	User Selected	IO_L17P_T2_13	T24	Bank HB User Defined Signal Pair 13 (+)
E31	HB13_N	HB.HB13_N				IO_L17N_T2_13	T25	Bank HB User Defined Signal Pair 13 (-)
E32	GND	GND	--	--	--	--	--	Logic Ground
E33	HB19_P	HB.HB19_P	13	VIO_B_M2C	User Selected	IO_L18P_T2_13	P23	Bank HB User Defined Signal Pair 19 (+)
E34	HB19_N	HB.HB19_N				IO_L18N_T2_13	P24	Bank HB User Defined Signal Pair 19 (-)
E35	GND	GND	--	--	--	--	--	Logic Ground
E36	HB21_P	HB.HB21_P	13	VIO_B_M2C	User Selected	IO_L4P_T0_13	N29	Bank HB User Defined Signal Pair 21 (+)
E37	HB21_N	HB.HB21_N				IO_L4N_T0_13	P29	Bank HB User Defined Signal Pair 21 (-)
E38	GND	GND	--	--	--	--	--	Logic Ground
E39	VADJ	VADJ	--	--	--	--	--	VADJ Power Supply (1.2V to 3.3V)
E40	GND	GND	--	--	--	--	--	Logic Ground

Table 12: J3: FMC Connector ROW F – Pin-Assignment

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
F1	PG_M2C	FSIG.PG_M2C	--	--	--	--	--	Asserted high by the FMC when Power Supplies VIO_B_M2C, VREF_A_M2C, VREF_B_M2C are within tolerance.
F2	GND	GND	--	--	--	--	--	Logic Ground
F3	GND	GND	--	--	--	--	--	Logic Ground
F4	HA00_P_CC	HA.HA00_CC_P	12	VADJ	User Selected	IO_L12P_T1_MRCC_12	AC28	Bank HA User Defined Signal Pair 0 (+) – Clock Preferable
F5	HA00_N_CC	HA.HA00_CC_N				IO_L12N_T1_MRCC_12	AD28	Bank HA User Defined Signal Pair 0 (-) – Clock Preferable
F6	GND	GND	--	--	--	--	--	Logic Ground
F7	HA04_P	HA.HA04_P	12	VADJ	User Selected	IO_L4P_T0_12	Y28	Bank HA User Defined Signal Pair 4 (+)
F8	HA04_N	HA.HA04_N				IO_L4N_T0_12	AA29	Bank HA User Defined Signal Pair 4 (-)
F9	GND	GND	--	--	--	--	--	Logic Ground
F10	HA08_P	HA.HA08_P	12	VADJ	User Selected	IO_L9P_T1_DQS_12	AC29	Bank HA User Defined Signal Pair 8 (+)
F11	HA08_N	HA.HA08_N				IO_L9N_T1_DQS_12	AD29	Bank HA User Defined Signal Pair 8 (-)
F12	GND	GND	--	--	--	--	--	Logic Ground
F13	HA12_P	HA.HA12_P	12	VADJ	User Selected	IO_L18P_T2_12	AE25	Bank HA User Defined Signal Pair 12 (+)
F14	HA12_N	HA.HA12_N				IO_L18N_T2_12	AF25	Bank HA User Defined Signal Pair 12 (-)

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
F15	GND	GND	--	--	--	--	--	Logic Ground
F16	HA15_P	HA.HA15_P	12	VADJ	User Selected	IO_L21P_T3_DQS_12	AJ28	Bank HA User Defined Signal Pair 15 (+)
F17	HA15_N	HA.HA15_N				IO_L21N_T3_DQS_12	AJ29	Bank HA User Defined Signal Pair 15 (-)
F18	GND	GND	--	--	--	--	--	Logic Ground
F19	HA19_P	HA.HA19_P	12	VADJ	User Selected	IO_L20P_T3_12	AJ30	Bank HA User Defined Signal Pair 19 (+)
F20	HA19_N	HA.HA19_N				IO_L20N_T3_12	AK30	Bank HA User Defined Signal Pair 19 (-)
F21	GND	GND	--	--	--	--	--	Logic Ground
F22	HB02_P	HB.HB02_P	13	VIO_B_M2C	User Selected	IO_L23P_T3_13	U24	Bank HB User Defined Signal Pair 2 (+)
F23	HB02_N	HB.HB02_N				IO_L23N_T3_13	V24	Bank HB User Defined Signal Pair 2 (-)
F24	GND	GND	--	--	--	--	--	Logic Ground
F25	HB04_P	HB.HB04_P	13	VIO_B_M2C	User Selected	IO_L9P_T1_DQS_13	V27	Bank HB User Defined Signal Pair 4 (+)
F26	HB04_N	HB.HB04_N				IO_L9N_T1_DQS_13	W28	Bank HB User Defined Signal Pair 4 (-)
F27	GND	GND	--	--	--	--	--	Logic Ground
F28	HB08_P	HB.HB08_P	13	VIO_B_M2C	User Selected	IO_L2P_T0_13	T30	Bank HB User Defined Signal Pair 8 (+)
F29	HB08_N	HB.HB08_N				IO_L2N_T0_13	U30	Bank HB User Defined Signal Pair 8 (-)
F30	GND	GND	--	--	--	--	--	Logic Ground

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
F31	HB12_P	HB.HB12_P	13	VIO_B_M2C	User Selected	IO_L20P_T3_13	T22	Bank HB User Defined Signal Pair 12 (+)
F32	HB12_N	HB.HB12_N				IO_L20P_T3_13	T23	Bank HB User Defined Signal Pair 12 (-)
F33	GND	GND	--	--	--	--	--	Logic Ground
F34	HB16_P	HB.HB16_P	13	VIO_B_M2C	User Selected	IO_L16P_T2_13	P25	Bank HB User Defined Signal Pair 16 (+)
F35	HB16_N	HB.HB16_N				IO_L16N_T2_13	P26	Bank HB User Defined Signal Pair 16 (-)
F36	GND	GND	--	--	--	--	--	Logic Ground
F37	HB20_P	HB.HB20_P	13	VIO_B_M2C	User Selected	IO_L3P_T0_DQS_13	N28	Bank HB User Defined Signal Pair 20 (+)
F38	HB20_N	HB.HB20_N				IO_L3N_T0_DQS_13	P28	Bank HB User Defined Signal Pair 20 (-)
F39	GND	GND	--	--	--	--	--	Logic Ground
F40	VADJ	VADJ	--	--	--	--	--	VADJ Power Supply (1.2V to 3.3V)

Table 13: J3: FMC Connector ROW G – Pin-Assignment

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
G1	GND	GND	--	--	--	--	--	Logic Ground
G2	CLK1_M2C_P	FCK.CLK1_M2C_P	--	--	--	--	--	Module-to-Carrier Clock 1 (+)
G3	CLK1_M2C_N	FCK.CLK1_M2C_N				--	--	Module-to-Carrier Clock 1 (-)
G4	GND	GND	--	--	--	--	--	Logic Ground
G5	GND	GND	--	--	--	--	--	Logic Ground
G6	LA00_P_CC	LA.LA00_CC_P	10	VADJ	User Selected	IO_L13P_T2_MRCC_10	AG17	Bank LA User Defined Signal Pair 0 (+) – Clock Preferable
G7	LA00_N_CC	LA.LA00_CC_N				IO_L13N_T2_MRCC_10	AG16	Bank LA User Defined Signal Pair 0 (-) – Clock Preferable
G8	GND	GND	--	--	--	--	--	Logic Ground
G9	LA03_P	LA.LA03_P	10	VADJ	User Selected	IO_L18P_T2_10	AD16	Bank LA User Defined Signal Pair 3 (+)
G10	LA03_N	LA.LA03_N				IO_L18N_T2_10	AD15	Bank LA User Defined Signal Pair 3 (-)
G11	GND	GND	--	--	--	--	--	Logic Ground
G12	LA08_P	LA.LA08_P	10	VADJ	User Selected	IO_L7P_T1_10	AE12	Bank LA User Defined Signal Pair 8 (+)
G13	LA08_N	LA.LA08_N				IO_L7N_T1_10	AF12	Bank LA User Defined Signal Pair 8 (-)
G14	GND	GND	--	--	--	--	--	Logic Ground
G15	LA12_P	LA.LA12_P	10	VADJ	User Selected	IO_L1P_T0_10	AK13	Bank LA User Defined Signal Pair 12 (+)
G16	LA12_N	LA.LA12_N				IO_L1N_T0_10	AK12	Bank LA User Defined Signal Pair 12 (-)

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
G17	GND	GND	--	--	--	--	--	Logic Ground
G18	LA16_P	LA.LA16_P	10	VADJ	User Selected	IO_L4P_T0_10	AJ16	Bank LA User Defined Signal Pair 16 (+)
G19	LA16_N	LA.LA16_N				IO_L4N_T0_10	AK16	Bank LA User Defined Signal Pair 16 (-)
G20	GND	GND	--	--	--	--	--	Logic Ground
G21	LA20_P	LA.LA20_P	11	VADJ	User Selected	IO_L16P_T2_11	AK17	Bank LA User Defined Signal Pair 20 (+)
G22	LA20_N	LA.LA20_N				IO_L16N_T2_11	AK18	Bank LA User Defined Signal Pair 20 (-)
G23	GND	GND	--	--	--	--	--	Logic Ground
G24	LA22_P	LA.LA22_P	10	VADJ	User Selected	IO_L15P_T2_DQS_10	AF18	Bank LA User Defined Signal Pair 22 (+)
G25	LA22_P	LA.LA22_N				IO_L15N_T2_DQS_10	AF17	Bank LA User Defined Signal Pair 22 (-)
G26	GND	GND	--	--	--	--	--	Logic Ground
G27	LA25_P	LA.LA25_P	11	VADJ	User Selected	IO_L8P_T1_11	AG24	Bank LA User Defined Signal Pair 25 (+)
G28	LA25_N	LA.LA25_N				IO_L8N_T1_11	AG25	Bank LA User Defined Signal Pair 25 (-)
G29	GND	GND	--	--	--	--	--	Logic Ground
G30	LA29_P	LA.LA29_P	11	VADJ	User Selected	IO_L24P_T3_11	AC22	Bank LA User Defined Signal Pair 29 (+)
G31	LA29_N	LA.LA29_N				IO_L24N_T3_11	AC23	Bank LA User Defined Signal Pair 29 (-)
G32	GND	GND	--	--	--	--	--	Logic Ground

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
G33	LA31_P	LA.LA31_P	11	VADJ	User Selected	IO_L23P_T3_11	AA22	Bank LA User Defined Signal Pair 31 (+)
G34	LA31_N	LA.LA31_N				IO_L23N_T3_11	AA23	Bank LA User Defined Signal Pair 31 (-)
G35	GND	GND	--	--	--	--	--	Logic Ground
G36	LA33_P	LA.LA33_P	11	VADJ	User Selected	IO_L21P_T3_DQS_11	Y22	Bank LA User Defined Signal Pair 33 (+)
G37	LA33_N	LA.LA33_N				IO_L21N_T3_DQS_11	Y23	Bank LA User Defined Signal Pair 33 (-)
G38	GND	GND	--	--	--	--	--	Logic Ground
G39	VADJ	VADJ	--	--	--	--	--	VADJ Power Supply (1.2V to 3.3V)
G40	GND	GND	--	--	--	--	--	Logic Ground

Table 14: J3: FMC Connector ROW H – Pin-Assignment

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
H1	VREF_A_M2C	FVREF.VREF_A_M2C	10	VADJ	User Selected	IO_L6N_T0_VREF_10	AH16	Reference Voltage associated with the signaling standard used by the Bank A (LA/HA).
			10			IO_L19N_T3_VREF_10	AC13	
			11			IO_L6N_T0_VREF_11	AH22	
			11			IO_L19N_T3_VREF_11	AB22	
			12			IO_L6N_T0_VREF_12	AB26	
			12			IO_L19N_T3_VREF_12	AH29	
H2	PRSNT_M2C_L	FSIG.PRSNT_M2C_L	--	--	--	--	--	Indicates to the Carrier if a FMC is Present.
H3	GND	GND	--	--	--	--	--	Logic Ground
H4	CLK0_M2C_P	FCK.CLK0_M2C_P	--	--	--	--	--	Module-to-Carrier Clock 0 (+)
H5	CLK0_M2C_N	FCK.CLK0_M2C_N	--	--	--	--	--	Module-to-Carrier Clock 0 (-)
H6	GND	GND	--	--	--	--	--	Logic Ground
H7	LA02_P	LA.LA02_P	10	VADJ	User Selected	IO_L20P_T3_10	AA15	Bank LA User Defined Signal Pair 2 (+)
H8	LA02_N	LA.LA02_N				IO_L20N_T3_10	AA14	Bank LA User Defined Signal Pair 2 (-)
H9	GND	GND	--	--	--	--	--	Logic Ground

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
H10	LA04_P	LA.LA04_P	10	VADJ	User Selected	IO_L21P_T3_DQS_10	AB12	Bank LA User Defined Signal Pair 4 (+)
H11	LA04_N	LA.LA04_N				IO_L21N_T3_DQS_10	AC12	Bank LA User Defined Signal Pair 4 (-)
H12	GND	GND	--	--	--	--	--	Logic Ground
H13	LA07_P	LA.LA07_P	10	VADJ	User Selected	IO_L17P_T2_10	AE18	Bank LA User Defined Signal Pair 7 (+)
H14	LA07_N	LA.LA07_N				IO_L17N_T2_10	AE17	Bank LA User Defined Signal Pair 7 (-)
H15	GND	GND	--	--	--	--	--	Logic Ground
H16	LA11_P	LA.LA11_P	11	VADJ	User Selected	IO_L18P_T2_11	AF19	Bank LA User Defined Signal Pair 11 (+)
H17	LA11_N	LA.LA11_N				IO_L18N_T2_11	AG19	Bank LA User Defined Signal Pair 11 (-)
H18	GND	GND	--	--	--	--	--	Logic Ground
H19	LA15_P	LA.LA15_P	10	VADJ	User Selected	IO_L2P_T0_10	AH18	Bank LA User Defined Signal Pair 15 (+)
H20	LA15_N	LA.LA15_N				IO_L2N_T0_10	AJ18	Bank LA User Defined Signal Pair 15 (-)
H21	GND	GND	--	--	--	--	--	Logic Ground
H22	LA19_P	LA.LA19_P	11	VADJ	User Selected	IO_L17P_T2_11	AH19	Bank LA User Defined Signal Pair 19 (+)
H23	LA19_N	LA.LA19_N				IO_L17N_T2_11	AJ19	Bank LA User Defined Signal Pair 19 (-)
H24	GND	GND	--	--	--	--	--	Logic Ground
H25	LA21_P	LA.LA21_P	11	VADJ	User Selected	IO_L10P_T1_11	AD21	Bank LA User Defined Signal Pair 21 (+)
H26	LA21_N	LA.LA21_N				IO_L10N_T1_11	AE21	Bank LA User Defined Signal Pair 21 (-)

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
H27	GND	GND	--	--	--	--	--	Logic Ground
H28	LA24_P	LA.LA24_P	11	VADJ	User Selected	IO_L9P_T1_DQS_11	AF23	Bank LA User Defined Signal Pair 24 (+)
H29	LA24_N	LA.LA24_N				IO_L9N_T1_DQS_11	AF24	Bank LA User Defined Signal Pair 24 (-)
H30	GND	GND	--	--	--	--	--	Logic Ground
H31	LA28_P	LA.LA28_P	11	VADJ	User Selected	IO_L7P_T1_11	AC24	Bank LA User Defined Signal Pair 28 (+)
H32	LA28_N	LA.LA28_N				IO_L7N_T1_11	AD24	Bank LA User Defined Signal Pair 28 (-)
H33	GND	GND	--	--	--	--	--	Logic Ground
H34	LA30_P	LA.LA30_P	11	VADJ	User Selected	IO_L22P_T3_11	AA24	Bank LA User Defined Signal Pair 30 (+)
H35	LA30_N	LA.LA30_N				IO_L22N_T3_11	AB24	Bank LA User Defined Signal Pair 30 (-)
H36	GND	GND	--	--	--	--	--	Logic Ground
H37	LA32_P	LA.LA32_P	11	VADJ	User Selected	IO_L20P_T3_11	W21	Bank LA User Defined Signal Pair 32 (+)
H38	LA32_N	LA.LA32_N				IO_L20N_T3_11	Y21	Bank LA User Defined Signal Pair 32 (-)
H39	GND	GND	--	--	--	--	--	Logic Ground
H40	VADJ	VADJ	--	--	--	--	--	VADJ Power Supply (1.2V to 3.3V)

Table 15: J3: FMC Connector ROW I – Pin-Assignment

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
J1	GND	GND	--	--	--	--	--	Logic Ground
J2	CLK3_BIDIR_P	FCK.CLK3_BIDIR_P	--	--	--	--	--	Bidirectional Clock 3 (+)
J3	CLK3_BIDIR_P	FCK.CLK3_BIDIR_P				--	--	Bidirectional Clock 3 (-)
J4	GND	GND	--	--	--	--	--	Logic Ground
J5	GND	GND	--	--	--	--	--	Logic Ground
J6	HA03_P	HA.HA03_P	12	VADJ	User Selected	IO_L1P_T0_12	Y30	Bank HA User Defined Signal Pair 3 (+)
J7	HA03_N	HA.HA03_N				IO_L1N_T0_12	AA30	Bank HA User Defined Signal Pair 3 (-)
J8	GND	GND	--	--	--	--	--	Logic Ground
J9	HA07_P	HA.HA07_P	12	VADJ	User Selected	IO_L7P_T1_12	AC26	Bank HA User Defined Signal Pair 7 (+)
J10	HA07_N	HA.HA07_N				IO_L7N_T1_12	AD26	Bank HA User Defined Signal Pair 7 (-)
J11	GND	GND	--	--	--	--	--	Logic Ground
J12	HA11_P	HA.HA11_P	12	VADJ	User Selected	IO_L24P_T3_12	AJ26	Bank HA User Defined Signal Pair 11 (+)
J13	HA11_N	HA.HA11_N				IO_L24N_T3_12	AK26	Bank HA User Defined Signal Pair 11 (-)
J14	GND	GND	--	--	--	--	--	Logic Ground
J15	HA14_P	HA.HA14_P	12	VADJ	User Selected	IO_L17P_T2_12	AG26	Bank HA User Defined Signal Pair 14 (+)
J16	HA14_N	HA.HA14_N				IO_L17N_T2_12	AG27	Bank HA User Defined Signal Pair 14 (-)

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
J17	GND	GND	--	--	--	--	--	Logic Ground
J18	HA18_P	HA.HA18_P	12	VADJ	User Selected	IO_L15P_T2_DQS_12	AF29	Bank HA User Defined Signal Pair 18 (+)
J19	HA18_N	HA.HA18_N				IO_L15N_T2_DQS_12	AG29	Bank HA User Defined Signal Pair 18 (-)
J20	GND	GND	--	--	--	--	--	Logic Ground
J21	HA22_P	HA.HA22_P	12	VADJ	User Selected	IO_L14P_T2_SRCC_12	AE27	Bank HA User Defined Signal Pair 22 (+)
J22	HA22_N	HA.HA22_N				IO_L14N_T2_SRCC_12	AF27	Bank HA User Defined Signal Pair 22 (-)
J23	GND	GND	--	--	--	--	--	Logic Ground
J24	HB01_P	HB.HB01_P	13	VIO_B_M2C	User Selected	IO_L10P_T1_13	W25	Bank HB User Defined Signal Pair 1 (+)
J25	HB01_N	HB.HB01_N				IO_L10N_T1_13	W26	Bank HB User Defined Signal Pair 1 (-)
J26	GND	GND	--	--	--	--	--	Logic Ground
J27	HB07_P	HB.HB07_P	13	VIO_B_M2C	User Selected	IO_L7P_T1_13	V28	Bank HB User Defined Signal Pair 7 (+)
J28	HB07_N	HB.HB07_N				IO_L7N_T1_13	V29	Bank HB User Defined Signal Pair 7 (-)
J29	GND	GND	--	--	--	--	--	Logic Ground
J30	HB11_P	HB.HB11_P	13	VIO_B_M2C	User Selected	IO_L5P_T0_13	T29	Bank HB User Defined Signal Pair 11 (+)
J31	HB11_N	HB.HB11_N				IO_L5N_T0_13	U29	Bank HB User Defined Signal Pair 11 (-)
J32	GND	GND	--	--	--	--	--	Logic Ground

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
J33	HB15_P	HB.HB15_P	13	VIO_B_M2C	User Selected	IO_L21P_T3_DQS_13	R22	Bank HB User Defined Signal Pair 15 (+)
J34	HB15_N	HB.HB15_N				IO_L21N_T3_DQS_13	R23	Bank HB User Defined Signal Pair 15 (-)
J35	GND	GND	--	--	--	--	--	Logic Ground
J36	HB18_P	HB.HB18_P	13	VIO_B_M2C	User Selected	IO_L1P_T0_13	P30	Bank HB User Defined Signal Pair 18 (+)
J37	HB18_N	HB.HB18_N				IO_L1N_T0_13	R30	Bank HB User Defined Signal Pair 18 (-)
J38	GND	GND	--	--	--	--	--	Logic Ground
J39	VIO_B_M2C	VIO_B_M2C	13	VIO_B_M2C	--	VCCO_13	N30	Power Supply generated by the FMC to power the FPGA's interfaced Bank.
							P27	
							R24	
							T21	
							U28	
							V25	
J40	GND	GND	--	--	--	--	--	Logic Ground

Table 16: J3: FMC Connector ROW J – Pin-Assignment

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
K1	VREF_B_M2C	FVREF.VREF_B_M2C	13	VIO_B_M2C	User Selected	IO_L6N_T0_VREF_13	T28	Reference Voltage associated with the signalling standard used by the Bank B (HB).
						IO_L19N_T3_VREF_13	R21	
K2	GND	GND	--	--	--	--	--	Logic Ground
K3	GND	GND	--	--	--	--	--	Logic Ground
K4	CLK2_BIDIR_P	FCK.CLK2_BIDIR_P	--	--	--	--	--	Bidirectional Clock 2 (+)
K5	CLK2_BIDIR_N	FCK.CLK2_BIDIR_N				--	--	Bidirectional Clock 2 (-)
K6	GND	GND	--	--	--	--	--	Logic Ground
K7	HA02_P	HA.HA02_P	12	VADJ	User Selected	IO_L5P_T0_12	AA27	Bank HA User Defined Signal Pair 2 (+)
K8	HA02_N	HA.HA02_N				IO_L5N_T0_12	AA28	Bank HA User Defined Signal Pair 2 (-)
K9	GND	GND	--	--	--	--	--	Logic Ground
K10	HA06_P	HA.HA06_P	11	VADJ	User Selected	IO_L2P_T0_11	AK22	Bank HA User Defined Signal Pair 6 (+)
K11	HA06_N	HA.HA06_N				IO_L2N_T0_11	AK23	Bank HA User Defined Signal Pair 6 (-)
K12	GND	GND	--	--	--	--	--	Logic Ground
K13	HA10_P	HA.HA10_P	12	VADJ	User Selected	IO_L23P_T3_12	AH26	Bank HA User Defined Signal Pair 10 (+)
K14	HA10_N	HA.HA10_N				IO_L23N_T3_12	AH27	Bank HA User Defined Signal Pair 10 (-)

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
K15	GND	GND	--	--	--	--	--	Logic Ground
K16	HA17_P_CC	HA.HA17_CC_P	12	VADJ	User Selected	IO_L13P_T2_MRCC_12	AE28	Bank HA User Defined Signal Pair 17 (+) – Clock Preferable
K17	HA17_N_CC	HA.HA17_CC_N				IO_L13N_T2_MRCC_12	AF28	Bank HA User Defined Signal Pair 17 (-) – Clock Preferable
K18	GND	GND	--	--	--	--	--	Logic Ground
K19	HA21_P	HA.HA21_P	12	VADJ	User Selected	IO_L16P_T2_12	AF30	Bank HA User Defined Signal Pair 21 (+)
K20	HA21_N	HA.HA21_N				IO_L16N_T2_12	AG30	Bank HA User Defined Signal Pair 21 (-)
K21	GND	GND	--	--	--	--	--	Logic Ground
K22	HA23_P	HA.HA23_P	12	VADJ	User Selected	IO_L8P_T1_12	AD30	Bank HA User Defined Signal Pair 23 (+)
K23	HA23_N	HA.HA23_N				IO_L8N_T1_12	AE30	Bank HA User Defined Signal Pair 23 (-)
K24	GND	GND	--	--	--	--	--	Logic Ground
K25	HB00_P_CC	HB.HB00_CC_P	13	VIO_B_M2C	User Selected	IO_L12P_T1_MRCC_13	U26	Bank HB User Defined Signal Pair 0 (+) – Clock Preferable
K26	HB00_N_CC	HB.HB00_CC_N				IO_L12N_T1_MRCC_13	U27	Bank HB User Defined Signal Pair 0 (-) – Clock Preferable
K27	GND	GND	--	--	--	--	--	Logic Ground
K28	HB06_P_CC	HB.HB06_CC_P	13	VIO_B_M2C	User Selected	IO_L13P_T2_MRCC_13	R25	Bank HB User Defined Signal Pair 6 (+) – Clock Preferable
K29	HB06_N_CC	HB.HB06_CC_N				IO_L13N_T2_MRCC_13	R26	Bank HB User Defined Signal Pair 6 (-) – Clock Preferable
K30	GND	GND	--	--	--	--	--	Logic Ground

PIN	FMC LABEL	NAMC-ZYNQ-FMC LABEL	BANK	VCCO	I/O SELECT	PIN NAME	PIN NUMBER	DESCRIPTION
K31	HB10_P	HB.HB10_P	13	VIO_B_M2C	User Selected	IO_L22P_T3_13	U22	Bank HB User Defined Signal Pair 10 (+)
K32	HB10_N	HB.HB10_N				IO_L22N_T3_13	V22	Bank HB User Defined Signal Pair 10 (-)
K33	GND	GND	--	--	--	--	--	Logic Ground
K34	HB14_P	HB.HB14_P	13	VIO_B_M2C	User Selected	IO_L15P_T2_DQS_13	N26	Bank HB User Defined Signal Pair 14 (+)
K35	HB14_N	HB.HB14_N				IO_L15N_T2_DQS_13	N27	Bank HB User Defined Signal Pair 14 (-)
K36	GND	GND	--	--	--	--	--	Logic Ground
K37	HB17_P_CC	HB.HB17_CC_P	13	VIO_B_M2C	User Selected	IO_L14P_T2_SRCC_13	R27	Bank HB User Defined Signal Pair 17 (+) – Clock Preferable
K38	HB17_N_CC	HB.HB17_CC_N				IO_L14N_T2_SRCC_13	T27	Bank HB User Defined Signal Pair 17 (-) – Clock Preferable
K39	GND	GND	--	--	--	--	--	Logic Ground
K40	VIO_B_M2C	VIO_B_M2C	13	VIO_B_M2C	--	VCCO_13	N30	Power Supply generated by the FMC to power the FPGA's interfaced Bank.
							P27	
							R24	
							T21	
							U28	
							V25	

4.3.5 J4: Atmel Programming Header

Connector J4 connects to the programming-port of the Atmel µC device.

Table 17: J4: Atmel Programming Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	PDI_DATA	+3.3V	2
3	nc	PROG	4
5	PDI_CLK	GND	6

4.3.6 J5: I²C Debug Header

J5 offers a I²C debugging interface.

Table 18: J5: I²C Debug Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	MCUI2CSCL	PWRSCL	2
3	GND	GND	4
5	MCUI2CSDA	PWRSDA	6

4.3.7 J6: JTAG Programming Header

J6 offers a JTAG programming interface towards the FPGA.

Table 19: J6: JTAG Programming Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	FPGA_JTAG.TCK	FPGA_JTAG.TMS	2
3	FPGA_JTAG.TDO	FPGA_JTAG.TDI	4
5	P3V3	GND	6

Note: J6 cannot be used, if JTAG programming via backplane is enabled by hardwire!

4.3.8 J7: Debug Header

J7 offers a debug interface for internal use only.

4.3.9 J8: MicroSD Card Socket

J8 offers a MicroSD Card Socket.

Table 20: J8: MicroSD Card Socket – Pin Assignment

Pin #	Signal	Signal	Pin #
1	DAT2CASE	CD/DAT3	2
3	CMD	P3V3	4
5	CLK	VSS	6
7	DAT0	DAT1	8

4.3.10 J9: Ethernet PHY Debugging Interface

The **NAMC-ZYNQ-FMC** features a debugging option of the Ethernet PHYS via the management interface J9.

Table 21: J9: Ethernet PHY Debugging Interface – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GBE.MDC	GND	2
3	GND	GND	4
5	GBE.MDIO	GND	6

4.3.11 SW1: Hot Swap Switch

Switch SW1 is used to support Hot-Swapping of the module. It conforms to PICMG AMC.0.

4.3.12 SW2: Reset Switch

Switch SW2 is used to reset the SoC (PL) configuration logic.

4.3.13 DIP SW3: SoC Boot Mode Selection Switch

The SoC's boot mode is configured by DIP SW3. The table below shows the factory defaults.

Table 22: DIP SW3: SoC Boot Mode Selection – Pin Assignment

SW3 Row	SW3 Position	MIO Value	Boot Mode
1	OFF	MIO[6] = 0	• JTAG Boot Mode: Cascade Mode MIO[5..3] = 000 • QSPI [Dual_Stacked_QSPI] MIO[5..3] = 100 • SD Card MIO[5..3]=110
2	ON		
3	ON	MIO[5] = 1	
4	OFF		
5	OFF	MIO[4] = 0	
6	ON		
7	OFF	MIO[3] = 0	
8	ON		
9	OFF	MIO[2] = 0	
10	ON		

4.3.14 DIP SW4: GbE Reset Mode Switch

DIP SW4 controls the mode of reset of the GbE's PHYs Port 0 and Port 1. By default, the reset is managed by the SoC according to the following table.

Table 23: DIP SW4: GbE Reset Mode – Pin Assignment

SW4 Row	SW4 Position
1	ON
2	ON
3	OFF
4	OFF
5	ON
6	ON
7	OFF
8	OFF

This switch is used for debugging purposes only and the default configuration shall not be changed.

5 Board Specification

Table 24: NAMC-ZYNQ-FMC Features – Overview

SoC	XILINX ZYNQ-7000 FPGA (XC7Z045 or XC7Z100)
AMC-Module	Standard Advanced Mezzanine Card single width, mid-size
Front-I/O	µUSB Debug Connector
Power Consumption	12V / 6A
Operating Temperature	0°C – +55°C with forced cooling
Storage Temperature	-40°C - +85°C
Humidity	10% – 90% rh non-condensing
Standards compliance	PICMG AMC.0 Rev. 2.0 PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format) PICMG SFP.1 Rev. 1.0 (Internal TDM) IPMI Specification v2.0 Rev. 1.0 PICMG µTCA.0 Rev. 1.0

6 Installation

6.1 Safety Note

To ensure proper functioning of the **NAMC-ZYNQ-FMC** during its usual lifetime take the following precautions before handling the board.

CAUTION
Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime!

- Before installing or uninstalling the **NAMC-ZYNQ-FMC** read this installation section
- Before installing or uninstalling the **NAMC-ZYNQ-FMC**, read the Installation Guide and the User's Manual of the carrier board used, or of the µTCA system the board will be plugged into.
- Before installing or uninstalling the **NAMC-ZYNQ-FMC** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps
  - Finally turn on or off the power if necessary.
  - Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAMC-ZYNQ-FMC** is connected to the carrier board or to the µTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

6.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements!

6.2.1 Requirements

The installation requires only
- an ATCA carrier board or a µTCA backplane for connecting the **NAMC-ZYNQ-FMC**
- power supply
- cooling devices

6.2.2 Power supply

The power supply for the **NAMC-ZYNQ-FMC** must meet the following specifications:
- required for the module:
  - +12V / 6A max.
  - + 3,3V / 0.15A max.

6.2.3 Automatic Power Up

In the following situations the **NAMC-ZYNQ-FMC** will automatically be reset and proceed with a normal power up:
- The voltage sensor generates a reset
  - when +12V voltage level drops below 8V
  - when +3.3V voltage level drops below 3.08V
- The carrier board / backplane signals a PCIe Reset.

6.3 Statement on Environmental Protection

6.3.1 Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

6.3.2 Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste. If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on

"Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

6.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

6.3.4 Product Safety

The board complies with EN60950 and UL1950.

6.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

7 Known Bugs / Restrictions

none

Appendix A: Reference Documentation

[1] XILINX Zynq-7000 All Programmable SoC Data Sheet, DS190 (v1.11) 06/2017

Appendix B: Document's History

Revision	Date	Description	Author
0.1	16.11.2016	Draft Release	mm
1.0	25.09.2018	Initial Release	se
1.1	24.10.18	Correction of boot mode table (SW3)	mm
	03.02.20	Reworked JTAG section Added FAT pipe pin description Reworked Frontpanel LED description	mm
1.2	19.05.2020	Updated chapter 3.7 "Clock Architecture"	se
	04.06.2020	Updated chapters 4.3.3 and 4.4.4 (Assignment from AMC/FMC to FPGA pins)	se