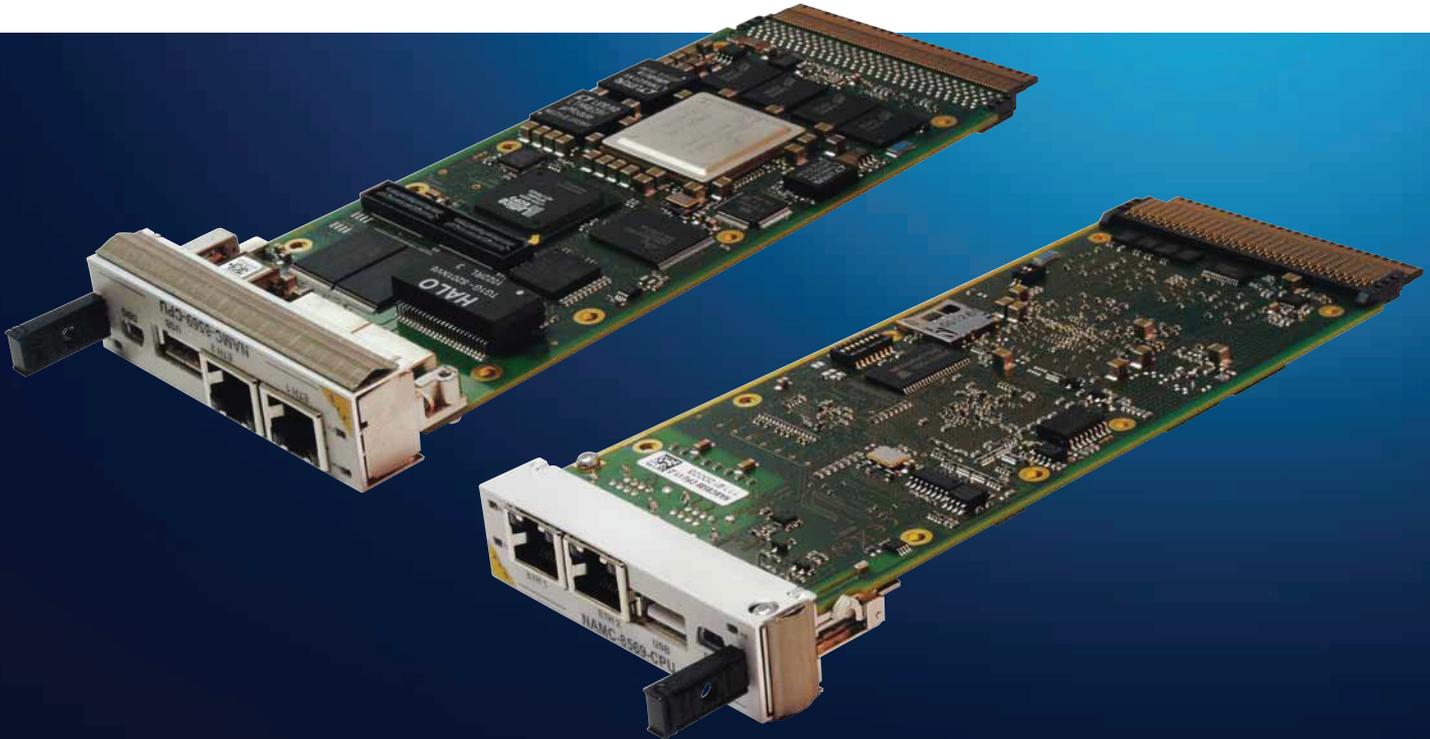


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NAMC-8569-CPU



Overview

The NAMC-8596-CPU is a multi-service CPU board in Advanced Mezzanine Card™ (AMC). Flexibility, high-bandwidth and low latency processing dedicate the **NAMC-8569-CPU** for applications in (tele-) communication, medical, industrial automation, defense&aerospace and telecommunication market. One or both GbE interfaces can be switched or multiplexed towards the CPU and the backplane. Depending on the required throughput one Fat Pipe (PCIe or SRIO) or the combination of both Fat Pipes (PCIe and SRIO) is available to the backplane. Thus, the **NAMC-8569-CPU** is targeting at applications where IO boards need PCIe and where low latency of SRIO for multiprocessing is requested.

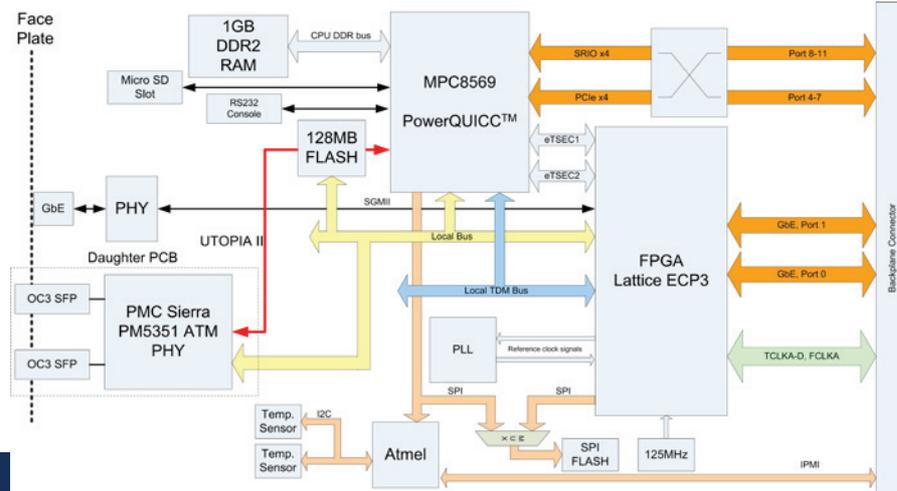
Key features

- Latest Freescale™ PowerQUICC® III MPC8569 processor
 - dual Multichannel Communication Controller (MCC)
 - higher core frequency than predecessor PowerQUICC III processors
- DDR2 SDRAM 1GB, NAND-Flash 2GB
- Lattice FPGA
 - up to 70.000 logic cells
- Interfaces at front panel
 - 2x Gigabit Ethernet (GbE)
 - USB port and RS232
 - optional user defined IO via sub module
 - optional TDM connectivity
- Backplane connections
 - 2x Gigabit Ethernet (GbE)
 - Serial Rapid IO (SRIO)
 - PCI Express® (PCIe)
- TDM and I-TDM
 - 125 µs and 1 ms I-TDM modes as well as TDM cross-connect supported
- customizable I/O mezzanines



Technical Data

NAMC-8569-CPU



Overview

The NAMC-8596-CPU is a multi-service processor board featuring multiple Ethernet, SRIO, PCIe interfaces along with an USB port and optional TDM connectivity. It is available as a single compact-, mid- and full-size AMC. The full-size AMC can be equipped with an extension board adding customized I/O functionality. The NAMC-8596-CPU provides flexibility, high-bandwidth and low latency processing in next generation systems based on the MicroTCA® or ATCA standards.

The combination of software based processing resources and FPGA based hardware resources dedicate the **NAMC-8569-CPU** for a wide-spread of possible applications in (tele-) communication, medical, industrial automation, defense&aerospace and telecommunication market.

CPU and Memory

The **NAMC-8569-CPU** is equipped with the powerful Freescale PowerQUICC III MPC8569. It offers an e500 PowerPC core combined with dedicated interface hardware and four RISC cores. This network processor operates at core frequencies of 800, 1000 or 1333 MHz. The main onboard

memory is delivered by 128-1024 MB DDR2 SDRAM. In addition, the **NAMC-8569-CPU** is equipped with 16-128 MB 16-bit parallel FLASH (NOR) and 2GB NAND Flash memory. A Micro-SD-Card slot could be used for high capacity, non-volatile but removable memory. Permanent write capabilities i.e. for data capturing are provided by an optional 512kB MRAM (non-volatile SRAM).

Front Panel Interfaces

The flexible deployment of the **NAMC-8569-CPU** is based on the rich offer of versatile interfaces. For example, the USB trunk can be applied either to implement USB host or device functionality. The RS232 serves for debugging purpose along with a standard terminal program. Both GbE interfaces are directly connected to the FPGA from Lattice and can be operated via back plane or front panel, or in a combination of both.

TDM and I-TDM Interface

The ECP3 FPGA from Lattice provides the powerful TDM to I-TDM bridge of the **NAMC-8569-CPU** along with a timeslot interchanger (TSI) that is also implemented in the FPGA logic. Line interfaces of other AMC boards can be

directly connected to channels of the MPC8569 MCC controllers allowing flexible routing. The TDM-to-ITDM bridge converts the TDM oriented bit stream into Ethernet packets and vice versa. In addition to the I-TDM interface, the TSI offers an optional 32MHz clocked H.110-alike TDM backplane interface at the AMC connector (extended area).

Fabric Support

Fat Pipe

The **NAMC-8569-CPU** offers four bidirectional serial lanes that can be operated either as PCIe, SRIO, or a combination of both. The **NAMC-8569-CPU** can be configured to implement either PCIe: one x1 (port 4/8) or one x4 (ports 4-7/8-11). SRIO: two x1 (port 4 and 8) or one x4 (port 4-7/8-11). The speed is configurable for 1.25Gb/s, 2.5Gb/s or 3.125Gb/s. PCIe and SRIO: one x1 PCIe (port 4) and one SRIO (port 8). In this case the speed of the SRIO interface is fixed at 2.5Gb/s

Base Fabric

The **NAMC-8569-CPU** provides two 1000BaseX interfaces at port 0 and port 1 of the common options region of the AMC backplane connector.

Key Features

System Processor and Memory

- up to 1,3GHz Freescale PowerQUICCIII MPC8569
- 128-1024 MB DDR2 SDRAM
- 16-128 MB FLASH
- Micro-SD-Card slot
- 512 kB MRAM
- 2GB NAND Flash

Front Panel Interfaces

- USB, RS232, 2 x GbE

Backplane Connectivity

Fat Pipe Interface Options

- PCIe x4 on ports 4-7 or 8-11
- PCIe x1 on port 4 or 8
- SRIO x4 on ports 4-7 or 8-11; speed 1.25Gb/s or 2.5Gb/s or 3.125 Gb/s per lane
- SRIO x1 on ports 4 and port 8; speed 1.25Gb/s or 2.5Gb/s or 3.125 Gb/s
- PCIe x1 on port 4 and SRIO x1 on port 8;

speed 2.5Gb/s

I-TDM Interface

- 1024 bidirect. 64kbit/s channels
- 125 µs-mode and 1ms-mode support

TDM (optional)

- H.110 alike 32MHz clocked TDM interface connects to ports 12, 13 (data) and port 14 (sync)

Networking

- 2 x 1 GbE at AMC port 0 and 1
- 2 x 1000/100/10 Base T

Indicator LEDs

- Various link indications by 4 LED's at RJ45 connector
- 1 fault indication LED controlled by the IPMI controller
- 1 general purpose LED controlled by the FPGA/CPU

Operating System Support

- OK-1, QNX, LINUX (on request)

Power Consumption

- 12 V, 2A max.

Environmental Conditions

- operating temp.: 0°C to +55°C with forced cooling
- storage temp.: -40°C to +85°C
- relative humidity: 10% to 90% rh noncondensing

Standard Compliance

- PICMG AMC.0 Rev. 2.0
- PICMG AMC.1 Rev. 1.0
- PICMG AMC.2 Rev. 1.0 (Type E2)
- PCIe Base Spec. Rev. 1.1
- PICMG SFP.0 Rev. 1.0
- PICMG SFP.1 Rev. 1.0
- IPMI Specification v2.0 Rev. 1.0
- PICMG µTCA.0 Rev. 1.0