NAMC-ARRIA10-FMC
AMC-FMC Carrier Module
Technical Reference Manual V1.4
HW Revision 1.5

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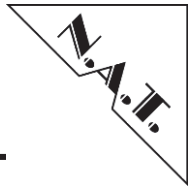

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

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Conventions

If not otherwise specified, addresses and memory maps are written in hexadecimal notation, identified by 0x. The following table gives a list of the abbreviations used in this document.

Table 1: List of used abbreviations

Abbreviation	Description
AMC	Advanced Mezzanine Card
AS	Active Serial
COM	Communication Port
CPU	Central Processing Unit
CvP	Configuration via Protocol
DBG	Debug
DDR SDRAM	Double Data Rate Synchronous Dynamic RAM
DIP SW	Dual In-Line Switch
EEPROM	Electrically Erasable PROM
ECC	Error Correcting Code
FCLK	Fabric Clock
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
FRU	Field Replaceable Unit
GbE	Gigabit Ethernet
GND	Ground
HPC	High Pinout Connector
HPS	Hard Processor System
PS	Hot Swap
I²C	Inter-Integrated Circuit
I/O	Input / Output
IP	Internet Protocol
IPMI	Intelligent Platform Management Interface
JSM	JTAG Switch Module
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LPC	Low Pinout Connector
µC	Microcontroller
µTCA	Micro Telecommunications Computing Architecture
MMC	Module Management Controller
(M)LVDS	Multipoint Low Voltage Differential Signalling
P2P	Peer-To-Peer
PCB	Printed Circuit Board
PCI(e)	Peripheral Component Interconnect (Express)
PS	Passive Serial
PS	Processing System
QSPI	Quad SPI
RAM	Random Access Memory
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface

Abbreviation	Description
(P)ROM	(Programmable) Read Only Memory
PLL	Phase Locked Loop
SAS	Serial Attached SCSI
SATA	Serial Advanced Technology Attachment
SCSI	Small Computer System Interface
SD-Card	Secure Digital Memory Card
SerDes	Serializer / Deserializer
SGMII	Serial Gigabit Media Independent Interface
SoC	System On A Chip
SRIO	Serial Rapid I/O
TCKL	Telecom Clock
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
XAUI	10 GbE (via 4x 3.125 GB/s)

1 Introduction

N.A.T.'s **NAMC-ARRIA10-FMC** is a high performance AMC carrier card for FMC modules. It supports HPC and LPC connector FMC modules as defined by VITA 57.1. The heart of the board is formed by the Intel/Altera Arria10 FPGA in NF40 BGA-1517 package with high count I/O to facilitate the connectivity of all required FMC HPC connector pins with the FPGA core. Intel® Arria® 10 FPGAs deliver massive performance and power consumption improvements compared to prior-generation FPGAs, both midrange and high-end devices. The board is available in various FPGA configurations beginning from SX570 over SX660 (with embedded dual ARM core CPU) up to GX1150.

The capability of carrying both HPC and LPC FMC modules allows it to be used in a wide range of applications providing data acquisition, networking, RF or other functionality. Typical applications might be wireless base stations, camera systems or generic research applications which require high speed sensor data conversions from analogue to digital.

The **NAMC-ARRIA10-FMC** is a single width AMC card available with full-size or mid-size front panels which allows it to be used in any MicroTCA chassis. The board has three FPGA/CPU dedicated high dense DDR4 memory interfaces with a total amount of up to 16 Gigabytes. To simplify the user interaction with the FPGA/SoC the front panel of the board gives access to the MircoSD card and the onboard Altera© Blaster II circuitry for comfortable JTAG access without any probe or adapter needed.

The following figure shows a photo of the **NAMC-ARRIA10-FMC.**

Figure 1: Board View

2 Overview

2.1 Major Features

Form Factor
- Single width, full-size or mid-size AMC

FPGA configurations
- Intel/Altera Arria 10
- GX1150, GX900, GX660, GX570
- SX660, SX570

CPU (SX variant only)
- Dual Core ARM Cortex A9 processor, up to 1.5 GHz

FMC slot:
- High-Pin Count FMC slot per VITA 57.1 compliant
- Low-Pin Count FMC slot per VITA 57.1 compliant
- All HPC differential pairs (LA/HA/HB) are routed to the FPGA.
- DP0 to DP09 are routed to the FPGA

Memory
- Total up to 16GB of SDRAM
- 8 GB DDR4 (x72) memory bank with ECC dedicated to FPGA
- 4 GB DDR4 (x40) memory bank with ECC dedicated to FPGA
- 4 GB DDR4 (x40) memory bank with ECC dedicated to HPS or FPGA
- 128 MB HPS boot memory flash (QSPI)
- 128 MB FPGA configuration memory flash (QSPI)
- MicroSD card slot

Backplane Connectivity
- Dual 1GbE connect to Port 0 and Port 1
- Ports 2 and 3 for SATA, SAS
- One x8 PCIexpress Gen3 connect to Fat-Pipe-Region Ports 4-11 or
- Dual x4 PCIexpress Gen3 to Fat-Pipe-Region Ports 4-7 and Ports 8-11 or
- Dual x4 SRIO Gen2 to Fat-Pipe-Region Ports 4-7 and Ports 8-11
- Any Combinations of PCIe, SRIO, XAUI (on request)
- Full AMC TCLKA-D and FCLKA connectivity (bidirectional)
- Point to point connectivity: Ports 12-15 routed to FPGA (2 x 4 LVDS)
- 8x MLVDS trigger lines (Ports 17-20)

Front Panel
- Dual UART-USB to ARM core (SX660, SX570 only) and MMC
- AMC standard LEDs and Hot Swap Handle
- Application LEDs

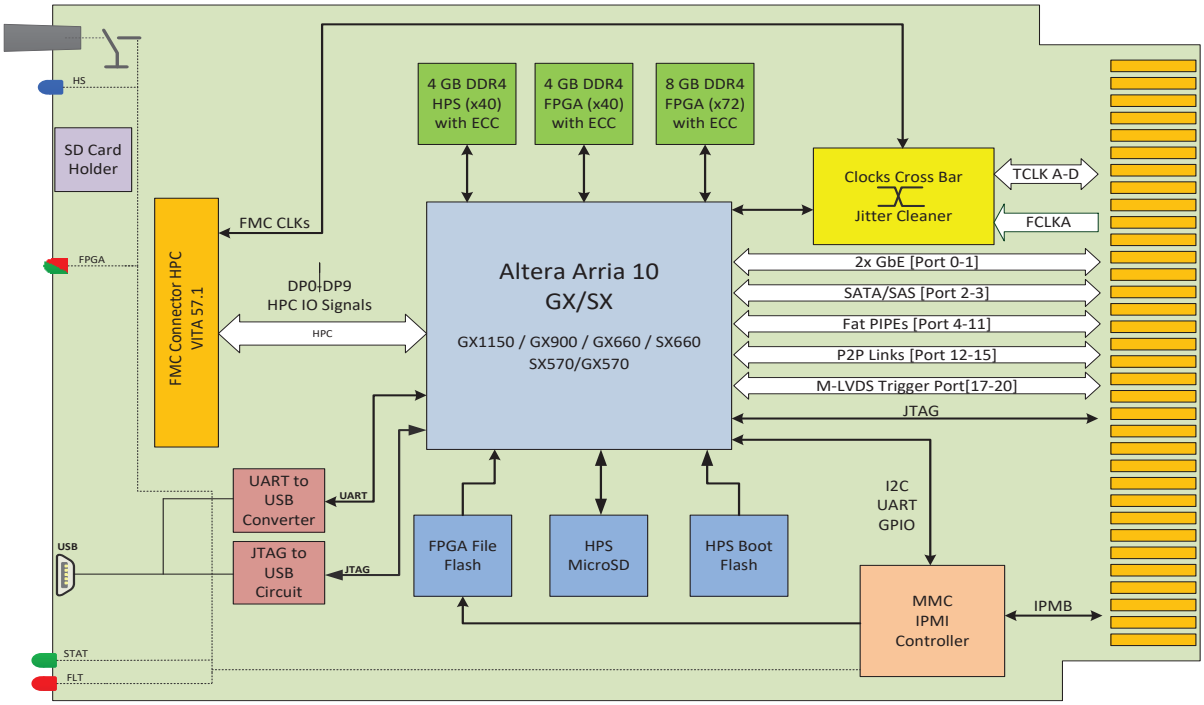
Compliance

- AMC.0 R2.0, AMC.1, AMC.2, AMC.3, AMC.4, IMPI V1.5, HPM.1
- EN60950, UL1950, RoHS

2.2 Block Diagram

The following figure shows a block diagram of the **NAMC-ARRIA10-FMC**.

Figure 2: Block Diagram



3 Board Inspection

3.1 Location Diagram

The position of important components and connectors is shown in the following location overview. Depending on the board type it might be that the board does not include all components shown in the location diagram.

Figure 3: Board View (TOP)

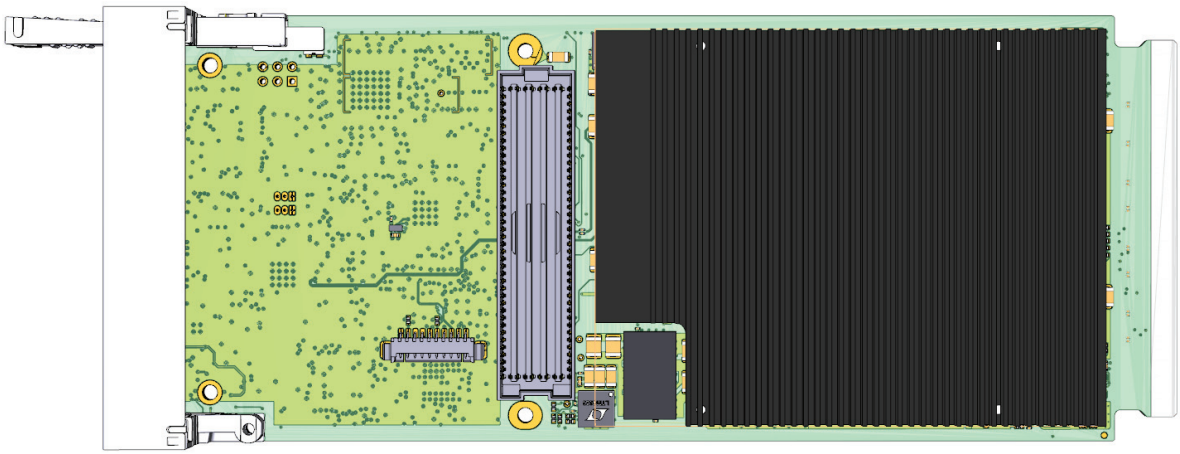
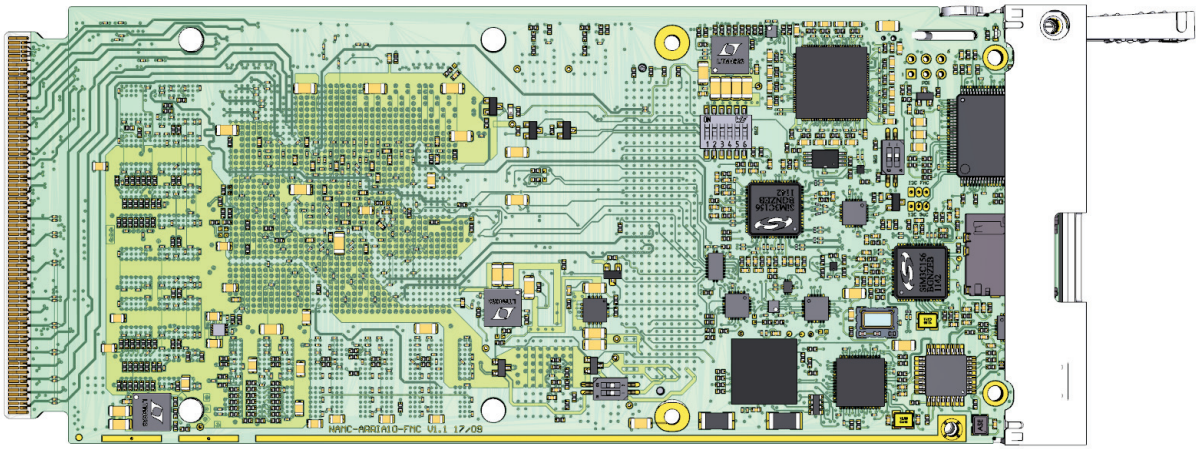


Figure 4: Board View (BOT)



3.2 DIP Switches

The board is configurable using DIP switches SW2, SW3 and SW4. The following figure shows the switch locations on the bottom side of the PCB.

Figure 5: DIP Switch locations

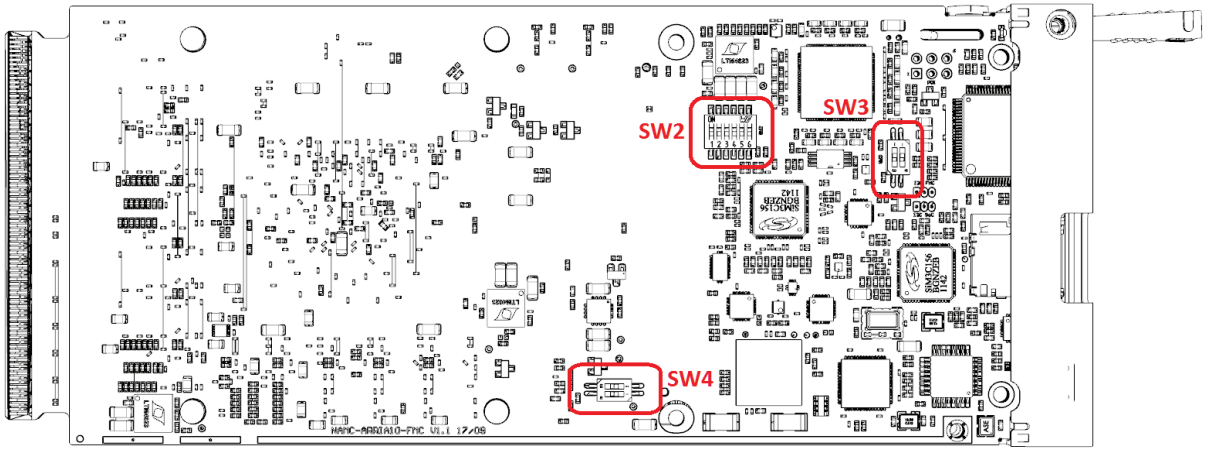


Table 2: SW2 DIP switch configuration

	ON	OFF (Factory Default)
SW2-1 (Note 1)	User Logic	User Logic
SW2-2 (Note 2)	User Logic	User Logic
SW2-3 (Note 3)	Start FMC FRU record wizard to create / edit FMC records during board startup (see section 7)	Use FMC records to determine module requirements. If FMC records are corrupted or not available the carrier will not power on.
SW2-4	Skip parsing of FMC EEPROM FRU and power VADJ and VIO_B_M2C with 1.8V.	Parsing of FMC EEPROM FRU enabled. VADJ, and VIO_B_M2C is set at the carrier according to the contents of the FMC EEPROM records.
SW2-5	Set FPGA configuration source to Passive Serial (PS)	Set FPGA configuration source to Active Serial (ASx4). It uses the EPCQ flash device for its configuration
SW2-6 (Note 4)	Set HPS boot source to QSPI flash memory	Set HPS boot source to SD-Card.

Note 1: SW2-1 is connected to user FPGA logic (PIN_H18)
Note 2: SW2-2 is connected to user FPGA logic (PIN_H19)
Note 3: SW2-3 has no effect when SW2-4 is set to "ON"
Note 4: If the HPS boot source is "SD-Card" the user needs to do an Early-I/O-Release first in order for the HPS to get access to the SD card controller which is connected to FPGA logic.

See chapter 4.3 Configuration & Booting for more information.

Table 3: SW3 DIP switch configuration

	ON	OFF (Factory Default)
SW3-1	Select Backplane as JTAG master	Select Embedded USB Blaster as JTAG master
SW3-2 (Note 1)	Route FPGA JTAG to Backplane	Route FMC JTAG to Backplane

Note 1: See section 4.2.3 for more detailed information regarding JTAG multiplexing. This dip switch is not available for PCB version greater than V1.1.
Note 2: To use the external JTAG header as master, DIP SW3-2 needs to be turned off (Only for board revision 1.1)
Note 3: SW3-2 has no effect on hardware revision 1.2. When selecting Embedded USB Blaster as JTAG master (SW3-1) on revision 1.2 the FMC JTAG is automatically routed to backplane.

Table 4: SW3 DIP switch configuration (only revision 1.0 and 1.1)

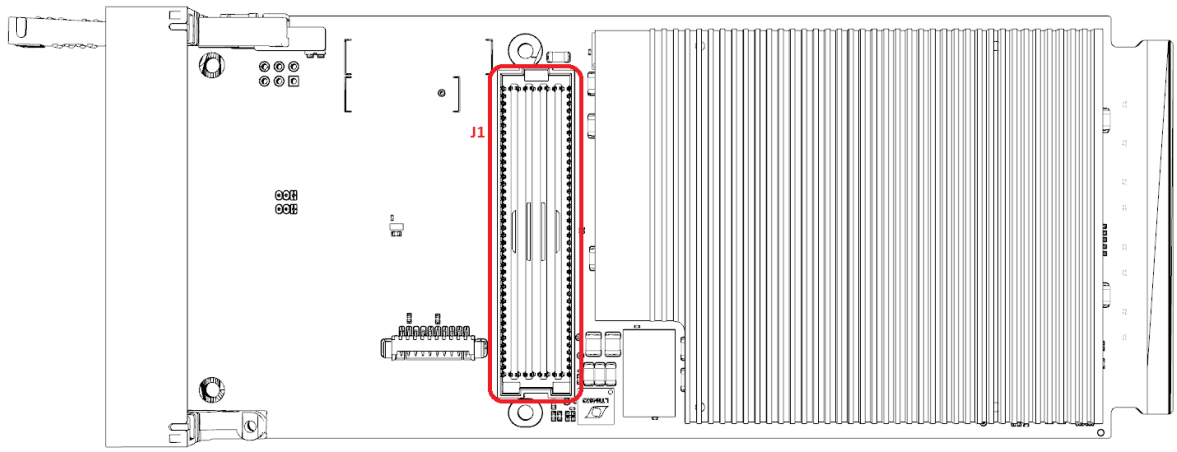
	ON	OFF (Factory Default)
SW4-1	VIO_B_M2C is always switched on. Voltage is equal to VADJ (1.2 – 1.8V)	VIO_B_M2C is switched on/off automatically based on FMC DC records
SW4-2	VREF_B_M2C is always switched on. Voltage is equal to VADJ (1.2 – 1.8V)	VREF_B_M2C is switched on/off automatically based on FMC DC records

Note: Per VITA 57.1 specification HPC FMC modules source VIO_B_M2C and VREF_B_M2C. Use this DIP switch to overwrite sourcing of these voltages regardless the FMC EEPROM contents. The FPGA cannot be used without sourcing VIOB_M2C and VREF_B_M2C.

Note: DIP switch SW4 has been replaced with MOSFET switching circuitry on hardware revision 1.2.

3.3 FMC Baseboard Connector

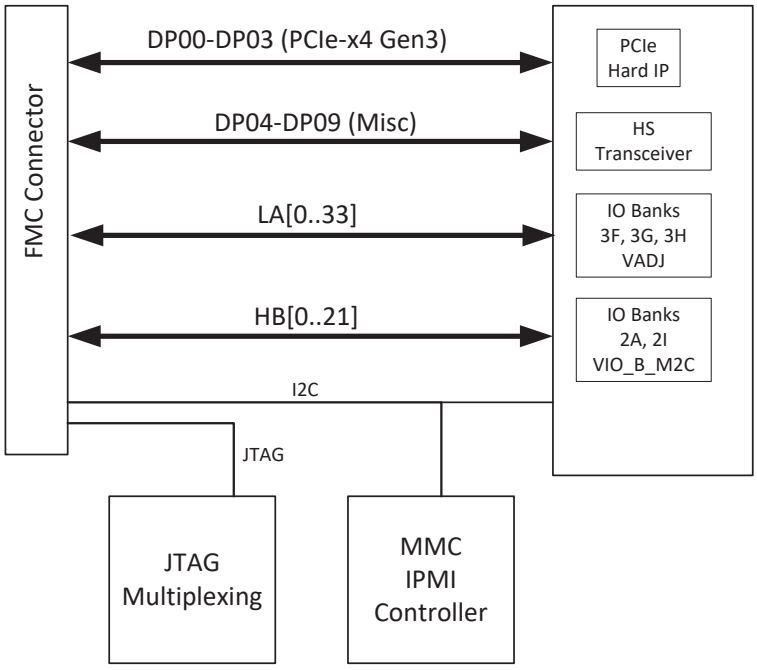
Figure 6: FMC Baseboard Connector



The figure above shows the locations of the main FMC HPC connector (J1). Please see chapter 10 for a detailed pin map of connector J1.

The following figure shows the pin mapping between the FPGA and FMC connector.

Figure 7: FMC to FPGA Signalling



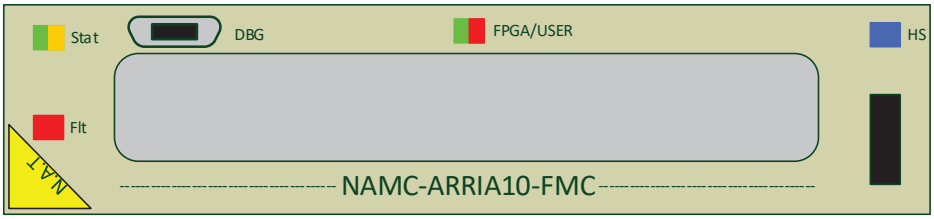
All high-speed transceiver pins are connected to FPGA transceivers. Especially DP00 to DP03 can be used with the FPGA internal PCIe-x4 hard IP controller. It is also possible to use DP00-DO07 as PCIe-x8 link. All User-I/O are connected as LVDS transmission lines to the FPGA. The FPGA also has access to the FMC management bus (I^2C) that can be used to read / write FMC records from within FPGA logic. The FMC JTAG signals can be routed

to the backplane using the board JTAG multiplexer logic (See Section ***JTAG*** for more information).

3.4 Front Panel & LEDs

The front panel gives access to interfaces and LEDs. The following figure shows the locations of the following utilities.

Figure 8: Front Panel



The MicroUSB Port (DBG) gives access to a dual UART interface port (MMC and FPGA) and the embedded USB blaster programmer. Both functions are merged using an USB hub.

Note: For hardware revision 1.0 and 1.1 maximum USB speed is limited to full speed (12M). USB highspeed (480M) is available from hardware revision 1.2.

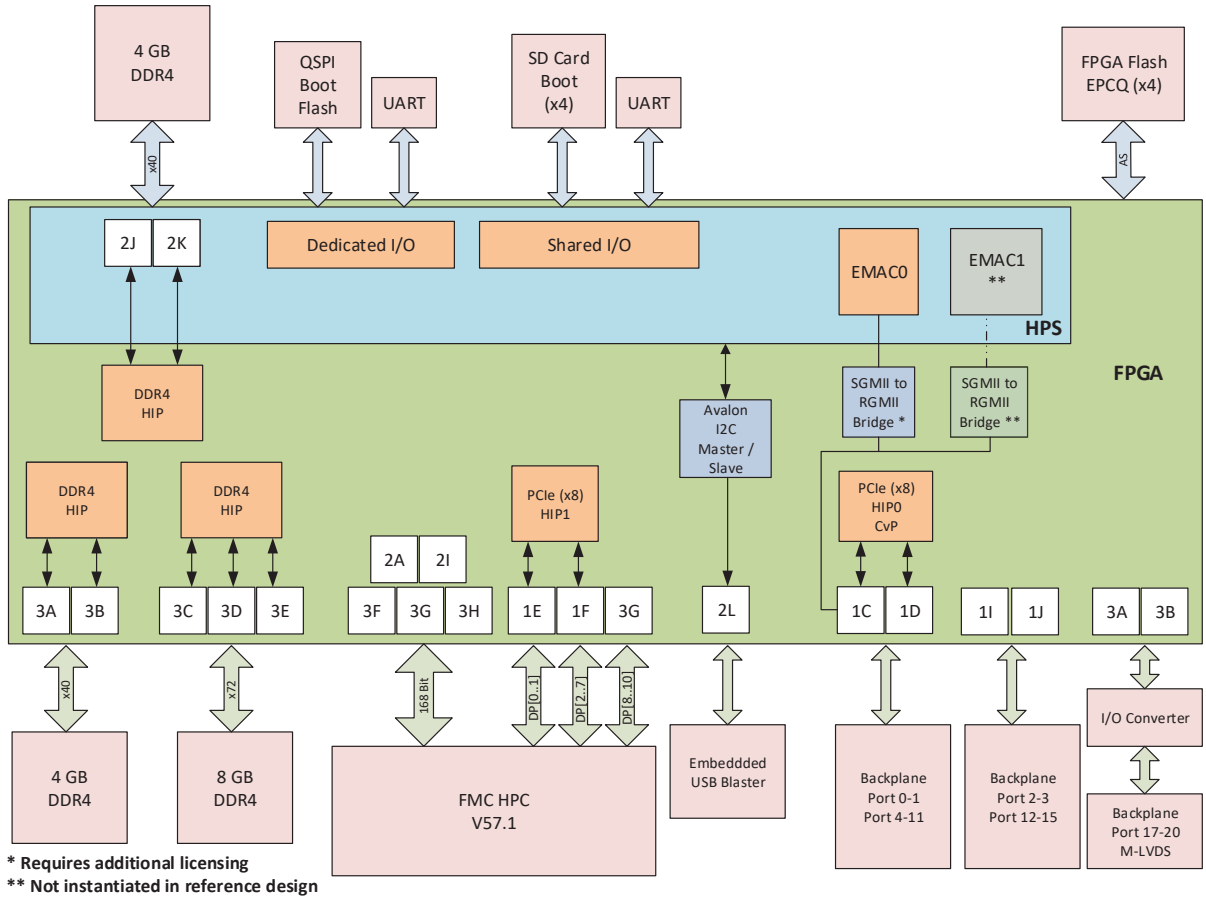
Table 5: LED functions

Led	Function		
FLT (Red)	ON	Error. See error codes to figure out condition	
	OFF	Normal operation	
	BLINK	FMC is not compatible with carrier	
	Error Code	Stat LED is blinking constantly	FPGA is not configured
		Stat LED is blinking but not constant	Error during board initialization. See MMC log for more information.
HS (Blue)	ON	AMC is in M1 state (HS Handle is pulled out)	
	OFF	AMC is in M4 state (HS handle is pushed in)	
	BLINK	During state transition between M1 and M4	
Stat (Green)	ON	Normal operation	
	OFF	During FPGA board initialization	
	BLINK	-	
Stat (Yellow)	ON	-	
	OFF	Normal operation	
	BLINK	FPGA is not configured	
User (Green/Red)	User LED connected to FPGA logic. When using the factory image this LED toggles between GREEN/RED each second. Red: PIN_G17, High Active Green: PIN_F18, High Active		
Board LED (Green)	User LED connected to HPS I/O. When using Factory Image this LED gets turned off when FPGA is configuration is done. PIN_L18, High Active.		

4 FPGA Operation

4.1 Resource Overview

Figure 9: FPGA Resource Overview



The figure above shows how the HPS and FPGA section within the Arria10 are connected to outside peripherals. The blue box shows all peripherals that are dedicated to the Hard Processor System in case of using the **NAMC-ARRIA10-FMC** in any SX option. The green section visualizes the fabric part of the device with internal hard or soft IPs. All orange boxes symbolize hard IPs while the soft blue boxes show soft IPs that are required for specific functions to be used. Some of the soft IPs e.g. SGMII to HPS may need additional licensing.

The Hard Processor System (HPS) has dedicated connections to a QSPI boot flash for firmware or bootloader storage, UART and 4 gigabytes of dedicated DDR4 memory. The DDR4 memory is connected to FPGA banks 2J and 2K. The SD card hard IP controller is connected to the HPS using the shared I/O section. Any function that is connected to the shared I/O will not be accessible to the HPS until the FPGA is fully configured. To speed up access to the shared IO the user can split the programming file into two parts in order to do an early I/O release from within u-boot on chip memory.

To get ethernet access from within the HPS the user will have to instantiate a SGMII to RGMII bridge that performs the conversion from 1000Base-X or SGMII backplane Ethernet to the processor's parallel internal GMII interface. This softcore contains the PCS/PMA function of the TSE (Tripple Speed Ethernet) IP Core which needs additional licensing.

The user could use the PCIE Hard IP "0" which is connected to AMC backplane port 4-11 to be used as a single x8 or x4 link. This hard IP supports Configuration via Protocol (CvP) to configure the FPGA over PCIexpress. The second PCIe Hard IP is connected to FMC high speed data lanes DP00-DP07 to create a x8 link.

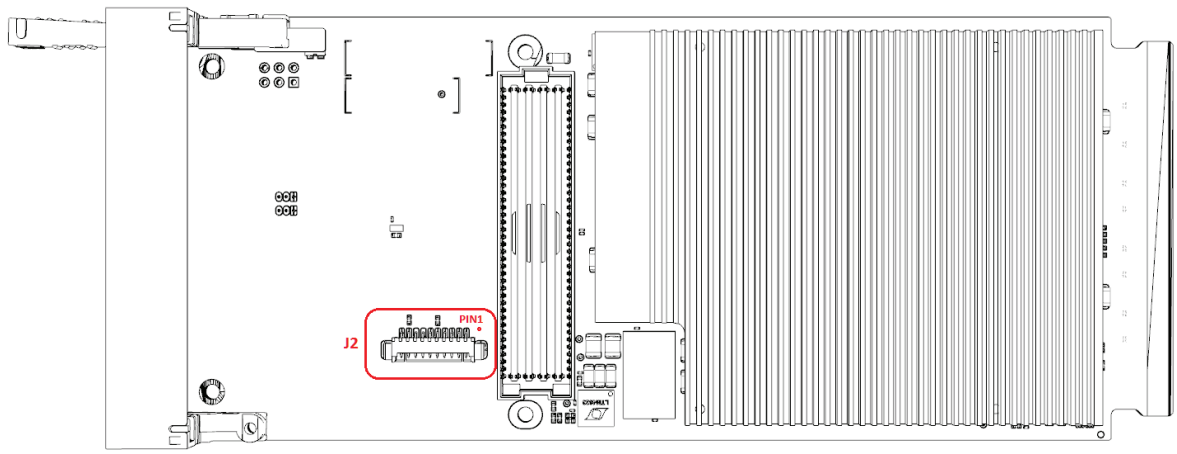
In order to get I^2C access to board peripherals such as the clocking multiplexer or clock generators the user has to instantiate a soft IP core (Avalon I^2C).

To offer users a more easy and quick start with the **NAMC-ARRIA10-FMC** the board is delivered with a Quartus Prime hardware example project which implements most of the functions that are shown in Figure 9: FPGA Resource Overview. It also includes the complete FPGA pinout.

4.2 JTAG

4.2.1 External JTAG Header

Figure 10: External JTAG Header



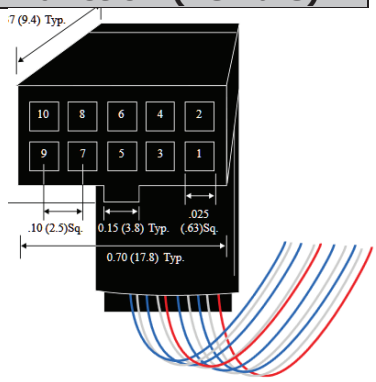
The pin out of connector J2 is shown in Figure 10: External JTAG Header. This connector gives direct access to FPGA JTAG signals. To connect to the FPGA use the JTAG connector on the top side of the carrier. Use the adapter cable that has been delivered with the board to connect the 10 pin female header of the Intel Altera USB Blaster II Programmer. **Please do only use the original programmer delivered by Altera/Intel (see figure below) in order not to damage the FPGA.**

Figure 11: Intel Programming Cable II

There are several no-name low-budget copies of the blaster programming cable available that may damage the FPGA. The original programming cable can be obtained by the following part number: PL-USB2-BLASTER

Table 6: JTAG Connector Signal Mapping

Pin	Board Header Function	Intel FPGA Download Cable II Function (Female)
1	TCK	TCK
2	GND	GND
3	TDO	TDO
4	VCC (TRGT) (+1.8V)	VCC (TRGT)
5	TMS	TMS
6	Processor Warm Reset	Processor Warm Reset
7	Reserved	-
8	Reserved	-
9	TDI	TDI
10	GND	GND



Source: Altera UG-01150

Note: Please see the official Intel/USB Download Cable II manual (UG-01150) for more detailed information.

Note: The board uses the following male connector part: Molex 53261-1071
Suggested mating female connector cable: Molex 15134-1000

Note: To use the external JTAG header as master, DIP SW3-2 needs to be turned off (Only board revision 1.1)

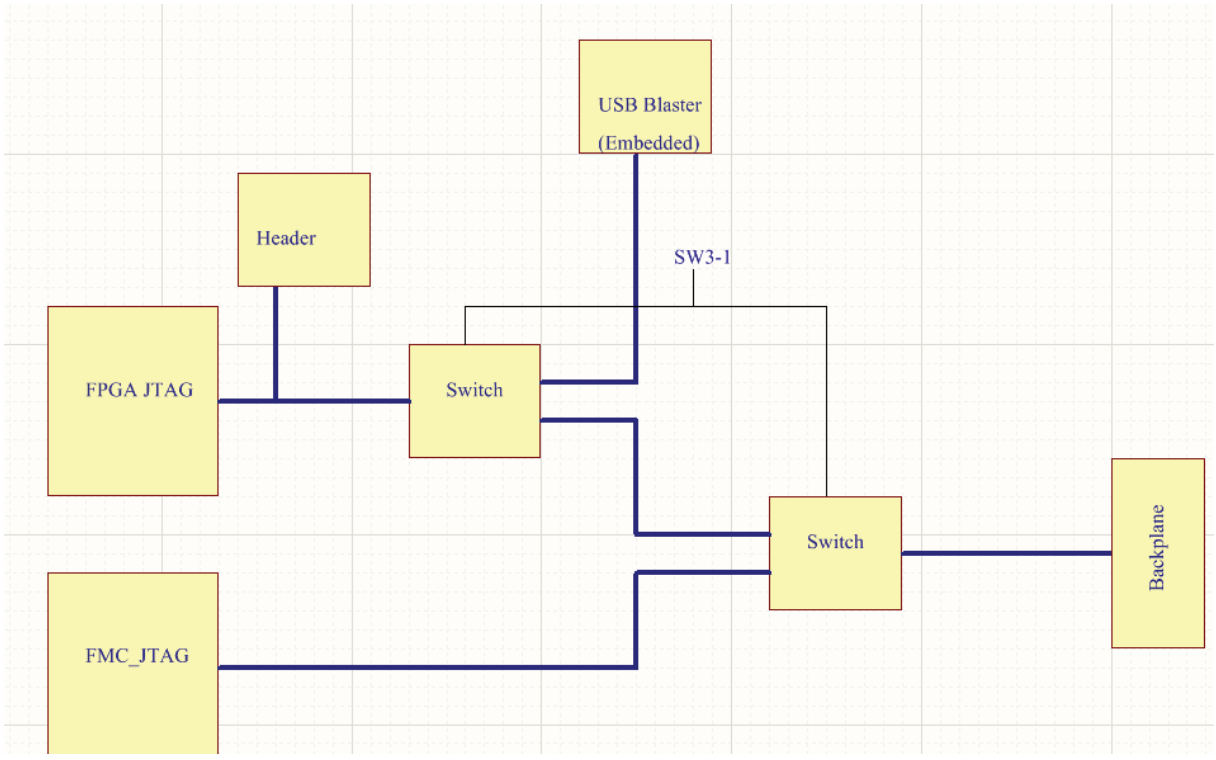
4.2.2 Embedded USB Blaster II

The FMC carrier board implements the USB-Blaster II circuitry on the PCB so that the user can access the FPGA using the front panel USB port. The embedded programmer will be recognized as "NAT-AMC" by the Quartus Programming Tools.

4.2.3 JTAG Multiplexer Logic

The **NAMC-ARRIA10-FMC** implements an electrical circuit to route different JTAG slaves to a specific JTAG master. Possible JTAG slaves are the Arria10 FPGA and the FMC JTAG port. The user can decide whether to route the FPGA JTAG signals or the FMC signals over the backplane to an external JTAG master (e.g. **NAT-JSM**). In case the FPGA JTAG is not routed to the backplane the external JTAG header the embedded USB-Blaster or the external JTAG header is the JTAG master which is directly connected to the Arria10 FPGA. The embedded blaster will be switched off while onboard header adapter cable is connected to the board. The following figure shows a block diagram of the JTAG switching logic which can be controlled with an onboard DIP-Switch (SW3-1).

Figure 12: JTAG switching logic



Note: On hardware revision 1.2 and newer DIP SW3-1 controls both switches simultaneously. DIP SW3-2 has no effect.

4.3 Configuration & Booting

4.3.1 HPS boot sources

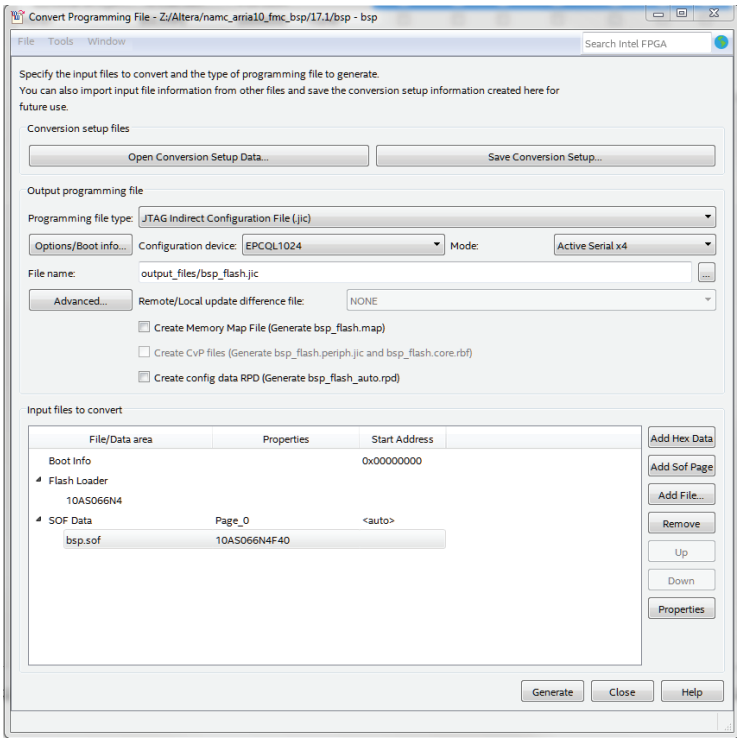
Available processor boot sources on the NAMC-ARRIA10-FMC are the embedded QSPI flash memory or SD-Card. The boot source can be selected by DIP switch SW2-6 (see Table 2: SW2 DIP switch configuration). The default boot setting is to boot from QSPI memory. Depending on the peripherals being used by the HPS it is necessary for the FPGA to be fully or partially configured first. In case the HPS needs to access DRAM and shared IO connections (e.g. SD Card) it is sufficient for the FPGA at least to be configured as "Early IO Release".

4.3.2 FPGA boot sources

The FPGA can be configured using Active Serial (x4) or Passive Serial programming. The boot source can be selected by DIP switch SW2-5 (see Table 2: SW2 DIP switch configuration). When using Active Serial the FPGA will load its configuration file from the EPCQ1024 on board flash memory during start up. When using Passive Serial the FPGA has to be programmed by the HPS. The default boot configuration is Active Serial (x4).

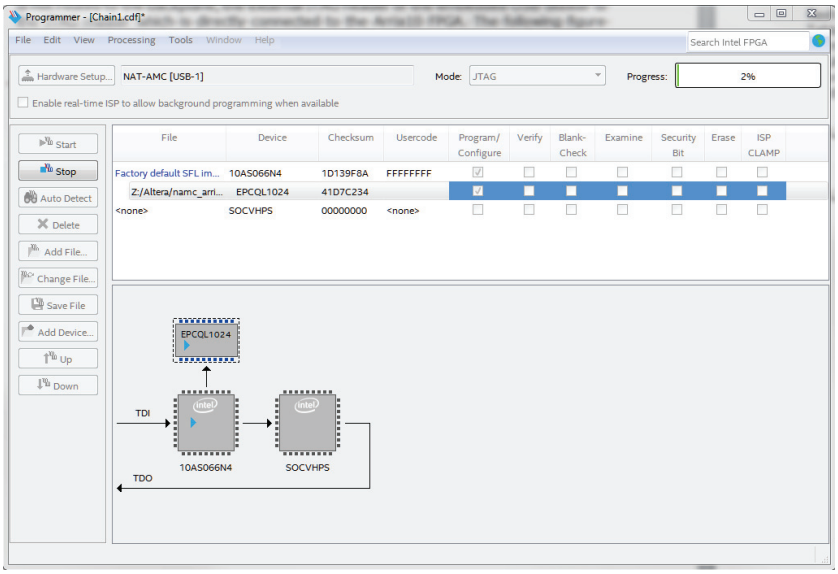
As the EPCQ1024 has no direct connection to the programming header it is necessary to do an indirect JTAG configuration through the FPGA. This can be either done by instantiating the "Intel Serial Flash Loader" IP core from the IP catalogue or by creating an indirect JTAG configuration file ".jic" with the Quartus Tool using "File → Convert Programming Files" dialog. Referring to Figure 13: Create Indirect JTAG configuration File you will have to select the proper flash device and serial flash loader core. Click on "add Sof Page" to add the .sof File prior generated by the Quartus assembler.

Figure 13: Create Indirect JTAG configuration File



Once this is done you should open the Quartus Programmer from the "Tools → Programmer" dialogue. Click on "Auto Detect" to detect the proper FPGA device. Then right click on the FPGA device and choose "Change File". Select the .jic File and enable the "Program / Configure" checkboxes.

Figure 14: Program FLASH memory



4.3.3 HPS Dedicated I/O-Pin-Assignments

The following table shows the HPS dedicated IO pin assignments. Pin functions are fixed and cannot be changed by the user.

Table 7: HPS dedicated I/O Pin Assignments

Pin Name	Pin Location	Function
GPIO2_IO0	E16	QSPI_CLK (HPS Boot Flash)
GPIO2_IO1	H16	QSPI_IO0 (HPS Boot Flash)
GPIO2_IO2	G16	QSPI_CSn (HPS Boot Flash)
GPIO2_IO3	H17	QSPI_IO1 (HPS Boot Flash)
GPIO2_IO4	F15	QSPI_IO2 (HPS Boot Flash)
GPIO2_IO5	K16	QSPI_IO3 (HPS Boot Flash)
GPIO2_IO6	L17	BOOTSEL1 (Controlled by MMC)
GPIO2_IO7	N19	BOOTSEL0 (Controlled by MMC)
GPIO2_IO8	N.C.	-
GPIO2_IO9	N.C.	-
GPIO2_IO10	N.C.	-
GPIO2_IO11	L18	Board LED (Green), Active High
GPIO2_IO12	M17	UART1_TX (To Front USB)
GPIO2_IO13	K17	UART1_RX (To Front USB)

4.3.4 HPS/FPGA Shared I/O Pin Assignments

The following table shows shared pins between the HPS and FPGA. All functions are fixed and cannot be changed by the user.

Table 8: HPS/FPGA shared I/O Pin Assignments Part 1

Pin Name	Pin Location	Function
GPIO0_IO0	D18	SD_DATA0
GPIO0_IO1	E18	SD_CMD
GPIO0_IO2	C19	SD_CLK
GPIO0_IO3	D19	SD_DATA1
GPIO0_IO4	E17	SD_DATA2
GPIO0_IO5	F17	SD_DATA3
GPIO0_IO6	C17	UART_TX (Shared IO Soft UART capable)
GPIO0_IO7	C18	UART_RX (Shared IO Soft UART capable)
GPIO0_IO8	N.C.	-
GPIO0_IO9	N.C.	-
GPIO0_IO10	N.C.	-
GPIO0_IO11	N.C.	-
GPIO0_IO12	H18	Input from DIP SW2-1
GPIO0_IO13	H19	Input from DIP SW2-2
GPIO0_IO14	F18	FPGA_LED1 (Green, Front Panel)
GPIO0_IO15	G17	FPGA_LED0 (Red, Front Panel)
GPIO0_IO16	E20	RESERVED
GPIO0_IO17	F20	RESERVED
GPIO0_IO18	G20	Positive Clock Output (PL_CLK_OUT0_P) from Clock Switch. See Section Board Support Package The board support package is a combination of hardware and software logic which is generated by Intel Design Sofware Quartus Prime Pro 17.0 This tool can be download at the IntelFPGA Download Center. The BSP is production programmed and delivered with the NAMC-ARRIA10-FMC hardware board. The board support package contains the following items: • Quartus 17.0 Example Project, Block Design Level, QSYS • Linux Distribution on SD Card • Instructions how to generate & compile everything (Yocto 2.4.2) The compiled Quartus 17.0 hardware project is stored in the internal QSPI flash together with the U-Boot. The Linux distribution is loaded from SD-Card by U-Boot. The hardware project can be used for board testing as it implements the main hardware interfaces. The hardware project is generatred

		with the Quartus Platform Designer QSYS Pro and then embedded as block symbol file into the top level wrapper. The block design hardware file contains the following IPs:
		
		• Arria10 Hard Processor IP core
		  ○ EMAC0, EMAC1 connected to FPGA fabric
		  ○ Memory interface connected to FPGA fabric (x40, 4 GB)
		  ○ HPS to FPGA memory interface (AXI)
		  ○ HPS IO/s connected to FPGA fabric (SD, I2C, GPIO)
		• Arria10 External Memory Interface Hard IP (x72, 8GB)
		• Arria10 External Memory Interface Hard IP (x40, 4GB)
		• LED (and-connected) to "calibration done" output of memory controllers for visual DRAM operational test
		• Address Span Extender
		  ○ Needed for accessing 16 GB total system memory from HPS
		• Arria10 Hard IP for PCI Express
		  ○ Connected to AMC Port 4-7
		  ○ Configuration: Endpoint, Gen3, x4, Avalon MM 128bit
		• SGMII Subsystem for 1000Base-X Ethernet
		  ○ Connected to HPS EMAC0 and AMC Backplane Port 0
		  ○ Connected to HPS EMAC1 and AMC Backplane Port 1
		• PIO (Parallel IO) IP
		  ○ Connected to HA/LA/HB Pins on FMC
		  ○ Connected to LVDS Trigger Lines on AMC Port 17-20
		• Reset and Clocking IPs
		
		The compiled Linux distribution contains drivers to access and test the hardware:
		
		• Full range memory access (using 2 GB windows)
		• Ethernet on both SGMII Ports
		• GPIO Access on PIO for FMC I/O and backplane I/O loopback testing
		• Kernel I2C driver for reading & editing FMC EEPROM records
		• Kernel I2C driver for PLL's and Clock Distribution Multiplexer

		On request, the following example projects can be provided by N.A.T. • Transceiver Loopback Application (FMC Port DP0-DP9, AMC Ports 0-17) BER validation with Transceiver Toolkit • NAT-FMC-PoE-4GigE example application, with 6x Soft EMAC to SGMII connected to HPS via Avalon Bus Clock Distribution System. Differential HSTL 1.8V Clock Capable Output Pin.
GPIO0_IO19	G21	Positive Clock Output (PL_CLK_OUT0_N) from Clock Switch. See Section Board Support Package The board support package is a combination of hardware and software logic which is generated by Intel Design Sofware Quartus Prime Pro 17.0 This tool can be download at the IntelFPGA Download Center. The BSP is production programmed and delivered with the NAMC-ARRIA10-FMC hardware board. The board support package contains the following items: • Quartus 17.0 Example Project, Block Design Level, QSYS • Linux Distribution on SD Card • Instructions how to generate & compile everything (Yocto 2.4.2) The compiled Quartus 17.0 hardware project is stored in the internal QSPI flash together with the U-Boot. The Linux distribution is loaded from SD-Card by U-Boot. The hardware project can be used for board testing as it implements the main hardware interfaces. The hardware project is generatred with the Quartus Platform Designer QSYS Pro and then embedded as block symbol file into the top level wrapper. The block design hardware file contains the following IPs: • Arria10 Hard Processor IP core o EMAC0, EMAC1 connected to FPGA fabric

		○ Memory interface connected to FPGA fabric (x40, 4 GB) ○ HPS to FPGA memory interface (AXI) ○ HPS IO/s connected to FPGA fabric (SD, I2C, GPIO) • Arria10 External Memory Interface Hard IP (x72, 8GB) • Arria10 External Memory Interface Hard IP (x40, 4GB) • LED (and-connected) to "calibration done" output of memory controllers for visual DRAM operational test • Address Span Extender ○ Needed for accessing 16 GB total system memory from HPS • Arria10 Hard IP for PCI Express ○ Connected to AMC Port 4-7 ○ Configuration: Endpoint, Gen3, x4, Avalon MM 128bit • SGMII Subsystem for 1000Base-X Ethernet ○ Connected to HPS EMAC0 and AMC Backplane Port 0 ○ Connected to HPS EMAC1 and AMC Backplane Port 1 • PIO (Parallel IO) IP ○ Connected to HA/LA/HB Pins on FMC ○ Connected to LVDS Trigger Lines on AMC Port 17-20 • Reset and Clocking IPs The compiled Linux distribution contains drivers to access and test the hardware: • Full range memory access (using 2 GB windows) • Ethernet on both SGMII Ports • GPIO Access on PIO for FMC I/O and backplane I/O loopback testing • Kernel I2C driver for reading & editing FMC EEPROM records • Kernel I2C driver for PLL's and Clock Distribution Multiplexer On request, the following example projects can be provided by N.A.T.

		• Transceiver Loopback Application (FMC Port DP0-DP9, AMC Ports 0-17) BER validation with Transceiver Toolkit • NAT-FMC-PoE-4GigE example application, with 6x Soft EMAC to SGMII connected to HPS via Avalon Bus Clock Distribution System. Differential HSTL 1.8V Clock Capable Output Pin.
GPIO0_IO20	F19	FPGA_RSTn External Reset Input, Active Low. On SX Device this signal is connected to HPS warm reset
GPIO0_IO21	G19	Single Ended Clock input from System PLL (Output 2_P). This always has the same frequency as HPS clock. Default = 25 MHz
GPIO0_IO22	F22	Positive Clock Input (PL_CLK_IN0_P) from Clock Switch. See Section Board Support Package The board support package is a combination of hardware and software logic which is generated by Intel Design Sofware Quartus Prime Pro 17.0 This tool can be download at the IntelFPGA Download Center. The BSP is production programmed and delivered with the NAMC-ARRIA10-FMC hardware board. The board support package contains the following items: • Quartus 17.0 Example Project, Block Design Level, QSYS • Linux Distribution on SD Card • Instructions how to generate & compile everything (Yocto 2.4.2) The compiled Quartus 17.0 hardware project is stored in the internal QSPI flash together with the U-Boot. The Linux distribution is loaded from SD-Card by U-Boot. The hardware project can be used for board testing as it implements the main hardware interfaces. The hardware project is generatred with the Quartus Platform Designer QSYS Pro and then embedded as block symbol file into the top level wrapper. The block design hardware file contains the following IPs: • Arria10 Hard Processor IP core o EMAC0, EMAC1 connected to FPGA fabric

		○ Memory interface connected to FPGA fabric (x40, 4 GB) ○ HPS to FPGA memory interface (AXI) ○ HPS IO/s connected to FPGA fabric (SD, I2C, GPIO) • Arria10 External Memory Interface Hard IP (x72, 8GB) • Arria10 External Memory Interface Hard IP (x40, 4GB) • LED (and-connected) to "calibration done" output of memory controllers for visual DRAM operational test • Address Span Extender ○ Needed for accessing 16 GB total system memory from HPS • Arria10 Hard IP for PCI Express ○ Connected to AMC Port 4-7 ○ Configuration: Endpoint, Gen3, x4, Avalon MM 128bit • SGMII Subsystem for 1000Base-X Ethernet ○ Connected to HPS EMAC0 and AMC Backplane Port 0 ○ Connected to HPS EMAC1 and AMC Backplane Port 1 • PIO (Parallel IO) IP ○ Connected to HA/LA/HB Pins on FMC ○ Connected to LVDS Trigger Lines on AMC Port 17-20 • Reset and Clocking IPs The compiled Linux distribution contains drivers to access and test the hardware: • Full range memory access (using 2 GB windows) • Ethernet on both SGMII Ports • GPIO Access on PIO for FMC I/O and backplane I/O loopback testing • Kernel I2C driver for reading & editing FMC EEPROM records • Kernel I2C driver for PLL's and Clock Distribution Multiplexer On request, the following example projects can be provided by N.A.T.

		• Transceiver Loopback Application (FMC Port DP0-DP9, AMC Ports 0-17) BER validation with Transceiver Toolkit • NAT-FMC-PoE-4GigE example application, with 6x Soft EMAC to SGMII connected to HPS via Avalon Bus Clock Distribution System. Differential HSTL 1.8V Clock Capable Input Pin
GPIO0_IO23	G22	Negative Clock Input (PL_CLK_IN0_N) from Clock Switch. See Section Board Support Package The board support package is a combination of hardware and software logic which is generated by Intel Design Sofware Quartus Prime Pro 17.0 This tool can be download at the IntelFPGA Download Center. The BSP is production programmed and delivered with the NAMC-ARRIA10-FMC hardware board. The board support package contains the following items: • Quartus 17.0 Example Project, Block Design Level, QSYS • Linux Distribution on SD Card • Instructions how to generate & compile everything (Yocto 2.4.2) The compiled Quartus 17.0 hardware project is stored in the internal QSPI flash together with the U-Boot. The Linux distribution is loaded from SD-Card by U-Boot. The hardware project can be used for board testing as it implements the main hardware interfaces. The hardware project is generatred with the Quartus Platform Designer QSYS Pro and then embedded as block symbol file into the top level wrapper. The block design hardware file contains the following IPs: • Arria10 Hard Processor IP core o EMAC0, EMAC1 connected to FPGA fabric o Memory interface connected to FPGA fabric (x40, 4 GB) o HPS to FPGA memory interface (AXI) o HPS IO/s connected to FPGA fabric (SD, I2C, GPIO)

		• Arria10 External Memory Interface Hard IP (x72, 8GB)
		• Arria10 External Memory Interface Hard IP (x40, 4GB)
		• LED (and-connected) to "calibration done" output of memory controllers for visual DRAM operational test
		• Address Span Extender
		  ○ Needed for accessing 16 GB total system memory from HPS
		• Arria10 Hard IP for PCI Express
		  ○ Connected to AMC Port 4-7
		  ○ Configuration: Endpoint, Gen3, x4, Avalon MM 128bit
		• SGMII Subsystem for 1000Base-X Ethernet
		  ○ Connected to HPS EMAC0 and AMC Backplane Port 0
		  ○ Connected to HPS EMAC1 and AMC Backplane Port 1
		• PIO (Parallel IO) IP
		  ○ Connected to HA/LA/HB Pins on FMC
		  ○ Connected to LVDS Trigger Lines on AMC Port 17-20
		• Reset and Clocking IPs
		
		The compiled Linux distribution contains drivers to access and test the hardware:
		
		• Full range memory access (using 2 GB windows)
		• Ethernet on both SGMII Ports
		• GPIO Access on PIO for FMC I/O and backplane I/O loopback testing
		• Kernel I2C driver for reading & editing FMC EEPROM records
		• Kernel I2C driver for PLL's and Clock Distribution Multiplexer
		
		On request, the following example projects can be provided by N.A.T.
		
		• Transceiver Loopback Application (FMC Port DP0-DP9, AMC Ports 0-17) BER validation with Transceiver Toolkit
		• NAT-FMC-PoE-4GigE example application, with 6x Soft EMAC to SGMII connected to HPS via Avalon Bus

		Clock Distribution System. Differential HSTL 1.8V Clock Capable Input Pin

Table 9: HPS/FPGA shared I/O Pin Assignments Part 2

Pin Name	Pin Location	Function
GPIO1_IO2	H22	I^2C Data Line to Peripherals (SDA)
GPIO1_IO3	H21	I^2C Clock Line to Peripherals (SCL)
GPIO1_IO6	J18	Optional I^2C Request. Drive this signal low in order to get exclusive access to the multi master FMC I2C management bus.
GPIO1_IO7	J19	RESERVED
GPIO1_IO8	H23	RESERVED
GPIO1_IO9	J23	RESERVED
GPIO1_IO10	K21	RESERVED
GPIO1_IO11	K20	RESERVED
GPIO1_IO12	L20	RESERVED
GPIO1_IO13	M20	RESERVED
GPIO1_IO14	N20	RESERVED
GPIO1_IO15	P20	RESERVED
GPIO1_IO16	K23	RESERVED
GPIO1_IO17	L23	RESERVED
GPIO1_IO18	N23	RESERVED
GPIO1_IO19	N22	RESERVED
GPIO1_IO20	K22	RESERVED
GPIO1_IO21	L22	RESERVED
GPIO1_IO22	M22	RESERVED
GPIO1_IO23	M21	RESERVED

4.4 Creating HPS Bootloader Image

The HPS bootloader (U-Boot) can be generated using the "bsp-editor". The BSP editor is part of the SoC-EDS (Embedded Design Suite) Tools chain. To call this utility open the SoC-EDS-Command shell and type "bsp-editor". The bsp-editor needs the hardware handoff files located in the project directory "hps_isw_handoff" to generate the bootloader device tree and binaries.

Note: In order to use Ethernet access from U-Boot you will have to use modified U-Boot binaries by NAT as the standard code does not include drivers for the SGMII to HPS Ethernet bridge IP.

Note: Windows compilation of U-Boot is not possible. Use the Linux Toolchain instead.

Use the following command from the SoC-EDS-Command-Shell to program the HPS QSPI memory:

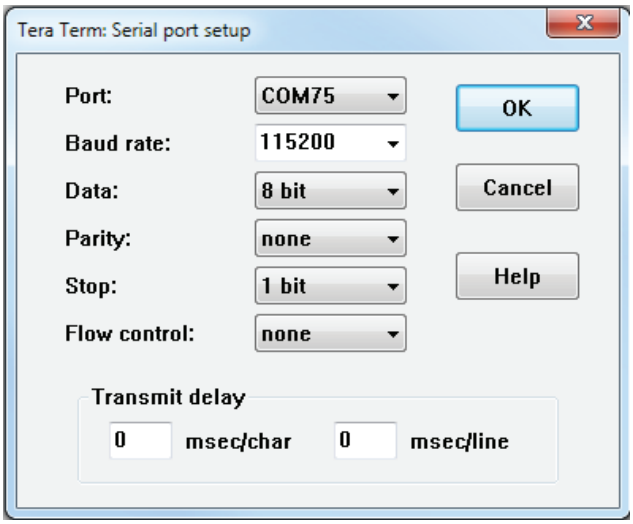
```
quartus_hps --boot=18 --cable=1 --operation=P uboot_w_dtb-mkpimage.bin
```

4.5 Serial Console

The modules front panel gives access to two COM ports which are useable with any USB host. When connecting the USB cable the host should detect a UART to USB device (CP2105) which serves to independent COM ports for serial access. One COM port is dedicated to the FPGA/HPS UART and the other one is occupied by the MMC management controller. In most cases the MMC console is not needed in case there are no issues with the board initialization or the user may want to use the FMC EEPROM wizard *(*see section ***7)***

The FPGA/HPS UART port is generally being used by any operating system which runs on the HPS or FPGA, e.g. Linux Command Line. To access the COM port you will have to use a serial terminal like Tera Term or PuttY. The settings for both ports are shown below.

Figure 15: Serial Console COM Port Settings



5 Board Support Package

The board support package is a combination of hardware and software logic which is generated by Intel Design Sofware Quartus Prime Pro 17.0 This tool can be download at the IntelFPGA Download Center. The BSP is production programmed and delivered with the NAMC-ARRIA10-FMC hardware board.

The board support package contains the following items:

- Quartus 17.0 Example Project, Block Design Level, QSYS
- Linux Distribution on SD Card
- Instructions how to generate & compile everything (Yocto 2.4.2)

The compiled Quartus 17.0 hardware project is stored in the internal QSPI flash together with the U-Boot. The Linux distribution is loaded from SD-Card by U-Boot.

The hardware project can be used for board testing as it implements the main hardware interfaces. The hardware project is generatred with the Quartus Platform Designer QSYS Pro and then embedded as block symbol file into the top level wrapper. The block design hardware file contains the following IPs:

- Arria10 Hard Processor IP core
  - EMAC0, EMAC1 connected to FPGA fabric
  - Memory interface connected to FPGA fabric (x40, 4 GB)
  - HPS to FPGA memory interface (AXI)
  - HPS IO/s connected to FPGA fabric (SD, I2C, GPIO)
- Arria10 External Memory Interface Hard IP (x72, 8GB)
- Arria10 External Memory Interface Hard IP (x40, 4GB)
- LED (and-connected) to "calibration done" output of memory controllers for visual DRAM operational test
- Address Span Extender
  - Needed for accessing 16 GB total system memory from HPS
- Arria10 Hard IP for PCI Express
  - Connected to AMC Port 4-7
  - Configuration: Endpoint, Gen3, x4, Avalon MM 128bit
- SGMII Subsystem for 1000Base-X Ethernet
  - Connected to HPS EMAC0 and AMC Backplane Port 0
  - Connected to HPS EMAC1 and AMC Backplane Port 1
- PIO (Parallel IO) IP
  - Connected to HA/LA/HB Pins on FMC
  - Connected to LVDS Trigger Lines on AMC Port 17-20
- Reset and Clocking IPs

The compiled Linux distribution contains drivers to access and test the hardware:

- Full range memory access (using 2 GB windows)
- Ethernet on both SGMII Ports
- GPIO Access on PIO for FMC I/O and backplane I/O loopback testing
- Kernel I2C driver for reading & editing FMC EEPROM records
- Kernel I2C driver for PLL's and Clock Distribution Multiplexer

On request, the following example projects can be provided by N.A.T.

- Transceiver Loopback Application (FMC Port DP0-DP9, AMC Ports 0-17) BER validation with Transceiver Toolkit
- NAT-FMC-PoE-4GigE example application, with 6x Soft EMAC to SGMII connected to HPS via Avalon Bus

6 Clock Distribution System

The clocks on the board get generated using two SiLab5347 PLL's modules. They are called "System PLL" and "Application PLL". The System PLL is mainly responsible for setting up the reference clocks that are needed for the FPGA to boot and for running basic communication protocols such as Gigabit Ethernet and PCI Express. Also the System PLL gives the reference clock for the second Application PLL. A Stratum III reference clock is used by the first PLL to lock to a stable frequency and serve it as base to the second application PLL as input source. The application PLL is mainly responsible for setting up reference clocks for the advanced AMC fabrics (Port 12-15) and all the clocks that are referred to the FMC.

On the Prototype board all clocks get initialized by the MMC's static configuration during start up. As the PLL's management bus (I^2C) is also connected to the FPGA the whole configuration of the PLL can be adjusted by the FPGA. The SiLabs Clock Builder Pro Tool can be used to generate an initialization file. By default, the clocks are configured by the MMC as follows:

Table 10: PLL Clocks

System PLL (I2C: 0x6D)	Application PLL (I2C: 0x6C)
Output 0: 100 MHz	Output 0: 125 MHz
Output 1: 100 MHz	Output 1: 125 MHz
Output 2: 25 MHz	Output 2: 125 MHz
Output 3: 100 MHz	Output 3: 125 MHz
Output 4: 125 MHz	Output 4: 125 MHz
Output 5: 100 MHz	Output 5: 125 MHz
Output 6: 50 MHz	Output 6: 125 MHz
Output 7: 200 MHz	Output 7: 125 MHz

The clock distribution of the system can be configured with the IDT clock crossbar switch (IDT8V54816). Any input can be connected with any output. The clock switch is also reachable by the FPGA I^2C management bus at address (0x5D. Figure 16: Clock Distribution System gives an overview of the whole clock distribution network.

Figure 16: Clock Distribution System

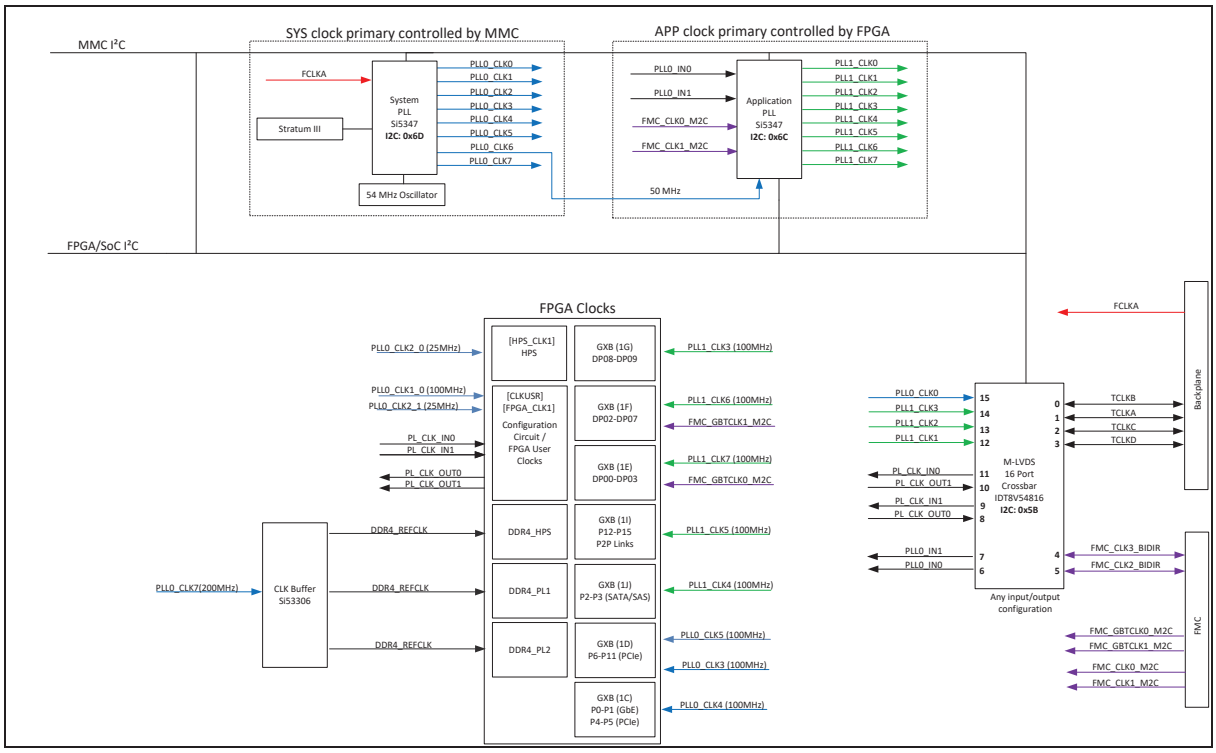


Table 11: General Purpose Clock Inputs/Outputs from/to IDT8V54816

Clock Pin Name	FPGA Pin	I/O Standard	Direction
PL_CLK_IN0_P	F22	Differential HSTL 1.8V	Input
PL_CLK_IN0_N	G22	Differential HSTL 1.8V	Input
PL_CLK_IN1_P	P11	LVDS (VADJ >= 1.8V)*	Input
PL_CLK_IN1_N	R11	LVDS (VADJ >= 1.8V)*	Input
PL_CLK_OUT0_P	G20	Differential HSTL 1.8V	Output
PL_CLK_OUT0_N	G21	Differential HSTL 1.8V	Output
PL_CLK_OUT1_P	P8	LVDS (VADJ >= 1.8V)*	Output
PL_CLK_OUT1_N	R8	LVDS (VADJ >= 1.8V)*	Output

* For LVDS operation VADJ voltage must be greater than 1.8V.

7 FMC Operation

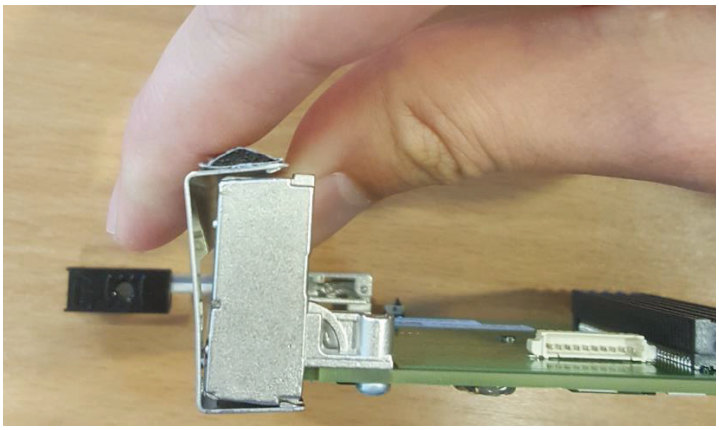
7.1 Supported FMC's

All FMCs compliant to VITA 57.1 are supported. VADJ and VIO_B_M2C are limited to 1.8V.

7.2 Installing a FMC Module

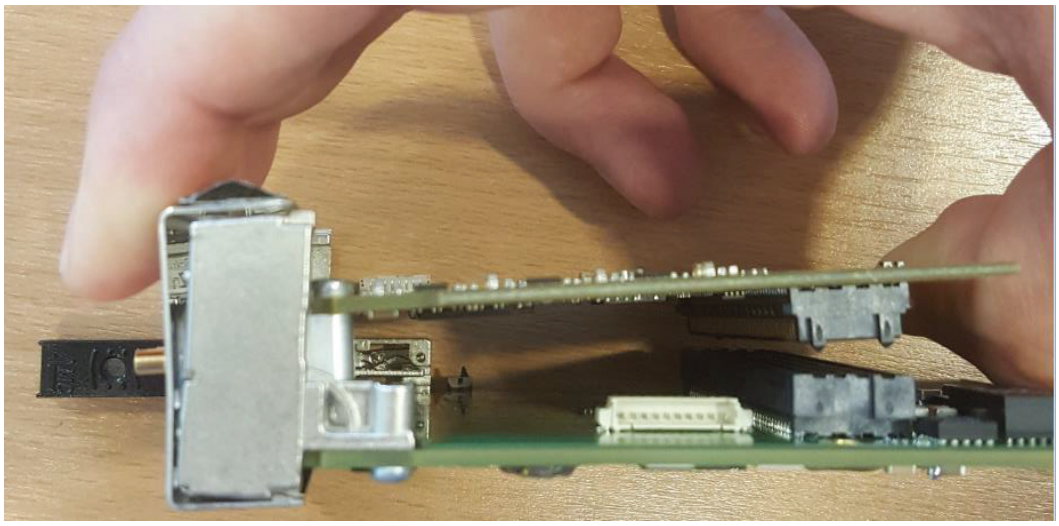
When applying a FMC module it could be necessary to remove or to untighten the front metal in order for the FMC front to fit into the cutout.

Figure 17: Installing FMC Module Part 1



After fitting the FMC module to the carrier, the front panel needs to be restored.

Figure 18: Installing FMC Module Part 2



7.3 FMC EEPROM Wizard

Per default the carrier will try to parse the FMC FRU records from the modules EEPROM contents to set the carrier's power supply and clock direction. In case there is an FMC without records there are two options:

1) Generate and program the records with the carrier. Set SW2-3 to "ON".
2) Skip FMC EEPROM parsing with setting SW2-4 to ON.

Warning: In this case a default VADJ voltage of 1.8V gets applied to the FMC module. Please check the capabilities of your FMC in this case.

In case the records for the FMC should be generated with the carrier the Micro USB cable has to be connected to the front plate's USB port. The host should detect a USB-Hub and two COM ports. The first enumerated COM port is the serial console of the MMC. Open it with a tool (e.g. TeraTerm) and set the COM settings according to Figure 15: Serial Console COM Port Settings.

The MMC has to be rebooted with triggering the HS-Handle. The console output should output the following line:

```
Press any key to generate FMC FRU file ... 5.0
```

Within five seconds time press any key to enter the FMC programming mode. This mode is guided and will lead through the steps to program the FMC records. At the end of the wizard it will ask to program the EEPROM file of the FMC.

8 Troubleshooting

1) quartus_hps fails programming the QSPI flash.

Set down the JTAG frequency of the blaster programming cable.

Example:

```
jtagconfig setparam <cable> <TCK>
```

Example:

```
jtagconfig --setparam 1 JtagClock 6M
```

2) quartus_hps is unable to access the QSPI flash.

Set SW2-6 to "ON" in order to set the BSEL to QPSI. Instruct quartus_hps to trigger a cold reset before accessing the QSPI.

Example:

```
quartus_hps --boot=18 --cable=1 --operation=P uboot_w_dtb-mkpimage.bin
```

9 Known Limitations

1) For PCB Versions smaller V1.2: Embedded USB Blaster will not work properly with Altera Tools Signal-Tap and Transceiver Toolkit. HPS Boot-Flash programming may fail.
2) For PCB Versions smaller V 1.4: M-LVDS clock inputs and outputs connected to FPGA banks 2L with IDT clock multiplexer (PL_CLK_IN & PL_CLK_OUT) will not work.
3) For industrial temperature board configuration the maximum amount of DRAM is reduced due to DRAM chip availability
    a. HPS DDR bank (x40) is limited to 2 GB
    b. PL DDRA (x72) is limited to 4 GB
    c. PL DDRB (x40) is limited to 2 GB

10 FMC-Connector I/O-Pin-Map

Figure 19: FMC Connector IO Assignments

FMC Pin	FMC Label	FPGA Bank / Transceiver CH	FPGA VCCO	FPGA Pin Number
A1	GND			
A2	DP1_M2C_P	1E, CH5	GXB, HSSI	AD31
A3	DP1_M2C_N	1E, CH5	GXB, HSSI	AD30
A4	GND	-	-	-
A5	GND	-	-	-
A6	DP2_M2C_P	1F, CH0	GXB, HSSI	AD35
A7	DP2_M2C_N	1F, CH0	GXB, HSSI	AD34
A8	GND	-	-	-
A9	GND	-	-	-
A10	DP3_M2C_P	1F, CH1	GXB, HSSI	AC33
A11	DP3_M2C_N	1F, CH1	GXB, HSSI	AC32
A12	GND	-	-	-
A13	GND	-	-	-
A14	DP4_M2C_P	1F, CH2	GXB, HSSI	AB31
A15	DP4_M2C_N	1F, CH2	GXB, HSSI	AB30
A16	GND	-	-	-
A17	GND	-	-	-
A18	DP5_M2C_P	1F, CH3	GXB, HSSI	AB35
A19	DP5_M2C_N	1F, CH3	GXB, HSSI	AB34
A20	GND	-	-	-
A21	GND	-	-	-
A22	DP1_C2M_P	1E, CH5	GXB, HSSI	AF39
A23	DP1_C2M_N	1E, CH5	GXB, HSSI	AF38
A24	GND	-	-	-
A25	GND	-	-	-
A26	DP2_C2M_P	1F, CH0	GXB, HSSI	AE37
A27	DP2_C2M_N	1F, CH0	GXB, HSSI	AE36
A28	GND	-	-	-
A29	GND	-	-	-
A30	DP3_C2M_P	1F, CH3	GXB, HSSI	AD39
A31	DP3_C2M_N	1F, CH3	GXB, HSSI	AD38
A32	GND	-	-	-
A33	GND	-	-	-
A34	DP4_C2M_P	1F, CH2	GXB, HSSI	AC37
A35	DP4_C2M_N	1F, CH2	GXB, HSSI	AC36
A36	GND	-	-	-
A37	GND	-	-	-
A38	DP5_C2M_P	1F, CH3	GXB, HSSI	AB39
A39	DP5_C2M_N	1F, CH3	GXB, HSSI	AB38
A40	GND	-	-	-

FMC Pin	FMC Label	FPGA Bank / Transceiver CH	FPGA VCCO	FPGA Pin Number
B1	CLK_DIR	-	-	-
B2	GND	-	-	-
B3	GND	-	-	-
B4	DP9_M2C_P	1G, CH1	GXB, HSSI	W33
B5	DP9_M2C_N	1G, CH1	GXB, HSSI	W32
B6	GND	-	-	-
B7	GND	-	-	-
B8	DP8_M2C_P	1G, CH0	GXB, HSSI	Y31
B9	DP8_M2C_N	1G, CH0	GXB, HSSI	Y30
B10	GND	-	-	-
B11	GND	-	-	-
B12	DP7_M2C_P	1F, CH5	GXB, HSSI	Y35
B13	DP7_M2C_N	1F, CH5	GXB, HSSI	Y34
B14	GND	-	-	-
B15	GND	-	-	-
B16	DP6_M2C_P	1F, CH4	GXB, HSSI	AA33
B17	DP6_M2C_N	1F, CH4	GXB, HSSI	AA32
B18	GND	-	-	-
B19	GND	-	-	-
B20	GBTCLK1_M2C_P	1F, CHT	GXB, HSSI	AA29
B21	GBTCLK1_M2C_N	1F, CHT	GXB, HSSI	AA28
B22	GND	-	-	-
B23	GND	-	-	-
B24	DP9_C2M_P	1G, CH1	GXB, HSSI	V39
B25	DP9_C2M_N	1G, CH1	GXB, HSSI	V38
B26	GND	-	-	-
B27	GND	-	-	-
B28	DP8_C2M_P	1G, CH0	GXB, HSSI	W37
B29	DP8_C2M_N	1G, CH0	GXB, HSSI	W36
B30	GND	-	-	-
B31	GND	-	-	-
B32	DP7_C2M_P	1F, CH5	GXB, HSSI	Y39
B33	DP7_C2M_N	1F, CH5	GXB, HSSI	Y38
B34	GND	-	-	-
B35	GND	-	-	-
B36	DP6_C2M_P	1F, CH4	GXB, HSSI	AA37
B37	DP6_C2M_N	1F, CH4	GXB, HSSI	AA36
B38	GND	-	-	-
B39	GND	-	-	-
B40	RES0	NC	-	-

FMC Pin	FMC Label	FPGA Bank / Transceiver CH	FPGA VCCO	FPGA Pin Number
C1	GND	-		
C2	DP0_C2M_P	1E, CH4	GXB, HSSI	AG37
C3	DP0_C2M_N	1E, CH4	GXB, HSSI	AG36
C4	GND			
C5	GND			
C6	DP0_M2C_P	1E, CH4	GXB, HSSI	AE33
C7	DP0_M2C_N	1E, CH4	GXB, HSSI	AE32
C8	GND			
C9	GND			
C10	LA06_P	3G	VADJ	E8
C11	LA06_N	3G	VADJ	F8
C12	GND			
C13	GND			
C14	LA10_P	3G	VADJ	B7
C15	LA10_N	3G	VADJ	C7
C16	GND			
C17	GND			
C18	LA14_P	3G	VADJ	A5
C19	LA14_N	3G	VADJ	B5
C20	GND	-	-	-
C21	GND	-	-	-
C22	LA18_P_CC	3F	VADJ	J3
C23	LA18_N_CC	3F	VADJ	K3
C24	GND	-	-	-
C25	GND	-	-	-
C26	LA27_P	3F	VADJ	K7
C27	LA27_N	3F	VADJ	L7
C28	GND	-	-	-
C29	GND	-	-	-
C30	SCL	2L	+1.8V	H21
C31	SDA	2L	+1.8V	H22
C32	GND	-	-	-
C33	GND	-	-	-
C34	GA0	-	-	-
C35	12POV	-	-	-
C36	GND	-	-	-
C37	12POV	-	-	-
C38	GND	-	-	-
C39	3P3V	-	-	-
C40	GND	-	-	-

FMC Pin	FMC Label	FPGA Bank / Transceiver CH	FPGA VCCO	FPGA Pin Number
D1	PG_C2M	-	-	-
D2	GND	-	-	-
D3	GND	-	-	-
D4	GBTCLK0_M2C_P	1E, CHT	GXB, HSSI	AE29
D5	GBTCLK0_M2C_N	1E, CHT	GXB, HSSI	AE28
D6	GND	-	-	-
D7	GND	-	-	-
D8	LA01_P_CC	3G	VADJ	E5
D9	LA01_N_CC	3G	VADJ	F5
D10	GND	-	-	-
D11	LA05_P	3G	VADJ	F9
D12	LA05_N	3G	VADJ	G9
D13	GND	-	-	-
D14	LA09_P	3G	VADJ	B6
D15	LA09_N	3G	VADJ	C6
D16	GND	-	-	-
D17	LA13_P	3G	VADJ	D4
D18	LA13_N	3G	VADJ	D5
D19	GND	-	-	-
D20	LA17_P_CC	3F	VADJ	N6
D21	LA17_N_CC	3F	VADJ	N7
D22	GND	-	-	-
D23	LA23_P	3F	VADJ	M6
D24	LA23_N	3F	VADJ	M7
D25	GND	-	-	-
D26	LA26_P	3F	VADJ	F4
D27	LA26_N	3F	VADJ	G4
D28	GND	-	-	-
D29	TCK	-	-	-
D30	TDI	-	-	-
D31	TDO	-	-	-
D32	3P3VAUX	-	-	-
D33	TMS	-	-	-
D34	TRST_L	-	-	-
D35	GA1	-	-	-
D36	3P3V	-	-	-
D37	GND	-	-	-
D38	3P3V	-	-	-
D39	GND	-	-	-
D40	3P3V	-	-	-

FMC Pin	FMC Label	FPGA Bank / Transceiver CH	FPGA VCCO	FPGA Pin Number
E1	GND	-	-	-
E2	HA01_P_CC	3H	VADJ	E12
E3	HA01_N_CC	3H	VADJ	E13
E4	GND	-	-	-
E5	GND	-	-	-
E6	HA05_P	3H	VADJ	C13
E7	HA05_N	3H	VADJ	D13
E8	GND	-	-	-
E9	HA09_P	3H	VADJ	G14
E10	HA09_N	3H	VADJ	D14
E11	GND	-	-	-
E12	HA13_P	3H	VADJ	H12
E13	HA13_N	3H	VADJ	H13
E14	GND	-	-	-
E15	HA16_P	3H	VADJ	F12
E16	HA16_N	3H	VADJ	G12
E17	GND	-	-	-
E18	HA20_P	3H	VADJ	D10
E19	HA20_N	3H	VADJ	E10
E20	GND	-	-	-
E21	HB03_P	2A	VIOB_M2C	AJ19
E22	HB03_N	2A	VIOB_M2C	AH19
E23	GND	-	-	-
E24	HB05_P	2A	VIOB_M2C	AK16
E25	HB05_N	2A	VIOB_M2C	AK17
E26	GND	-	-	-
E27	HB09_P	2A	VIOB_M2C	AN17
E28	HB09_N	2A	VIOB_M2C	AM17
E29	GND	-	-	-
E30	HB13_P	2A	VIOB_M2C	AP19
E31	HB13_N	2A	VIOB_M2C	AN19
E32	GND	-	-	-
E33	HB19_P	2I	VIOB_M2C	AM22
E34	HB19_N	2I	VIOB_M2C	AL22
E35	GND	-	-	-
E36	HB21_P	2I	VIOB_M2C	AN21
E37	HB21_N	2I	VIOB_M2C	AN22
E38	GND	-	-	-
E39	VADJ	-	-	-
E40	GND	-	-	-

FMC Pin	FMC Label	FPGA Bank / Transceiver CH	FPGA VCCO	FPGA Pin Number
F1	PG_M2C	-	-	-
F2	GND	-	-	-
F3	GND	-	-	-
F4	HA00_P_CC	3H	VADJ	C11
F5	HA00_N_CC	3H	VADJ	C12
F6	GND	-	-	-
F7	HA04_P	3H	VADJ	F10
F8	HA04_N	3H	VADJ	G10
F9	GND	-	-	-
F10	HA08_P	3H	VADJ	C14
F11	HA08_N	3H	VADJ	D14
F12	GND	-	-	-
F13	HA12_P	3H	VADJ	D11
F14	HA12_N	3H	VADJ	E11
F15	GND	-	-	-
F16	HA15_P	3H	VADJ	B11
F17	HA15_N	3H	VADJ	B12
F18	GND	-	-	-
F19	HA19_P	3H	VADJ	A9
F20	HA19_N	3H	VADJ	B9
F21	GND	-	-	-
F22	HB02_P	2A	VIOB_M2C	AL17
F23	HB02_N	2A	VIOB_M2C	AK18
F24	GND	-	-	-
F25	HB04_P	2A	VIOB_M2C	AJ16
F26	HB04_N	2A	VIOB_M2C	AH17
F27	GND	-	-	-
F28	HB08_P	2A	VIOB_M2C	AM19
F29	HB08_N	2A	VIOB_M2C	AM20
F30	GND	-	-	-
F31	HB12_P	2A	VIOB_M2C	AT17
F32	HB12_N	2A	VIOB_M2C	AR17
F33	GND	-	-	-
F34	HB16_P	2A	VIOB_M2C	AU16
F35	HB16_N	2A	VIOB_M2C	AU17
F36	GND	-	-	-
F37	HB20_P	2I	VIOB_M2C	AR21
F38	HB20_N	2I	VIOB_M2C	AP21
F39	GND	-	-	-
F40	VADJ	-	-	-

FMC Pin	FMC Label	FPGA Bank / Transceiver CH	FPGA VCCO	FPGA Pin Number
G1	GND	-	-	-
G2	CLK1_M2C_P	-	-	-
G3	CLK1_M2C_N	-	-	-
G4	GND	-	-	-
G5	GND	-	-	-
G6	LA00_P_CC	3G	VADJ	H8
G7	LA00_N_CC	3G	VADJ	H9
G8	GND	-	-	-
G9	LA03_P	3G	VADJ	J8
G10	LA03_N	3G	VADJ	K8
G11	GND	-	-	-
G12	LA08_P	3G	VADJ	C8
G13	LA08_N	3G	VADJ	D8
G14	GND	-	-	-
G15	LA12_P	3G	VADJ	A4
G16	LA12_N	3G	VADJ	B4
G17	GND	-	-	-
G18	LA16_P	3G	VADJ	C3
G19	LA16_N	3G	VADJ	C4
G20	GND	-	-	-
G21	LA20_P	3F	VADJ	K5
G22	LA20_N	3F	VADJ	K6
G23	GND	-	-	-
G24	LA22_P	3F	VADJ	L4
G25	LA22_N	3F	VADJ	M4
G26	GND	-	-	-
G27	LA25_P	3F	VADJ	E3
G28	LA25_N	3F	VADJ	F3
G29	GND	-	-	-
G30	LA29_P	3F	VADJ	E1
G31	LA29_N	3F	VADJ	E2
G32	GND	-	-	-
G33	LA31_P	3F	VADJ	F2
G34	LA31_N	3F	VADJ	G2
G35	GND	-	-	-
G36	LA33_P	3F	VADJ	H1
G37	LA33_N	3F	VADJ	J1
G38	GND	-	-	-
G39	VADJ	-	-	-
G40	GND	-	-	-

FMC Pin	FMC Label	FPGA Bank / Transceiver CH	FPGA VCCO	FPGA Pin Number
H1	VREF_A_M2C	-	-	-
H2	PRSNT_M2C_L	-	-	-
H3	GND	-	-	-
H4	CLK0_M2C_P	-	-	-
H5	CLK0_M2C_N	-	-	-
H6	GND	-	-	-
H7	LA02_P	3G	VADJ	G7
H8	LA02_N	3G	VADJ	H7
H9	GND	-	-	-
H10	LA04_P	3G	VADJ	G5
H11	LA04_N	3G	VADJ	G6
H12	GND	-	-	-
H13	LA07_P	3G	VADJ	E7
H14	LA07_N	3G	VADJ	F7
H15	GND	-	-	-
H16	LA11_P	3G	VADJ	D6
H17	LA11_N	3G	VADJ	E6
H18	GND	-	-	-
H19	LA15_P	3G	VADJ	C2
H20	LA15_N	3G	VADJ	D3
H21	GND	-	-	-
H22	LA19_P	3F	VADJ	J4
H23	LA19_N	3F	VADJ	J5
H24	GND	-	-	-
H25	LA21_P	3F	VADJ	H3
H26	LA21_N	3F	VADJ	H4
H27	GND	-	-	-
H28	LA24_P	3F	VADJ	L2
H29	LA24_N	3F	VADJ	L3
H30	GND	-	-	-
H31	LA28_P	3F	VADJ	C1
H32	LA28_N	3F	VADJ	D1
H33	GND	-	-	-
H34	LA30_P	3F	VADJ	G1
H35	LA30_N	3F	VADJ	H2
H36	GND	-	-	-
H37	LA32_P	3F	VADJ	K1
H38	LA32_N	3F	VADJ	K2
H39	GND	-	-	-
H40	VADJ	-	-	-

FMC Pin	FMC Label	FPGA Bank / Transceiver CH	FPGA VCCO	FPGA Pin Number
I1	GND	-	-	-
I2	CLK3_BIDIR_P	-	-	-
I3	CLK3_BIDIR_P	-	-	-
I4	GND	-	-	-
I5	GND	-	-	-
I6	HA03_P	3H	VADJ	P14
I7	HA03_N	3H	VADJ	P15
I8	GND	-	-	-
I9	HA07_P	3H	VADJ	L12
I10	HA07_N	3H	VADJ	L13
I11	GND	-	-	-
I12	HA11_P	3H	VADJ	K12
I13	HA11_N	3H	VADJ	K13
I14	GND	-	-	-
I15	HA14_P	3H	VADJ	G11
I16	HA14_N	3H	VADJ	H11
I17	GND	-	-	-
I18	HA18_P	3H	VADJ	A10
I19	HA18_N	3H	VADJ	B10
I20	GND	-	-	-
I21	HA22_P	3H	VADJ	A7
I22	HA22_N	3H	VADJ	A8
I23	GND	-	-	-
I24	HB01_P	2A	VIOB_M2C	AJ18
I25	HB01_N	2A	VIOB_M2C	AH18
I26	GND	-	-	-
I27	HB07_P	2A	VIOB_M2C	AL18
I28	HB07_N	2A	VIOB_M2C	AL19
I29	GND	-	-	-
I30	HB11_P	2A	VIOB_M2C	AR16
I31	HB11_N	2A	VIOB_M2C	AP16
I32	GND	-	-	-
I33	HB15_P	2A	VIOB_M2C	AU20
I34	HB15_N	2A	VIOB_M2C	AT20
I35	GND	-	-	-
I36	HB18_P	2I	VIOB_M2C	AR23
I37	HB18_N	2I	VIOB_M2C	AL22
I38	GND	-	-	-
I39	VIO_B_M2C	-	-	-
I40	GND	-	-	-

FMC Pin	FMC Label	FPGA Bank / Transceiver CH	FPGA VCCO	FPGA Pin Number
J1	GND	-	-	-
J2	CLK3_BIDIR_P	-	-	-
J3	CLK3_BIDIR_P	-	-	-
J4	GND	-	-	-
J5	GND	-	-	-
J6	HA03_P	3H	VADJ	P14
J7	HA03_N	3H	VADJ	P15
J8	GND	-	-	-
J9	HA07_P	3H	VADJ	L12
J10	HA07_N	3H	VADJ	L13
J11	GND	-	-	-
J12	HA11_P	3H	VADJ	K12
J13	HA11_N	3H	VADJ	K13
J14	GND	-	-	-
J15	HA14_P	3H	VADJ	G11
J16	HA14_N	3H	VADJ	H11
J17	GND	-	-	-
J18	HA18_P	3H	VADJ	A10
J19	HA18_N	3H	VADJ	B10
J20	GND	-	-	-
J21	HA22_P	3H	VADJ	A7
J22	HA22_N	3H	VADJ	A8
J23	GND	-	-	-
J24	HB01_P	2A	VIOB_M2C	AJ18
J25	HB01_N	2A	VIOB_M2C	AH18
J26	GND	-	-	-
J27	HB07_P	2A	VIOB_M2C	AL18
J28	HB07_N	2A	VIOB_M2C	AL19
J29	GND	-	-	-
J30	HB11_P	2A	VIOB_M2C	AR16
J31	HB11_N	2A	VIOB_M2C	AP16
J32	GND	-	-	-
J33	HB15_P	2A	VIOB_M2C	AU20
J34	HB15_N	2A	VIOB_M2C	AT20
J35	GND	-	-	-
J36	HB18_P	2I	VIOB_M2C	AR23
J37	HB18_N	2I	VIOB_M2C	AL22
J38	GND	-	-	-
J39	VIO_B_M2C	-	-	-
J40	GND	-	-	-

FMC Pin	FMC Label	FPGA Bank / Transceiver CH	FPGA VCCO	FPGA Pin Number
K1	VREF_B_M2C	-	-	-
K2	GND	-	-	-
K3	GND	-	-	-
K4	CLK2_BIDIR_P	-	-	-
K5	CLK2_BIDIR_N	-	-	-
K6	GND	-	-	-
K7	HA02_P	3H	VADJ	M14
K8	HA02_N	3H	VADJ	N14
K9	GND	-	-	-
K10	HA06_P	3H	VADJ	L14
K11	HA06_N	3H	VADJ	L15
K12	GND	-	-	-
K13	HA10_P	3H	VADJ	J13
K14	HA10_N	3H	VADJ	J14
K15	GND	-	-	-
K16	HA17_P_CC	3H	VADJ	F13
K17	HA17_N_CC	3H	VADJ	F14
K18	GND	-	-	-
K19	HA21_P	3H	VADJ	A12
K20	HA21_N	3H	VADJ	A13
K21	GND	-	-	-
K22	HA23_P	3H	VADJ	C9
K23	HA23_N	3H	VADJ	D9
K24	GND	-	-	-
K25	HB00_P_CC	2A	VIOB_M2C	AP18
K26	HB00_N_CC	2A	VIOB_M2C	AN18
K27	GND	-	-	-
K28	HB06_P_CC	2A	VIOB_M2C	AT18
K29	HB06_N_CC	2A	VIOB_M2C	AR18
K30	GND	-	-	-
K31	HB10_P	2A	VIOB_M2C	AN16
K32	HB10_N	2A	VIOB_M2C	AM16
K33	GND	-	-	-
K34	HB14_P	2A	VIOB_M2C	AU19
K35	HB14_N	2A	VIOB_M2C	AT19
K36	GND	-	-	-
K37	HB17_P_CC	2I	VIOB_M2C	AM21
K38	HB17_N_CC	2I	VIOB_M2C	AL20
K39	GND	-	-	-
K40	VIO_B_M2C	-	-	-

11 Board Specification

Table 12: Board Specification

FPGA	Altera Arria10 GX1150 / GX900 / GX660 / SX660 / SX570 / GX570
CPU (SX-Variant only)	Dual Core ARM Cortex A9 up to 1.5 GHz
AMC-Module	Standard Advanced Mezzanine Card, single width
Main Memory	Up to 16GB SDRAM
Removable Flash	Micro SD-Card Slot
Firmware	Linux BSP (on request)
Power Consumption	12V / 6.0A
Operating Temperature	0°C – +55°C with forced cooling
Storage Temperature	-40°C - +85°C
Humidity	10% – 90% rh non-condensing
Standards compliance	AMC.0 R2.0, AMC.1, AMC.2, AMC.3, AMC.4, IMPI V1.5, HPM.1 EN60950, UL1950, RoHS

12 Installation

12.1Safety Note

To ensure proper functioning of the **NAMC-ARRIA10-FMC** during its usual lifetime take the following precautions before handling the board.

CAUTION
Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their lifetime!

- Before installing or uninstalling the **NAMC-ARRIA10-FMC** read this installation section
- Before installing or uninstalling the **NAMC-ARRIA10-FMC**, read the Installation Guide and the User's Manual of the carrier board used, or of the µTCA system the board will be plugged into.
- Before installing or uninstalling the **NAMC-ARRIA10-FMC** on a carrier board or both in a rack:
  - Check all installed boards and modules for steps that you have to take before turning on or off the power.
  - Take those steps.
  - Finally turn on or off the power if necessary.
  - Make sure the part to be installed / removed is hot swap capable, if you don't switch off the power.
- Before touching integrated circuits ensure to take all require precautions for handling electrostatic devices.
- Ensure that the **NAMC-ARRIA10-FMC** is connected to the carrier board or to the µTCA backplane with the connector completely inserted.
- When operating the board in areas of strong electromagnetic radiation ensure that the module
  - is bolted the front panel or rack
  - and shielded by closed housing

12.2 Installation Prerequisites and Requirements

IMPORTANT
Before powering up check this section for installation prerequisites and requirements!

12.2.1 Requirements

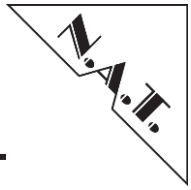
The installation requires only
- an ATCA carrier board, or a µTCA backplane for connecting the **NAMC-ARRIA10-FMC**
- power supply
- cooling devices

12.2.2 Power supply

The power supply for the **NAMC-ARRIA10-FMC** must meet the following specifications:
- required for the module:
  - +12V / 6A max.

12.2.3 Automatic Power Up

In the following situations the **NAMC-ARRIA10-FMC** will automatically be reset and proceed with a normal power up:
- The voltage sensor generates a reset
  - when +12V voltage level drops below 8V
  - when +3.3V voltage level drops below 3.08V
- The carrier board / backplane signals a PCIe Reset.



12.3Statement on Environmental Protection

12.3.1Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, polybrominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semiconductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

12.3.2Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste. If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on

"Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

12.3.3 Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

12.3.4 Product Safety

The board complies with EN60950 and UL1950.

12.3.5 Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

13 Known Bugs / Restrictions

Hardware Revision 1.0 / 1.1

- Maximum USB Speed is 12M

Hardware Revision 1.1:

- DIP SW3-2 has to be set to "OFF" when connecting external JTAG cable
- DIP SW3-2 has to be set to "ON" when using the embedded JTAG programmer

Appendix A: Reference Documentation

Appendix B: Document's History

Revision	Date	Description	Author
1.0	20.03.2018	Initial Release	MM / SE
1.1	11.04.2018	Fixed typos	MM
1.2	19.07.2018	Updated contents to PCB V1.4. Added notes that PL clocks connected to FPGA bank 2L will not work with PCB smaller V1.4. Updated clock tree. Updated known limitations section.	MM
1.3	15.08.2019	Added description for general purpose clock inputs/outputs from/to IDT clock multiplexer. Changed application PLL outputs to 125 MHz. Added limitation for industrial temperature range option.	MM
1.4	27.11.2019	Added description for BSP	MM