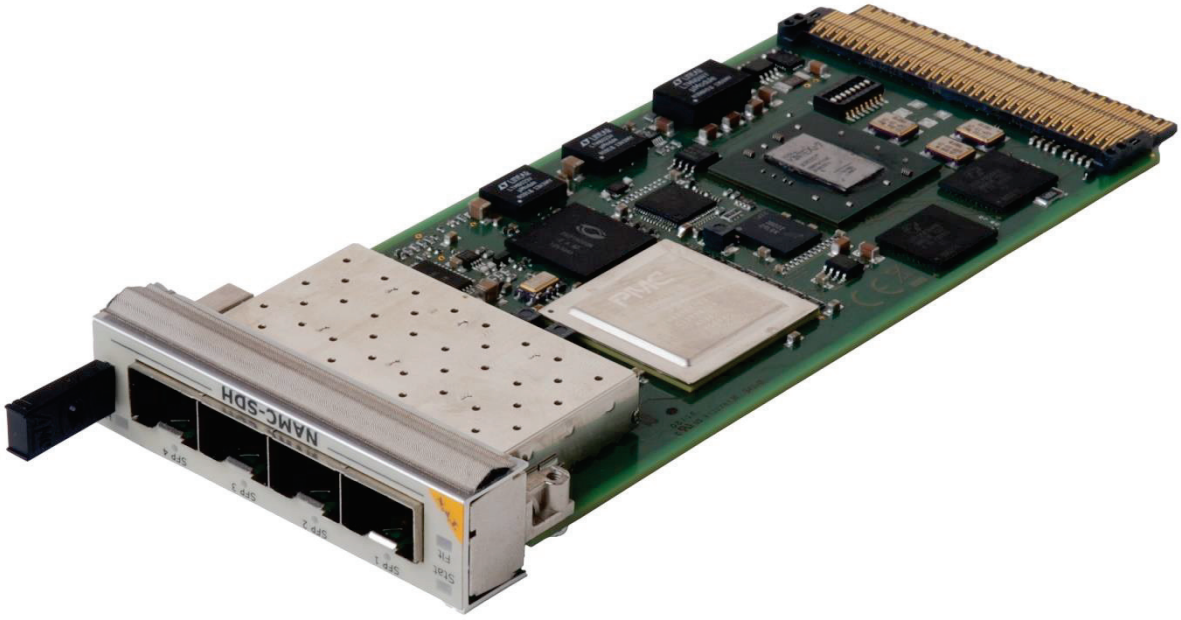
NAMC-SDH

TELECOM AMC MODULE

DESIGNED BY N.A.T. GMBH



TECHNICAL REFERENCE MANUAL V1.5

HW REVISION 1.X

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1. PREFACE

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1.2. About This Document

This document is intended to give an overview on the **NAMC-SDH's** functional capabilities.

Preface

General information about this document

Introduction

Abstract on the **NAMC-SDH's** main functionality and application field

Quick Start

Important information and mandatory requirements to be considered before operating the **NAMC-SDH** for the first time

Functional Description

Detailed information on the individual devices and the **NAMC-SDH's** main features

Hardware

Description of the connectors, switches, and LEDs located on the **NAMC-SDH**

Specifications and Compliances

Detailed list of specifications, abbreviations, and datasheets of components referred to in this document and standards, the **NAMC-SDH** complies to

Document's History

Revision record

Note:

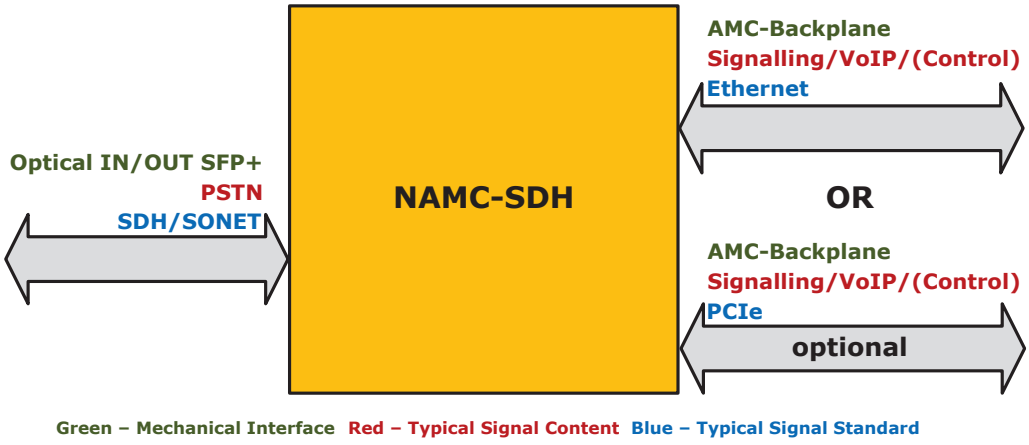
It is assumed, that the **NAMC-SDH** is handled by qualified personnel only!

2. INTRODUCTION

The **NAMC-SDH** is a telecommunication interface board for applications dealing with SDH/SONET (referred to as 'SDH' in the following). Due to its flexible line interface connectivity, it offers various data paths available over Ethernet from which the user can select the one best matching his application needs.

The following figure shows a high-level diagram of the **NAMC-SDH**. The applications shown here are just typical examples; the board's actual features are not limited to the described signals and standards.

Figure 1 – Typical Application



2.1. Basic Functionality

2.1.1. Multiplexing/De-Multiplexing

The **NAMC-SDH** offers multiplexing and de-multiplexing of the SDH-signal down to DS0-level (64 kbit/s – ISDN-channel).

2.1.2. Interworking

The **NAMC-SDH** features bi-directional data exchange between classic TDM traffic per SDH/SONET network and packet-orientated traffic per Ethernet. On Ethernet-side, the **NAMC-SDH** can transport traffic via RTP, iTDM, and custom Layer-2 Ethernet Packets.

2.1.3. HDLC-Controller

The HDLC-Controller implemented in the FPGA supports bi-directional exchange of HDLC-Traffic in any channel between SDH- and system-side.

2.2. Applications

An overview of the most common applications offered by the **NAMC-SDH** is given in the following paragraphs.

2.2.1. Gateway Applications

Combining its three basic functionalities, the **NAMC-SDH** offers the platform to build up the core of a media-gateway-system, such as conversion from legacy PSTN to VoIP and vice versa, and handling of time-critical PSTN-signalling.

2.2.2. Monitoring Applications

The **NAMC-SDH** features various options for monitoring traffic (listen-only), such as content-filtering, signalling-filtering, or any combination of both.

2.3. Main Features

Table 1 – Technical Data

Form Factor	
	• Single-width, full-size or mid-size AMC • Width: 73.5 mm, Depth: 180.6 mm
Processing Resources	
Add/Drop Multiplexer, E1/T1 and SDH Interface	• PMC TEMUX336 • 252 E1 or 336 T1 Framers • 4 OC-3/STM-1 or 2 OC-12/STM-4 Interfaces • Access possible down to single DS0 level

FPGA	• XILINX Kintex-7
	  • Default assembly: XC7K325T
	  • Other XC7K derivates on request
	• Available for custom use
	• Optionally featuring
	  • SDH-Interface
	  • Time-Slot-Interchanger (TSI)
	  • iTDM-Controller
	  • HDLC-Controller (optional)
	  • Control Interface
	  • Ethernet Interface(s)

Microcontroller	• Atmel ATmega128 as IPMI-Controller

Memory	• External memory for FPGA
	  • Either two 72Mbit QDR2+ SRAMs
	  • Or one 2GB DDR3 SRAM (default)

Operating System Support	• Host Driver for Ethernet Control Interface, supported O/S:
	  • LINUX
	  • OK-1

FPGA Programming Interface	
	• Xilinx FPGA JTAG on regular AMC JTAG Pins
Backplane Interconnect	
	• 4x Gigabit Ethernet • Optional fat pipe (XAUI or SRIO) at AMC ports 4-7 • ESSI for redundant/failover operation at AMC port 12 • iTDM via Gigabit Ethernet at AMC ports 0, 1, 4, 8 • PICMG SFP.1 Rev 1.0
Front Panel	

	• 4 SFP connectors to host
	  • Either 4x OC-3/STM-1 SFP transceivers
	  • Or 2x OC-12/STM-4 SFP transceivers
	• 4 bi-color link LEDs
	• Standard AMC LEDs

Compliance	
	• PICMG AMC.0 Rev. 2.0 • PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format) • PICMG SFP.1 Rev. 1.0 (Internal TDM) • PICMG HPM.0 (Hardware Platform Management) • IPMI Specification v2.0 Rev. 1.0 • PICMG µTCA.0 Rev. 1.0

Order Codes	
NAMC-SDH -[Option F]	• F: type of Kintex-FPGA
NAMC-SDH -[Option M]	• M: External Memory
NAMC-SDH -[Option S]	• S: Type of SFP transceiver (SDH level)
NAMC-SDH -[Option N]	• N: Number of transceivers
Environmental	
Operating Environment	• Default: 0°C to +50 °C (with forced cooling) • Humidity: 10% to 90% at +55°C (non-condensing) • Vibrations: sinusoidal , 0.38mm pk from 5Hz to 36Hz, 2g from 36Hz to 2KHz • Shocks: 20g, 11ms, 1⁄2 sine • Altitude: 0 to 5000m
Storage Environment	• Default: -40°C to +85°C • Humidity: 5% to 95% (non-condensing) • Vibrations: sinusoidal , 0.38mm pk from 5Hz to 36Hz, 3g from 36Hz to 2KHz • Shocks: 30g, 11ms, 1⁄2 sine • Altitude: 0 to 15000m

3. QUICK START

To ensure proper functioning of the **NAMC-SDH** during its usual lifetime, take the following precautions before handling the board.

3.1. Unpacking

Electrostatic discharge, incorrect board installation, and uninstallation can damage circuits or shorten their lifetime. Before touching integrated circuits, ensure to take all required precautions for handling electrostatic devices.

Avoid touching gold contacts of the AMC-Edge-Connector to ensure proper contact when inserting the **NAMC-SDH** onto the backplane.

Make sure that the board and its attachments are undamaged and complete according to delivery note.

3.2. Mechanical Requirements

The **NAMC-SDH** is designed to meet the requirements of µTCA systems, but can be plugged onto any ATCA carrier board supporting AMC standards as well. So the installation requires an ATCA-Carrier-Board or an µTCA-Backplane for connecting the **NAMC-SDH**, a power supply, and cooling devices.

Before installing or uninstalling the **NAMC-SDH**, read the Installation Guide and the User's Manual of the carrier board used, or of the µTCA system the board will be plugged into.

Check all installed boards and modules for steps that you have to take before turning on or off the power. After taking those steps, turn on or off the power if necessary.

Make sure the part to be installed / removed is hot-swap-capable, if you do not switch off the power.

Ensure that the **NAMC-SDH** is connected to the carrier board or to the µTCA backplane with the connector completely inserted.

When operating the board in areas of strong electromagnetic radiation, ensure that the module is bolted to the front panel or rack, and shielded by closed housing.

3.3. Voltage Requirements

3.3.1. Power supply

The power supply for the **NAMC-SDH** must meet the following specifications:

+12V / 2A max.

+ 3,3V / 0.15A max.

3.3.2. Hot-Swap

The **NAMC-SDH** supports hot-swapping, which means that the board can be inserted or extracted during normal system operation without affecting other modules.

Make sure to follow the procedure ***exactly*** to prevent the **NAMC-SDH** or the system it is plugged into from damage!

Insertion of a hot-swap-capable Module

- Ensure the module and the backplane/carrier support hot-swapping
- Ensure that the hot-swap-handle is in "unlock"-position (pulled out)
- Push the **NAMC-SDH** carefully into the dedicated connector until it is completely inserted
- The blue HS-LED turns solid on
- With pushing the hot-swap-handle to "lock"-position, the HS-LED starts blinking and the IPMI-Controller of the backplane/carrier detects the board
- If the information provided by the **NAMC-SDH** is valid, the backplane/carrier enables payload power and the blue HS-LED turns off

Extraction of a hot-swap-capable Module

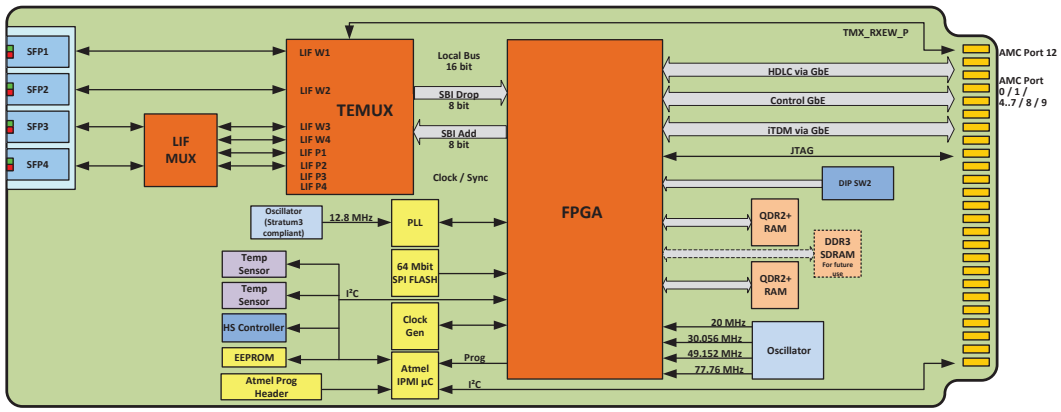
- Pull the hot-swap-handle in "unlock"-position
- The blue HS-LED starts blinking
- The IPMI-Controller of the backplane/carrier disables payload power
- The HS-LED turns solid on
- Pull the **NAMC-SDH** carefully out of the backplane/carrier

4. FUNCTIONAL DESCRIPTION

The **NAMC-SDH** can be divided into a number of functional blocks, which are described in the following paragraphs.

The following figure gives an overview on the functional blocks.

Figure 2 – Block Diagram

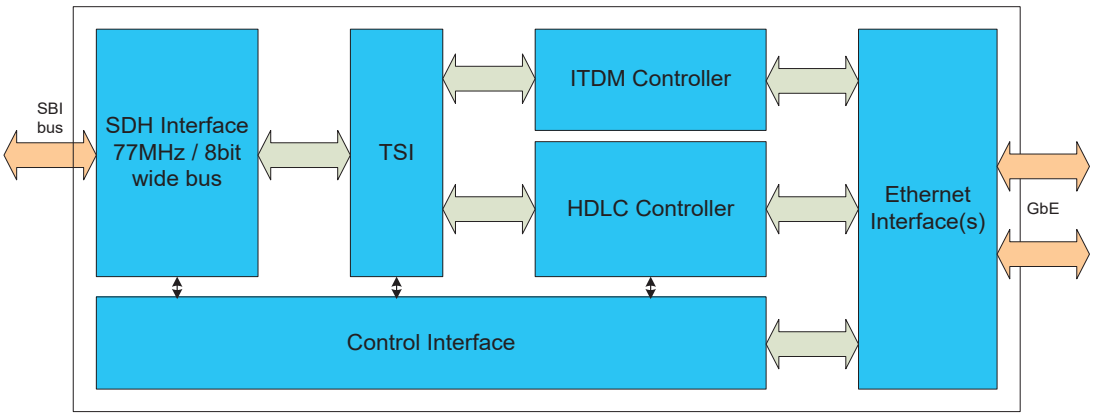


4.1. FPGA

The central component on the **NAMC-SDH** is a Xilinx Kintex-7 FPGA device, which offers a wide range of logic resources by migrating between various pin compatible devices available for one footprint. Target device for the standard assembly variant is the XC7K325T, featuring 325000 logic cells and around 16 Mbit internal SRAM. Please refer to Chapter 6.1 for reference documentation.

The following figure gives an overview of the main blocks implemented in the FPGA; details are described in the subchapters.

Figure 3 – FPGA Design Overview



4.1.1. SDH Interface

The FPGA connects towards the SDH chipset (TEMUX336) via an SBI bus. This bus consists of an 8-bit wide bus for Tx (add direction), and a separated 8-bit wide bus for Rx (drop direction). The data is transmitted byte-wise, organized in a fixed TDM structure. Thus every time-slot is found at a fixed location within a structure repeating every 125 µs. Clock frequency on the SBI bus is 77.76 MHz, so that the structure of one 125 µs frame consists of 9720 time-slots. Within these time-slots, depending on the used multiplexing scheme, around 8000 time-slots carry payload data.

The FPGA logic contains reduction logic to make the used payload time-slots accessible in the number space from 0 – 8191.

4.1.2. Time-Slot-Interchanger (TSI)

The TSI Block is used to either cross-connect a time-slot directly from Rx to Tx, to connect a time-slot to the ITDM controller, or to connect one or multiple of them to a channel of the HDLC controller. The delay introduced by the TSI cross-connect switch is two frames (each 125 µs), so that the total cross-connect delay can be equal or below 1 ms.

There is an override function implemented that is used to set all SDH time-slots to cross-connect for the case that the connection to the controlling host is lost. This is realized using a 16 bit-wide counter that permanently counts down in intervals of 1 ms (so offering a maximum time range of around one minute). Upon reaching zero it initiates a reset of the TSI routing memory to force complete cross-connect. In order to prevent it from doing so, the controlling host regularly has to set the counter to a value representing the desired time-out.

In addition to routing memory reset, the counter time-out will stop and reset the ITDM and HDLC controllers, to avoid a large amount of Ethernet frames being sent to a no longer present host (what might result in flooding the packets in the switches).

4.1.3. ITDM Controller

The ITDM Controller encapsulates TDM data into Ethernet frames. By this means, the **NAMC-SDH** is able to transmit and receive TDM data streams using the packet switching based infrastructure an ATCA or µTCA system offers. The function volume includes the standard ITDM implementation used on various ITDM-capable N.A.T. boards:

- Support of ITDM control message protocol
- Support of ITDM 125 µs-mode
- Support of ITDM 1 ms-mode
- Transmission of up to 8192 time-slots (each 64 kbit/s)
- Reception of up to 8192 time-slots (each 64 kbit/s)

4.1.4. HDLC Controller (optional)

The HDLC Controller offers a total capacity of 8192 * 64 kbit/s (8192 * DS0 bandwidth) per direction. It can be configured to handle up to 8192 separate 64 kbit/s channels, or to combine each up to 32 of the 64 kbit/s time-slots to super-channels.

In Rx direction, it performs detection and handling of the HDLC idle pattern, bit-unstuffing, checking CRC, and packing the received HDLC frames into Ethernet frames.

In Tx direction, it performs generation of the HDLC idle pattern, CRC generation, bit-stuffing, and putting data out of Ethernet frames into HDLC frames.

The HDLC-Feature is available as ordering option.

4.1.5. Control Interface

Besides the payload data, all configuration and management data going to and coming from the **NAMC-SDH** board is transmitted via Ethernet. Therefore, a control interface within the FPGA is able to handle Ethernet frames carrying a special protocol based upon regular Layer2 Ethernet. This handles memory-mapped accesses on the board's internal memory map, covering both FPGA internal blocks as well as external devices like the TEMUX336.

Furthermore, this control interface is able to initiate exchange of these management Ethernet frames to realize transmission of interrupt events towards the host.

4.1.6. Ethernet Interface(s)

There are four serial Gigabit Ethernet interfaces connecting to AMC ports 0, 1, 4, and 8. This allows the board to operate in redundant setups as well as to select whether data transfer resides in the AMC Common-Option region (port 0/1) or in the Fat-Pipe region (port 4/8).

When operating in the Fat-Pipe region, the **NAMC-SDH** will typically connect to a 10G Ethernet switch configured to Gigabit transmission mode for the respective port.

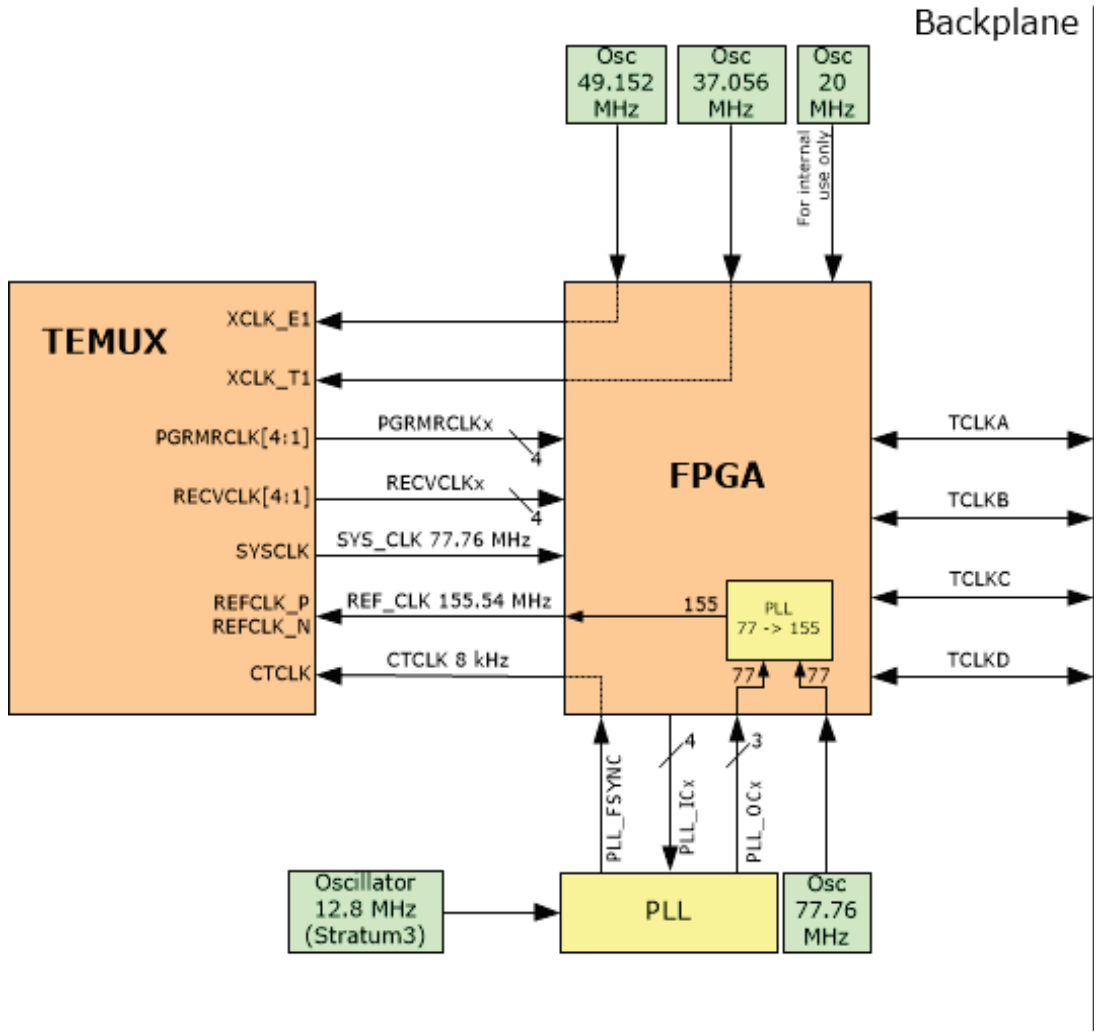
Towards the further FPGA internal components, Ethernet packets are delivered to the control interface if they carry control or management commands, to the HDLC engine if they carry frame data to be HDLC coded, or to the ITDM controller if they are ITDM control or data packets.

In outgoing direction, the packets coming from the control interface, coming from the HDLC engine, and coming from the ITDM controller are arbitrated and sent out depending on configuration using AMC port 0, 1, 4, or 8.

4.1.7. Clock Connectivity

There are various clock connections between the FPGA and the SDH chipset. An overview is given in the following figure.

Figure 4 – Clock Connectivity – Overview



For more detailed information about the signals and sources, please refer to the following table.

Table 2 – Clock Connectivity – Details

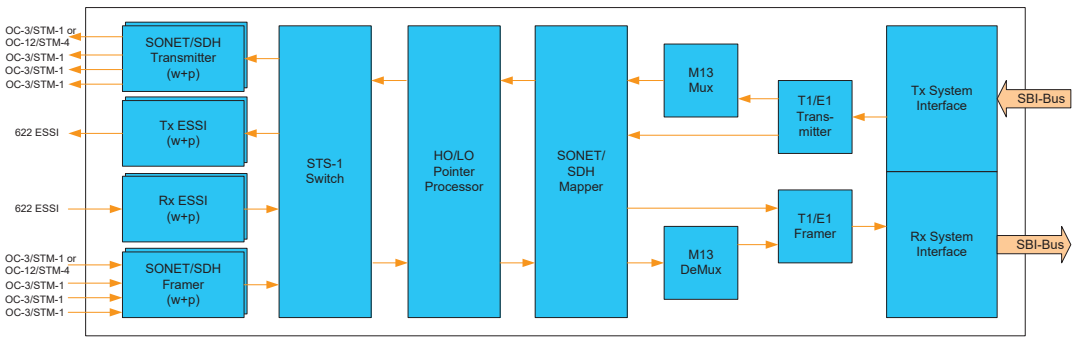
Clock Output	Clock Input	Sourced by
XCLK_E1	-	Oscillator 49.152 MHz
XCLK_T1	-	Oscillator 37.056 MHz
-	PGRMRCKLx	TEMUX PGRMRCLK[4:1]
-	RECVCLKx	TEMUX RECVCLK[4:1]
-	SYS_CLK 77.76 MHz	TEMUX SYSCLK
REF_CLK 155.54 MHz	-	PLL_OC2 (derived from Oscillator 12.8 MHz) Oscillator 77.76 MHZ => internal MUX, default PLL_OC2
CTCLK 8 kHz	-	PLL_FSYNC (Oscillator 12.8 MHz)
PLL_IC1	-	TCKLA
PLL_IC2	-	Please refer to the **NAMC-SDH** Programming Manual
PLL_IC3	-	TEMUX PGRMRCLK[1]
PLL_IC4	-	TEMUX RECVCLK[1]
TCLKA	-	Please refer to the **NAMC-SDH** Programming Manual
TCLKB	-	
TCLKC	-	
TCLKD	-	

Note: This table shows the information from FPGA point of view.

4.2. SDH Chipset and Line Interfaces

The **NAMC-SDH** is equipped with a TEMUX336 device from PMC Sierra. The following figure gives an overview of the main blocks implemented in the TEMUX336. Please refer to Chapter 6.1 for reference documentation.

Figure 5 – TEMUX Details



The device is capable of de-multiplexing and multiplexing a complete STM4 link down to single 64 kbit/s time-slots. By using different SFP modules, a wide range of physical interface standards can be covered.

Four of the Temux336 serial line interface channels are connected to SFP transceiver modules. This offers the following options for operation:

- 4x STM1 termination
- 1x STM4 termination

To support a wide range of clocking options, the **NAMC-SDH** features a Stratum3 compliant PLL with an appropriate oscillator.

4.3. FPGA External Memory

The **NAMC-SDH** offers the possibility of assembling different kinds of external memories connected to the FPGA.

4.3.1. Dual External SRAM (QDR2+)

Two 72Mbit QDR2+ SRAM devices connected to the FPGA are used to realize separate data buffers for each the Rx and the Tx direction. These devices are directly supported by the FPGA type using IP blocks available from Xilinx. Each device is capable of simultaneously doing read and write transfers, so that Rx and Tx direction will not interfere with each other.

Assembly of these devices is optional.

4.3.2. DDR3 SDRAM

One 2GB MT41J256M8 DDR3 SRAM device (or compatible) is connected to the FPGA. In the FPGA standard configuration, it is not used yet, but available for future extensions.

This device is equipped as standard.

4.4. AMC Clock Interface

The **NAMC-SDH** implements a very flexible clocking functionality concerning the AMC backplane clock ports TCLKA-D.

All clock lines can be used individually either as input or driven as output. Various output signals can be selected for the clock lines, and in input direction the clock lines can be used to supply the on-board PLL with a reference signal. Please refer to Chapter 6.1 for reference documentation.

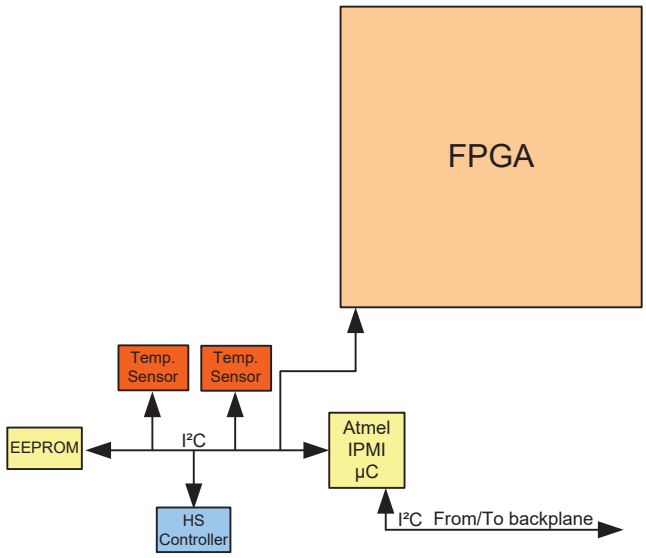
All TCLKA-D clock lines follow the MLVDS signalling standard.

4.5. IPMB-Interface and I²C-Devices

The **NAMC-SDH** implements an IPMB interface consisting of an IPMI-µC (ATMega128) and a couple of I²C devices connected via two I²C-Busses. Please refer to Chapter 6.1 for reference documentation.

The following figure shows the architecture in detail.

Figure 6 – IPMB-Interface



One bus is the IPMB bus towards the backplane; the other bus interfaces various local devices.

Table 3 – Local I²C-Devices

Device	Function	I²C-Address
FPGA		0xCC
EEPROM	Storage of board-specific information	0xA0
Temperature Sensors	2x measuring FPGA temperature 1x measuring chip-internal temperature	0x56
Hot-Swap Controller	Manages Hot-Swap functionality	0x96

The IPMI controller also manages the geographical address as requested by the AMC specification.

5. HARDWARE

5.1. Front Panel and LEDs

The **NAMC-SDH** module is equipped with four bi-coloured LEDs reflecting the SFP interface status. They are mounted above the SDH connectors.

Additionally, it features the standard AMC LEDs, with the red and blue LED being controlled by the IPMB-µC, and the green and orange ones being controlled via FPGA registers.

Figure 7 – Front Panel Mid-Size

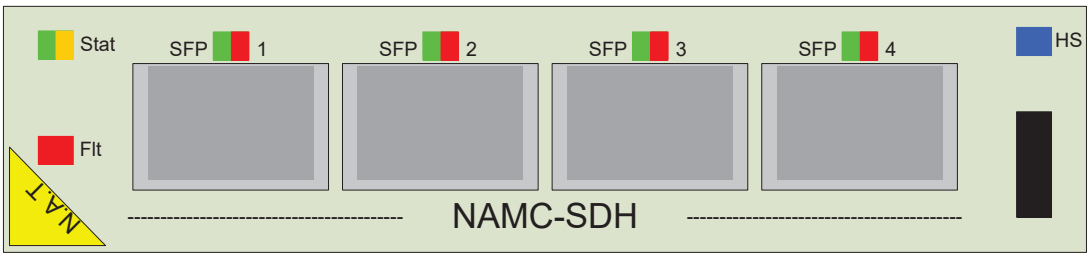


Table 4 – LED Functionality

LED	Function	Control
SFP1..4	Reflecting SFP interface status, tbd	FPGA
blue	AMC Hot Swap LED	IPMI-µC
red	Fault Indication LED	IPMI-µC
green	Solid: Ethernet link	FPGA
green	Blink: PLL Lock	FPGA
yellow	Blink: Ethernet Management Traffic	FPGA

The Fault Indication LED turns to “On” if the temperature sensor registers a temperature value falling below or exceeding a threshold level. If the temperature returns to normal value, the LED is switched to “Off” again.

Although optically appearing as one LED, the General Purpose LED physically consists of two LEDs (green and orange) sharing the same hole in the front plate. For more information on the behaviour of these LEDs, please refer to the **NAMC-SDH** Programming Manual.

5.2. AMC Port Definition

Table 5 – AMC Port Definition

Connector Region		AMC Port #	Signal		Non-Redundant MCH / Fabric #	Redundant MCH / Fabric #
Basic Side	Clocks	CLK1/TCLKA	Reference Clock 1			
		CLK2/TCLKB	Reference Clock 2			
		CLK3/FCLKA	Fabric Clock			
	Common Options	0	1000BaseX Ethernet Channel 0		A	1 / A
		1	1000BaseX Ethernet Channel 1			2 / A
		2	unassigned		(B)	(1 / B)
		3	unassigned		(C)	(2 / B)
	Fat Pipe	4	1000BaseX Ethernet Channel 2	XAUI-Interface Lane 0-3	D	1 / D
		5	na		E	1 / E
		6	na		F	1 / F
		7	na		G	1 / G
Extended Side	Extended Fat Pipe	8	1000BaseX Ethernet Channel 3			2 / D
		9	unassigned			2 / E
		10	unassigned			2 / F
		11	unassigned			2 / G
	Extended Options	12	TEMUX ESSI working			
		13	unassigned			
		14	unassigned			
		15	unassigned			
		16	Reference Clock 3/4			
		17	unassigned			
		18	unassigned			
		19	unassigned			
		20	unassigned			

Note: The mapping of the MCH's fabrics can vary depending on which backplane the **NAMC-SDH** is operated. This table shows the standard assignment.

5.3. Component-, Connector-, and Switch-Location

Figure 8 – Location Diagram – Top

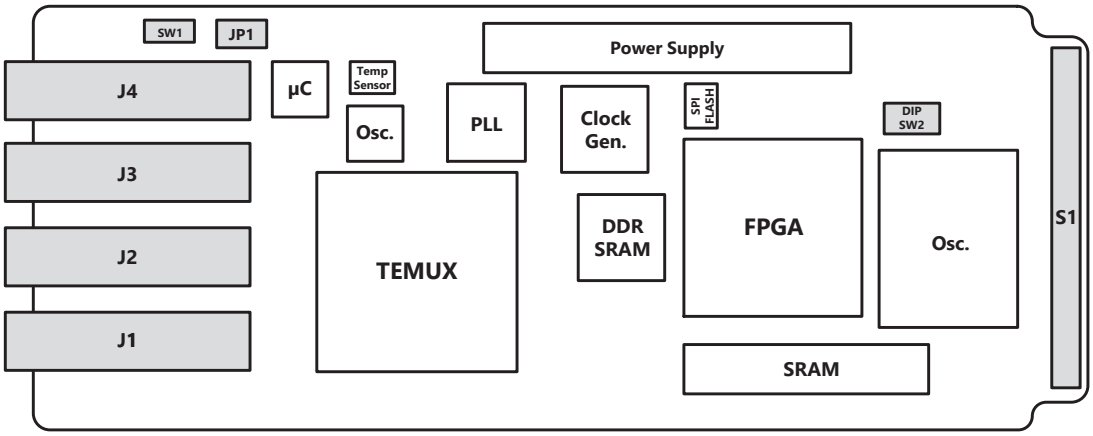
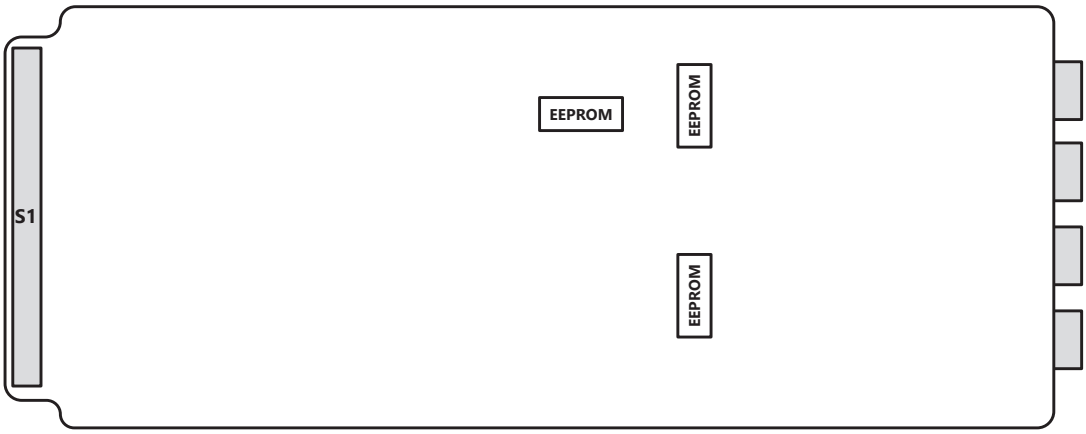


Figure 9 – Location Diagram – Bottom



Connectors on top side: drawings imply the board is orientated with the AMC Edge Connector to the right side

Connectors on bottom side: drawings imply the board is orientated with the AMC Edge Connector to the left side

Please refer to the following tables to look up the connector pin assignment of the **NAMC-SDH**.

5.3.1. S1: AMC Connector

Figure 10 – S1: AMC-Connector (top view)

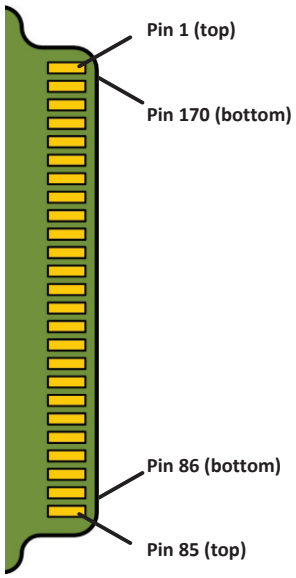


Table 6 – S1: AMC-Connector – Pin-Assignment

Pin #	Signal	Signal	Pin #
1	GND	GND	170
2	PWR	TDI	169
3	/PS1	TDO	168
4	PWR_IPMB	/TRST	167
5	GA0	TMS	166
6	RESVD	TCK	165
7	GND	GND	164
8	RESVD	/SPISEL	163
9	PWR	SPICLK	162
10	GND	GND	161
11	XLINK1_P	SPIMOSI	160
12	XLINK1_N	SPIMISO	159
13	GND	GND	158
14	RLINK1_P	PORT19TX_P	157
15	RLINK1_N	PORT19TX_N	156
16	GND	GND	155
17	GA1	PORT19RX_P	154
18	PWR	PORT19RX_N	153
19	GND	GND	152
20	XLINK2_P	PORT18TX_P	151
21	XLINK2_N	PORT18TX_N	150
22	GND	GND	149
23	RLINK2_P	PORT18RX_P	148

Pin #	Signal	Signal	Pin #
24	RLINK2_N	PORT18RX_N	147
25	GND	GND	146
26	GA2	NC	145
27	PWR	NC	144
28	GND	GND	143
29	NC	NC	142
30	NC	NC	141
31	GND	GND	140
32	NC	NC	139
33	NC	NC	138
34	GND	GND	137
35	NC	NC	136
36	NC	NC	135
37	GND	GND	134
38	NC	NC	133
39	NC	NC	132
40	GND	GND	131
41	/ENABLE	NC	130
42	PWR	NC	129
43	GND	GND	128
44	PET0_P_P4	RESVD	127
45	PET0_N_P4	TDM_REF	126
46	GND	GND	125
47	PER0_P_P4	TDM_FS	124
48	PER0_N_P4	TDM_CLK	123
49	GND	GND	122
50	NC	TDM7	121
51	NC	TDM6	120
52	GND	GND	119
53	PER1_P	TDM5	118
54	PER1_N	TDM4	117
55	GND	GND	116
56	IPMB_SCL	TDM3	115
57	PWR	TDM2	114
58	GND	GND	113
59	NC	TDM1	112
60	NC	TDM0	111
61	GND	GND	110
62	NC	NC	109
63	NC	NC	108
64	GND	GND	107
65	NC	NC	106
66	NC	NC	105
67	GND	GND	104
68	NC	NC	103
69	NC	NC	102
70	GND	GND	101
71	IPMB_SDA	NC	100
72	PWR	NC	99

Pin #	Signal	Signal	Pin #
73	GND	GND	98
74	CLK_1_P	NC	97
75	CLK_1_N	NC	96
76	GND	GND	95
77	CLK_2_P	NC	94
78	CLK_2_N	NC	93
79	GND	GND	92
80	CLK_3_P	PET0_P_P8	91
81	CLK_3_N	PET0_N_P8	90
82	GND	GND	89
83	/PS0	PER0_P_P8	88
84	PWR	PER0_N_P8	87
85	GND	GND	86

5.3.2. JP1: Atmel Programming Header

Connector JP1 connects to the programming-port of the Atmel µC device.

Figure 11 – JP1: Atmel Programming Header

Table 7 – JP1: Atmel Programming Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	PDI_DATA	+3.3V	2
3	nc	/PROG_ENABLE*	4
5	PDI_CLK	GND	6

Note: *For programming the **NAMC-SDH** out of system, connect Pin 4 and Pin 6 to force Pin 4 to Low-Status.

5.3.3. J1-J4: Front Panel SFP Connectors

The optical front panel connectors J1-J4 have standard LC-plugs and can be equipped with either singlemode or multimode transceivers.

Figure 12 – J1-J4: Front Panel SFP Connector

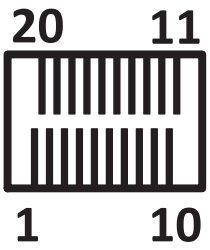


Table 8 – J1: Front Panel SFP Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	nc	2
3	GND	SDA_SFP1	4
5	SCL_SFP1	+3.3V_SFP1	6
7	+3.3V_SFP1	TMX_LOSW1	8
9	GND	GND	10
11	GND	TMX_RXW1_N	12
13	TMX_RXW1_P	GND	14
15	+3.3V_SFP1	+3.3V_SFP1	16
17	GND	TMX_TXW1_P	18
19	TMX_TXW1_N	GND	20

Table 9 – J2: Front Panel SFP Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	nc	2
3	GND	SDA_SFP2	4
5	SCL_SFP2	+3.3V_SFP2	6
7	+3.3V_SFP2	TMX_LOSW2	8
9	GND	GND	10
11	GND	TMX_RXW2_N	12
13	TMX_RXW2_P	GND	14
15	+3.3V_SFP2	+3.3V_SFP2	16
17	GND	TMX_TXW2_P	18
19	TMX_TXW2_N	GND	20

Table 10 – J3: Front Panel SFP Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	nc	2
3	GND	SDA_SFP3	4
5	SCL_SFP3	+3.3V_SFP3	6
7	+3.3V_SFP3	TMX_LOSW3	8
9	GND	GND	10
11	GND	TMX_RXW3_N	12
13	TMX_RXW3_P	GND	14
15	+3.3V_SFP3	+3.3V_SFP3	16
17	GND	TMX_TXW3_P	18
19	TMX_TXW3_N	GND	20

Table 11 – J4: Front Panel SFP Connector – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	nc	2
3	GND	SDA_SFP4	4
5	SCL_SFP4	+3.3V_SFP4	6
7	+3.3V_SFP4	TMX_LOSW4	8
9	GND	GND	10
11	GND	TMX_RXW4_N	12
13	TMX_RXW4_P	GND	14
15	+3.3V_SFP4	+3.3V_SFP4	16
17	GND	TMX_TXW4_P	18
19	TMX_TXW4_N	GND	20

5.4. DIP Switches

5.4.1. DIP SW2: Ethernet Options Select

The tables below provide information on the operating parameters and configuration options of DIP SW2.

Figure 13 – DIP SW2: Ethernet Options Select

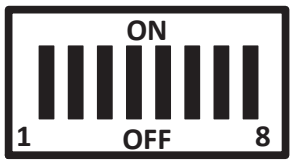


Table 12 – DIP SW2 – Operating Parameters

Switch #	Function
SW2-1	LIF Operation Mode Select
SW2-2	Backplane Ethernet Port Mapping Select
SW2-3	Fat Pipe Mapping Select
SW2-4	MAC-Address Value Bit 0 **only valid if DIP SW2-8 is turned to 'ON'**
SW2-5	MAC-Address Value Bit 1 **only valid if DIP SW2-8 is turned to 'ON'**
SW2-6	Ethernet Fallback Switching
SW2-7	Ethernet Auto-Negotiation Disable **for operation with XAUI switch, turn to 'ON'**
SW2-8	MAC-Address Configuration **MAC-Address value is determined by SW2-4 and SW2-5**

Table 13 – DIP SW2 – Configuration

Switch #	ON	OFF
SW2-1	LIF Operation Mode: 2x working / 2x protect	***LIF Operation Mode: 4x working***
SW2-2	Ethernet via Port 1/8 (Redundant)	***Ethernet via Port 0/4 (Primary)***
SW2-3	Ethernet via Port 4/8 (Fat-Pipe)	***Ethernet via Port 0/1 (Common Options)***
SW2-4	MAC-Address Value of Bit 0 is set to '1'	***MAC-Address Value of Bit 0 is set to '0'***
SW2-5	MAC-Address Value of Bit 1 is set to '1'	***MAC-Address Value of Bit 1 is set to '0'***
SW2-6	Ethernet Fallback Switching enabled	***Ethernet Fallback Switching disabled***
SW2-7	Ethernet Auto-Negotiation is disabled	***Ethernet Auto-Negotiation is enabled***
SW2-8	MAC-Address Configuration is enabled	***MAC-Address Configuration is disabled***

Note:

Default configuration is labelled with ***bold, italic letters***.

5.4.2. SW1: Hot Swap Switch

Switch SW1 is used to support Hot-Swapping of the module. It conforms to PICMG AMC.0.

6. SPECIFICATIONS AND COMPLIANCES

6.1. Internal Reference Documentation

- **NAMC-SDH** Programming Manual, please contact N.A.T.
- Ethernet Control Interface Technical Reference Manual, V1.2, 12/2003
- iTDM-FPGA Technical Reference Manual, V1.4, 07/2013

6.2. External Reference Documentation

- Xilinx Kintex-7 FPGA DS180, V2.6, 02/2018
- PMC Sierra TEMUX336 Product Brief, Issue 2
- Atmel ATmega128 µC Product Datasheet, Rev 2467X, 06/2011
- Zarlink DS31400 PLL Data Sheet, 04/2012

6.3. Standards Compliance

- PICMG AMC.0 Rev. 2.0
- PICMG SFP.0 Rev. 1.0 (System Fabric Plane Format)
- PICMG SFP.1 Rev. 1.0 (Internal TDM)
- IPMI Specification v2.0 Rev. 1.0
- PICMG µTCA.0 Rev. 1.0

6.4. Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, poly-brominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semi-conductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon

as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

6.5. Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relationships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

6.6. Compliance to CE Directive

Compliance to the CE directive is declared. A ‘CE’ sign can be found on the PCB.

6.7. Product Safety

The board complies with EN60950 and UL1950.

6.8. Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

6.9. Abbreviation List

Table 14 – Abbreviation List

Abbreviation	Description
AMC	Advanced Mezzanine Card
ATCA	Advanced Telecommunications Computing Architecture
CRC	Cyclic Redundancy Check
DDR3 SDRAM	Double Data Rate Synchronous Dynamic RAM
DIP SW	Dual In-Line Switch
E1	2.048 Mbit G.703 Interface
ECI	Ethernet Control Interface
EEPROM	Electrically Erasable PROM
ESSI	Extended Serial SONET/SDH Interface
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
H.110	Timeslot Interchange Bus
HDLC	High-Level Data Link Control
HS	Hot Swap
I^2C	Inter-Integrated Circuit
I/O	Input/Output
IP	Internet Protocol
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
IRQ	Interrupt Request
iTDM	Internal TDM
JTAG	Joint Test Action Group
LIF	Line Interface
µC	Microcontroller
µTCA	Micro Telecommunications Computing Architecture
MAC	Media Access Control
MUX	Multiplexer
OC	Optical Carrier
PCB	Printed Circuit Board
PCI(e)	Peripheral Component Interconnect (Express)
QDR 2+ SRAM	Quad Data Rate Static RAM
Rx	Receiver
R/W	Read/Write
RAM	Random Access Memory
(P)ROM	(Programmable) Read Only Memory

Abbreviation	Description
PLL	Phase Locked Loop
SBI	Scalable Bandwidth Interface
SDH	Synchronous Digital Hierarchy
SFP	Small Form-Factor Pluggable
SONET	Synchronous Optical Networking
STM	Synchronous Transfer Mode
T1	1,544 Mbit G.703 Interface (USA)
TCKL	Telecom Clock
TDM	Time Division Multiplex
TSI	Time Slot Interchanger
Tx	Transmitter
XAUI	10 GbE (via 4x 3.125 GB/s)

7. DOCUMENT'S HISTORY

Table 15 – Document's History

Rev	Date	Description	Author
1.0	24.06.2014	initial release	se
1.1	11.08.2014	Updated Chapter 5.1.12 - Register 0x0000100 – RESET	se
	3.09.2014	Added Chapter 5.1.18 - 0x0000110 – PLL_IC2_SEL	se
	10.09.2014	Added chapter 3.1.7 – Clock Connectivity	se
	25.11.2014	Corrected form factor to mid-size Added photo (Figure 1)	Te se
1.2	21.07.2016	Added table to explain E1 klm numbering	te
1.3	17.02.2017	Corrected klm E1 mapping in table 23 to match software implementation	te
1.4	22.9.2017	Corrected faceplate led numbering	te
	12.07.2018	Updated Chapter 4.1 AMC Port Definition	se
1.5	24.10.2018	Design change Reworked content and organisation of all chapters	se
	09.10.2019	Minor changes in layout Updated Table 12/13	se