



# NAMC-xE1/T1 and NAMC-xE3/T3



## Overview

The **NAMC-xE1/T1** is an Advanced Mezzanine Card (AMC) providing access to up to 16-E1/T1 interfaces in next generation systems based on MTCA and ATCA standards. The TDM-to-I-TDM converter connects the on-board E1/T1 interfaces with a Gigabit Ethernet port for system interconnect (I-TDM). The **NAMC-xE1/T1** is dedicated for (tele-)communication applications with extensive need for a high aggregation of multiple E1/T1 interfaces combined with access to switched networks based on high bandwidth Ethernet. The **NAMC-xE1/T1** is used for distributing signaling and payload data to DSP or CPU based processor resources within a MTCA or ATCA system.

## Key features

- Interfaces at the front panel:
  - 8x E1/T1 (NAMC-8E1/T1) or
  - 16x E1/T1 (NAMC-16E1/T1) or
  - 4x E3/T3 (NAMC-4E3/T3)
- Backplane
  - 2xGbE (port 0 and 1)
- FPGA resource with up to 64-Mbit of Quad Data Rate™ 2 (QDR2) SRAM

- extensive software support in combination with other N.A.T. AMC boards for any voice/data application in ISDN, SS7, ATM, VoIP or 3G environments.

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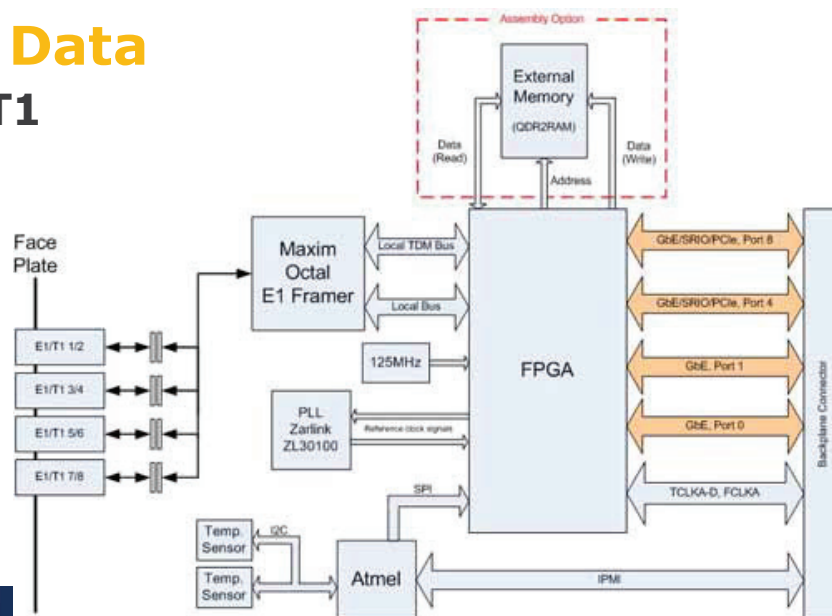
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# Technical Data

## NAMC-xE1/T1



## Overview

The **NAMC-xE1/T1** is available as a single width compact-, mid- or full-size AMC providing access to multiple E1/T1 or E3/T3 interfaces (NAMC-xE3/T3). The full-size version can be equipped with a mezzanine board offering additional 8E1/T1 line interfaces (NAMC-16E1/T1) or 4E3/T3 line interfaces (NAMC-4E3/T3).

The **NAMC-xE1/T1** and NAMC-xE3/T3 are dedicated for (tele-)communication applications with extensive need for a high aggregation of multiple E1/T1 or E3/T3 interfaces combined with access to switched networks based on high bandwidth Ethernet.

### FPGA and Memory

The **NAMC-xE1/T1** is equipped with an ECP3 FPGA from Lattice which offers 70.000 logic elements and 4 Mbit internal memory. In addition two external QDR2 SRAM devices can be assembled, each offering 32 Mbit.

### E1/T1 Access

The onboard DS26518 framer from Maxim/Dallas provides access to 8/16-E1/T1 lines at the front panel by four/eight RJ45 connectors. Besides the standard framing formats the **NAMC-xE1/T1** supports framing standards as:

- T1 Super Frame (SF)
- T1 Extended Super Frame (ESF),
- T1 Digital Multiplexer (DM)
- T1 Switch Line Carrier -96 (SLC-96)
- E1 G.704 and G.706 (CRC-4 multiframe)

The extremely sensitive input amplifier circuits support signal attenuation of up to -44dB making the board an optimal choice for all kind of monitoring applications.

### TDM and I-TDM Interface

The E1/T1 framer interfaces to the on-board timeslot interchanger (TSI) chipset. The TSI as well as the TDM-to-I-TDM bridge are incorporated in an ECP3 FPGA from Lattice. The TSI allows flexible routing as well as multicasting of 64kbps timeslots between the various E1/T1 streams. The TDM-to-I-TDM bridge converts the TDM oriented bit stream into Ethernet packets and vice versa. In addition to the I-TDM interface, the TSI offers an optional 32MHz clocked H.110-alike TDM backplane interface at the AMC connector (extended area).

### Fabric Support

#### Fat Pipe

The **NAMC-xE1/T1** offers two bidirectional serial lanes which can be operated either as GbE,

PCIe or SRIO. The interfaces at **NAMC-xE1/T1** can be configured to implement either GbE: two x1 (port 4 and 8) or optionally PCIe: one x1 (port 4 or 8) or on request SRIO: two x1 (port 4 and 8)

### Base Fabric

The **NAMC-xE1/T1** provides two 1000BaseX interfaces at port 0 and port 1 of the common options region of the AMC backplane connector.

### Extender Mezzanines

For applications requiring more TDM interfaces, N.A.T. offers an extender mezzanine supplying 8 additional E1/T1 lines at the front panel: the NAMC-16E1/T1.

The NAMC-4E3/T3 offers a mounted mezzanine providing four E3/T3 lines which are accessible via four RJ45 interfaces at the front panel. T3 handles a bandwidth of 44.736 Mbit/s or 672 channels and E3 supports data transmissions of 34.368 Mbit/s or 512, a higher data speed compared with E1 (2.048 Mbit/s - 32 channels) or T1 (1.544 Mbit/s - 24 channels).

## Key Features

### FPGA and Memory

- ECP3 FPGA from Lattice with 70.000 logic elements and 4 Mbit internal memory
- QDR2 SRAM with up to 64-Mbit

### Front Panel Interface

- 8-/16-E1/T1 available via 4/8 RJ45
- 4-E3/T3 available via four RJ45

### Backplane Connectivity

- clock distribution via full bi-directional clock support using TCLK-A, -B, -C, -D at AMC connector

### Base Fabric

- 2xGbE at AMC port 0 and port 1

### Fat Pipe Interface Options

- GbE x1 on ports 4 and 8 or optionally
- PCIe x1 on port 4 or 8 or on request
- SRIO x1 on ports 4 and 8

### I-TDM Interface

- 1024 bidirectional 64kbit/s channels
- 125  $\mu$ s-mode and 1ms-mode support

### TDM (optional)

H.110 alike 32MHz clocked TDM interface connects to ports 12, 13 (data) and port 14 (sync) of the extended options region of the AMC connector

### Indicator LEDs

- 8/16 (extension module) bicolour LEDs integrated in the RJ45 for E1 link status
- 2 standard LEDs as fault indicator and for general purpose status

### Host Operating System Support

- LINUX

### Power Consumption

- 12 V, 1A

### Environmental Conditions

- Operating temp.: 0°C to +60°C with forced cooling
- Storage temp.: -40°C to +85°C
- Humidity: 10% to 90% rh noncondensing

### Standard Compliance

- PICMG AMC.0 Rev. 2.0/AMC.1 Rev. 1.0/AMC.2 Rev. 1.0 (Type E2)
- PCIe Base Spec. Rev. 1.1
- PICMG SFP.0 Rev. 1.0/SFP.1 Rev. 1.0 (Internal CC)
- IPMI Spec. v2.0 Rev. 1.0
- PICMG MTCA.0 Rev. 1.0
- ITU-T G.823 (Jitter Attenuation)