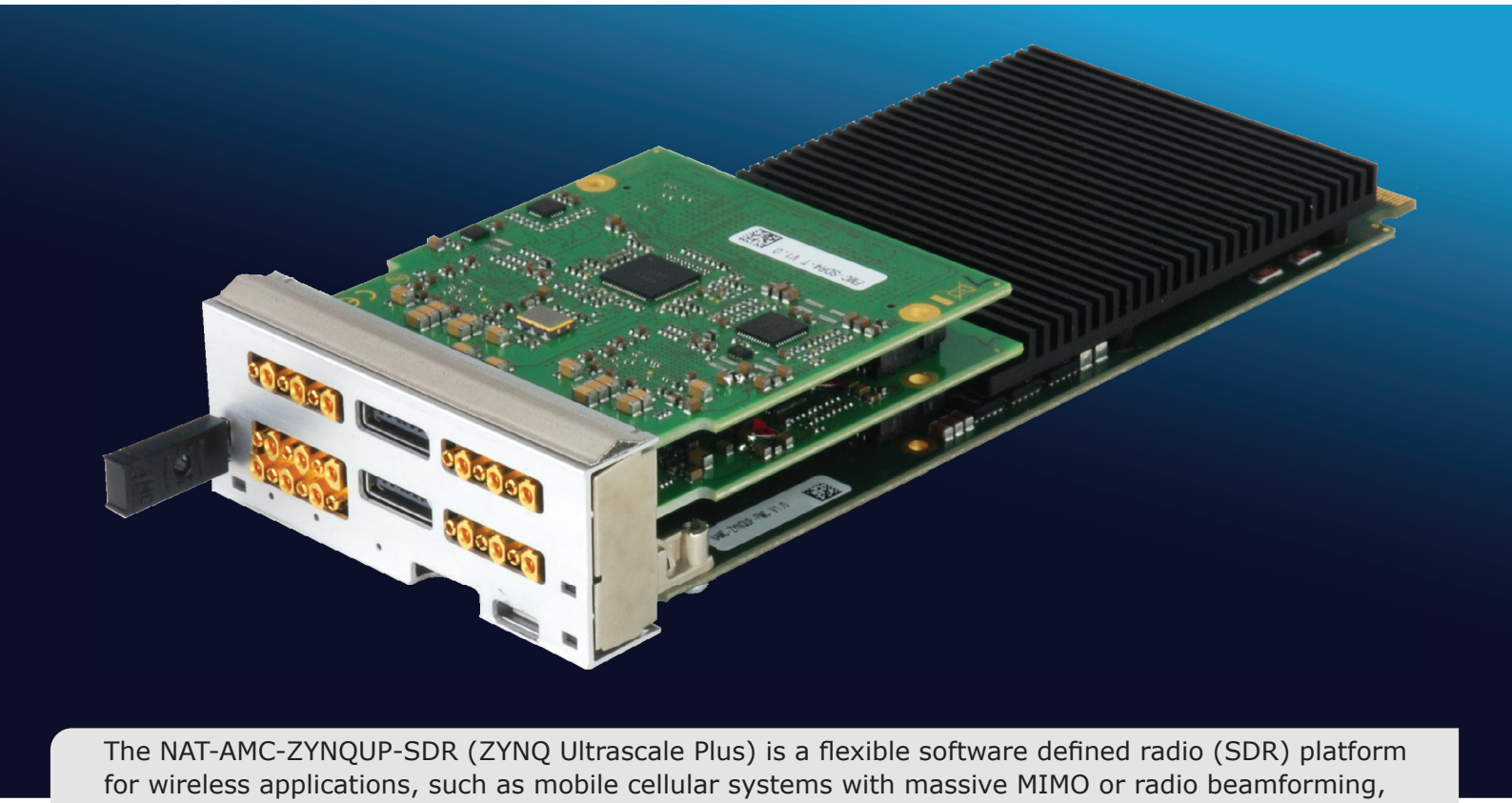
NAT-AMC-ZYNQUP-SDR

AMC with Xilinx Zynq UltraScale+ & 4x ADRV9009 Transceiver



The NAT-AMC-ZYNQUP-SDR (ZYNQ Ultrascale Plus) is a flexible software defined radio (SDR) platform for wireless applications, such as mobile cellular systems with massive MIMO or radio beamforming, which require a large number of phase-coherent antennas. It can support four or eight channels, defined by the number of stacked mezzanine cards.

The synchronization of multiple SDR boards enables you to create large antenna arrays with RF phase-coherent radio channels. The on-board Xilinx® Zynq® UltraScale+™ FPGA provides a powerful general-purpose ARM-CPU, field-programmable hardware accelerators (FPGA, DSP, and GPU) and flexible IO for signal and base band processing.

The combination of large bandwidth RF-transceivers and a powerful FPGA allows you to create 5G radio units with on-board PHY layer processing or NB-IoT/LTE full-network single-board solutions with base station and core network processing.

Key features

- Flexible software defined radio (SDR) platform
- Synchronizable for creating large phased arrays
- 4 or 8 RX/TX channels with 200 MHz instantaneous bandwidth each
- Observation receiver for Digital Pre-Distortion (DPD)
- Xilinx® Zynq® UltraScale+™ FPGA SoC ZU7EG or ZU11EG
- AMC form factor

Applications

- 4G/5G base station
- 5G radio unit (RU) with PHY processing
- Cellular prototyping
- Phased arrays
- Radio direction finding and tracking
- Frequency scanner and signal intelligence
- Radio astronomy
- Advanced wireless research
- Prototyping

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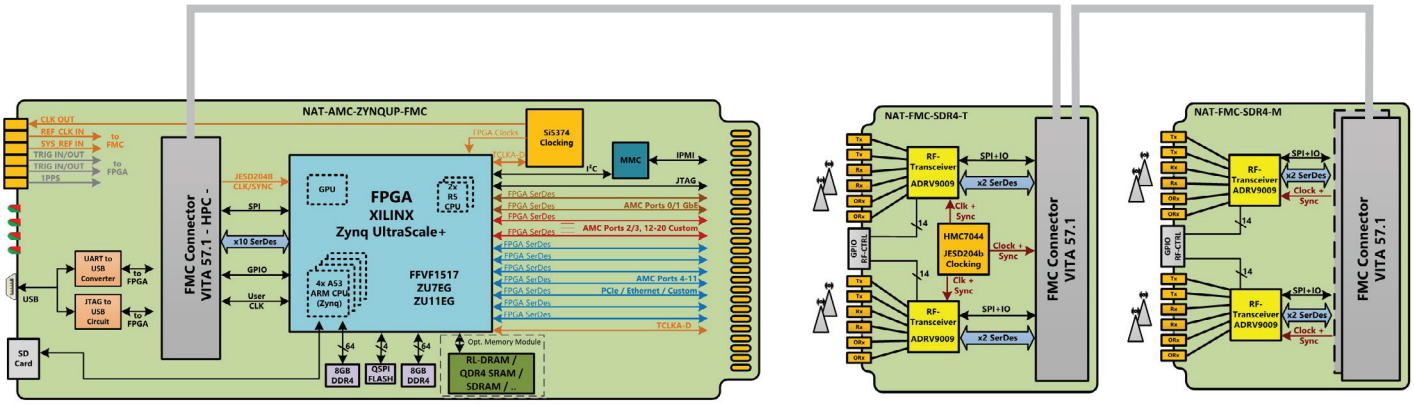
Technical Data

NAT-AMC-ZYNQUP-SDR



Overview

Consisting of a stacked FPGA base board and two radio frequency front-end mezzanine cards, the NAT-AMC-ZYNQUP-SDR supports different communication standards with variable signal bandwidths, carrier frequencies and transmit power.

Software Support

The default board support package and firmware contains all modules for starting development of the target application.

- Embedded Linux OS for controlling FPGA IP cores and on-board devices
- Device drivers (ADRV9009, Clocking, etc.)
- Sample applications for Matlab and GNURadio
- Applications for control and management
- Software documentation

The advanced firmware package additionally contains a real time PCIe IQ streaming driver for external signal processing units.

FPGA Reference Design

N.A.T. provides an FPGA project template / reference design for Xilinx Vivado Design Suite with board-specific modules that can be used as a base frame for developing the target application. It contains modules for:

- ADRV9009 RF transceivers
- JESD204b interfaces
- PCIe to MTCA backplane
- Gbit Ethernet to MTCA backplane
- Local clocking
- Clocking to MTCA backplane

Specifications

RF-Transceiver

- 4x Analog Devices ADRV9009 dual RF transmitter, receiver and observation receiver
- Maximum receiver bandwidth: 200 MHz
- Maximum tuneable transmitter synthesis bandwidth: 450 MHz
- Maximum observation receiver bandwidth: 450 MHz
- Multichip phase synchronization for RF- and baseband signals
- Multiboard synchronization
- JESD204B IQ sample data interface to FPGA
- Tuning range (center frequency): 75 MHz to 6000 MHz
- RX gain range: 30dB in 0.5dB steps
- RX Noise Figure: 2dB @ 800 MHz
3dB @ 2.4 GHz
3.8 dBm @ 5.5 GHz
- Maximum output power: 9 dBm @ 75 MHz < f ≤ 600 MHz
7 dBm @ 600 MHz < f ≤ 4000 MHz
6 dBm @ 4000 MHz < f ≤ 4800 MHz
4.5 dBm @ 4800 MHz < f ≤ 6000 MHz
- TX Error Vector Magnitude (EVM): 0.5% @ 75 MHz LO
0.7% @ 1900 MHz LO
0.7% @ 3800 MHz LO
1.1% @ 5900 MHz LO
- 3rd order output intermodulation OIP3: 23 dBm @ 800 MHz
19 dBm @ 2.4 GHz
17 dBm @ 5.5 GHz

Processing Resources

- System on Chip (SoC) Xilinx UltraScale+ ZU7EG or ZU11EG - F1517 footprint
- Application processor: Quad-core ARM Cortex-A53 MPCore up to 1.5 GHz
- Real-time processor: Dual-core ARM Cortex-R5 MPCore up to 600 MHz
- System logic cells: 504k / 653k
- DSP slices: 1728 / 2928
- 14x GTH 16.3Gb/s transceivers to MTCA backplane
- 10x GTH 16.3Gb/s transceivers to mezzanine cards

Memory & Storage

- 8GB DDR4 (x64, 1600-3200Mb/s) for ARM-CPU (PS)
- 8GB DDR4 (x64, 1600-3200Mb/s) for FPGA (PL)
- 4GB eMMC
- SD card holder
- QSPI flash
- Connector for additional memory modules
- Optional RLDRAM3 on module (2133Mb/s, 1 Gb, x36, 8ns tRC) for low latency access (up to 6 times faster than DDR4-3200). Useful for applications requiring RAM look up tables (LUTs)
- Optional QDR4 SRAM or additional DDR4-SDRAM

Backplane Connection

- Full AMC TCLKA-D and FCLKA connectivity (bidirectional)
- Ports 0, 1, 4-15 to FPGA GTH 16.3 Gb/s transceivers
- Dual 1 Gb/s Ethernet
- 10/40 Gb/s Ethernet via FPGA
- One x8 or dual x4 PCI Express Gen3 via FPGA or
- Dual x4 SRIO/XAUI via FPGA
- Any combinations of PCIe, SRIO, XAUI (on request)
- 2x4 point to point links (low latency) to FPGA
- 4 trigger lines
- Ports for SATA, SAS
- IPMI for module management
- JTAG

Front panel

8 TX, 8 RX, 8 ORX

- 4 x 7 GPIO 1V8 to ADRV9009
- 4 x 4 GPIO 3V3 to ADRV9009
- 12 x GPIO 1V8 to FPGA
- 1 PPS IN
- CLK OUT
- CLK IN (JESD204b)
- SYNC for JESD204b
- 2x Trigger IN/OUT to FPGA
- SD card holder
- UART-USB serial console for ARM core and MMC
- AMC standard LEDs and hot swap handle
- Application LEDs

Physical Dimensions

- Single-wide, full-size AMC
- Width 73.5mm, depth 180.6mm

Compliance

- AMC.0 R2.0, AMC.1, AMC.2, AMC.3, AMC.4, IMPI V1.5, HPM.1
- EN60950, UL1950, RoHS

Customization

The NAT-AMC-ZYNQUP-SDR8 consists of an FMC Carrier FPGA Board (NAT-AMC-ZYNQUP-FMC) with one or two stacked RF mezzanine boards in the FMC form factor (NAT-FMC-SDR4-T alone gives you four channels and NAT-FMC-SDR4-T plus NAT-FMC-SDR4-M gives you eight channels). This modularity makes the platform extremely flexible since you can change the RF front end and front panel I/O simply by choosing N.A.T.'s FMC-boards with the desired functions. SDR properties, such as number of RF channels, filtering, control IO for external RF components and high speed interface ports (e.g. QSFP), can be brought into the platform by choosing the right FMC building blocks. Custom mezzanine cards with special functions can be developed in close collaboration with N.A.T.