NAT-MCH-40G-XAUI

NAT-MCH-HUB-MODULE

DESIGNED BY N.A.T. GMBH

TECHNICAL REFERENCE MANUAL V1.3

HW REVISION 1.X

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1. PREFACE

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Note:

The release of the Hardware Manual is related to a certain HW board revision given in the document title. For HW revisions earlier than the one given in the document title please contact N.A.T. for the corresponding older Hardware Manual release.

1.2. About This Document

This document is intended to give an overview on the **NAT-MCH-40G-XAUIs** functional capabilities.

Preface

General information about this document

Introduction

Abstract on the **NAT-MCH-40G-XAUIs** main functionality and application field

Quick Start

Important information and mandatory requirements to be considered before operating the **NAT-MCH-40G-XAUIs** for the first time

Functional Description

Detailed information on the individual devices and the **NAT-MCH-40G-XAUIs** main features

Hardware

Information about LEDs, connectors, and port assignments

Firmware Update

Description of the firmware update procedure

Specifications and Compliances

Detailed list of specifications, abbreviations, and datasheets of components referred to in this document, as well as standards, the **NAT-MCH-40G-XAUI** complies to

Document's History

Revision record

Note:

It is assumed, that the **NAT-MCH-40G-XAUI** is handled by qualified personnel only!

2. INTRODUCTION

The **NAT-MCH-40G-XAUI** is a single-width HUB-module applicable for the single-width **NAT-MCH-Base** and the double-width **NAT-MCH-M4** (which is the base board of the **NAT-MCH-PHYS/-PHYS80**) as well.

As an upgrade option of the **NAT-MCH-XAUI** HUB-module, the **NAT-MCH-40G-XAUI** quadruples the backplane bandwidth and increases the optical uplink bandwidth by a factor of fifteen.

2.1. Basic Functionality

The **NAT-MCH-40G-XAUI** provides twelve lanes of up to 40GbE to the backplane and three optical uplinks of up to 100GbE towards the front plate. The maximum uplink speed depends on the chosen transceiver type.

2.2. Applications

The **NAT-MCH-40G-XAUI** is highly suitable for applications demanding highest bandwidth Ethernet in MTCA towards the backplane and the front panel.

2.3. Main Features

Table 1 – Technical Data

Form Factor		
	• Single-width, full-size AMC • Width: 73.5 mm, Depth: <180.6 mm	
Compatible MCH		
	• **NAT-MCH-BASE6-GbE** • **NAT-MCH-BASE12-GbE** • **NAT-MCH-M4** (as base board for **NAT-MCH-PHYS/-PHYS80**) • PCIe-HUB-Module can be replaced by **NAT-MCH-40G-XAUI**	
On-Board Resources		
CPU	• Dual ARM A53 Core Marvell 88F3720 with configuration interface	
Memory	• 4GB eMMC • 2GB DRAM DDR4-1600, 16bit • MicroSD-Card slot (for N.A.T. internal use)	
Ethernet Switch	• Marvell 98EX5520 “Armstrong-LP” 10G/40G/100G	
PIPE	• 4x Marvell 98PX1012 Passive Intelligent Port Extenders (PIPE) “Prestera-LP”	
Front Panel Uplink (optional)		

Optical Uplink Transceiver	• MTP/MPO connector
	• Finisar BOA 12 lanes ***10G***
	  • max. 10GbE per x1 port
	  => max. 40GbE per x4 port
		• MTP/MPO connector
		• Finisar BOA 12 lanes ***25G***
		  • max. 25GbE per x1 port
		  => max. 100GbE per x4 port

Ethernet Uplink Speed	• 1G-1000BASEX • 10G-KR • 40G-KR4	• 1G-1000BASEX • 10G-KR • 40G-KR4 • 100G-KR4
Current Ethernet Uplink Configuration	• Three x4 port up to 40 GbE each ***or*** • Twelve x1 ports up to 10GbE each	• Two x4 ports up to 100GbE each AND one x4 port up to 40 GbE ***or*** • Eight x1 ports up to 25GbE each AND four x1 ports up to 10GbE each
LEDs		
Indicator LEDs	• 12 LEDs for Ethernet status and activity of 12 AMC slots • 3 bi-colored LEDs for Ethernet status and activity of 3 optical uplinks • 1 bi-colored LED for Ethernet status and activity of downlink to CPU on **NAT-MCH-BASE**	
Backplane Interconnect		
AMC-Interconnection	• 1G-1000BASEX • 10G-KR • 10G-XAUI • 40G-KR4 • Mixture of 40 GbE and 10 GbE infrastructure • combination of 1 up to 4 lanes and 2.5 and 10 Gbaud per lane per AMC slot	
2nd MCH update-channel	• up to 40 GbE, performance depending on backplane	

Supported Features	
Port On/Off	• Supported
802.1Q VLAN	• Supported
Jumbo Frames	• Supported
Link Status	• Supported
Port-Based VLAN	• Supported
Link Aggregation	• By firmware upgrade, available soon
Packet Counters	• By firmware upgrade, available soon
Onboard Temperature Sensors	• By firmware upgrade, available soon
Compliance	
	• AMC.0 R2.0, AMC.1, IMPI V1.5, HPM.1 • EN60950, UL1950, RoHS
Order Codes	
NAT-MCH-40G-XAUI-<Opt>	• Single-width MCH sub-module with 10/40/100GbE Ethernet switch • <Opt>: None, O-40G, O-100G (preliminary, will be updated)
NAT-MCH-CABLE-<Length>	• optical cable • <Length>: 2m, 5m, 25m (preliminary, will be updated) • other cable length on request
Environmental	
Operating Environment	• default: 0 to +50 degrees Celsius • optional: -25 to +85 degrees Celsius • optional: -40 to +100 degrees Celsius • Humidity: 5% to 95% (non-condensing) • Vibrations: sinusoidal , 0.38mm pk from 5Hz to 36Hz, 2g from 36Hz to 2KHz • Shocks: 20g, 11ms, 1⁄2 sine • Altitude: 0 to 5000m
Storage Environment	• default: -40 to +100 degrees Celsius • Humidity: 5% to 95% (non-condensing) • Vibrations: sinusoidal , 0.38mm pk from 5Hz to 36Hz, 3g from 36Hz to 2KHz • Shocks: 30g, 11ms, 1⁄2 sine • Altitude: 0 to 15000m

3. QUICK START

As the **NAT-MCH-40G-XAUI** is only available mounted on a **NAT-MCH** baseboard, please refer to the according manual for information about quick start, unpacking, mechanical and electrical requirements.

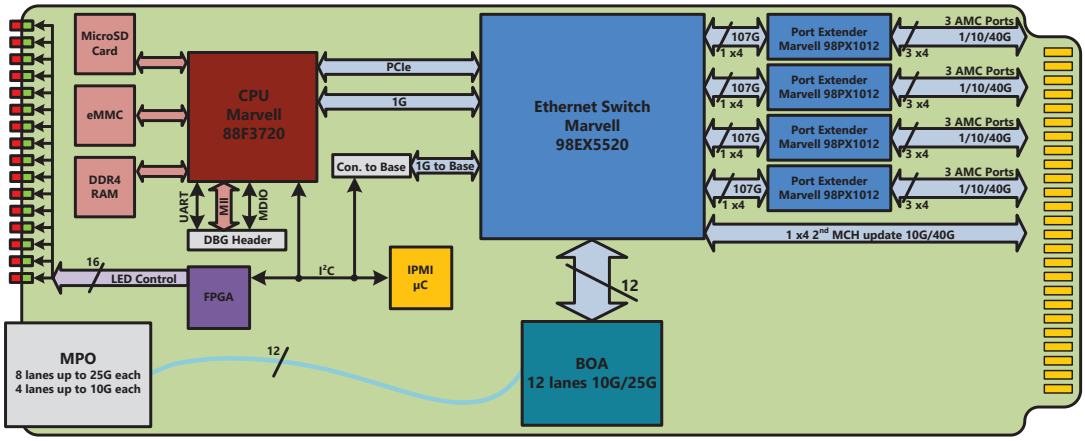
References are given in chapter 7.1 Internal Reference Documentation.

4. FUNCTIONAL DESCRIPTION

The **NAT-MCH-40G-XAUI** can be divided into a number of functional blocks, which are described in the following paragraphs.

The figure below gives an overview on the functional blocks.

Figure 1 – Block Diagram NAT-MCH-40G-XAUI



4.1. CPU and associated Memory

The **NAT-MCH-40G-XAUI** is equipped with a Marvell 88F3720 CPU with dual ARM A53 core. It has 4GB eMMC available, as well as 2GB DRAM DDR4-1600, 16 bit wide. For N.A.T.-internal use, also a MicroSD-Card slot is mounted.

4.2. Ethernet Switch

The **NAT-MCH-40G-XAUI** features a Marvell 98EX5520 “Armstrong-LP”.

The Switch Port assignment between the Ethernet switch and the PIPEs is described in chapter 5.3 Port Assignment.

4.3. Port Extenders (PIPE)

For providing XAUI functionality, the **NAT-MCH-40G-XAUI** owns four Marvell 98PX1012 passive intelligent port extenders (PIPE) “Prestera-LP”.

The Switch Port assignment of the PIPEs is described in chapter 5.3 Port Assignment.

4.4. Optical Transceiver (optional)

With the **NAT-MCH-40G-XAUI**, an optional Finisar BOA optical transceiver can be assembled to provide uplinks. It then provides twelve lanes of optical uplinks via fiber connection towards the front panel.

Two transceiver types are available, one providing10G per lane, and one providing 25G per lane. With the first one, the speed is limited to 10GbE per every x1 port, which results in 40GbE per x4 port. The second option offers 25GbE per every x1 port, which results in 100GbE per x4 port.

The optical connection from the Finisar BOA transceiver to the front uplink port of the **NAT-MCH-40G-XAUI** is realized by an optical cable, which is plugged into a mechanical guide at the front panel. The twelve lanes flow into one MTP/MPO connector (please refer to chapter 5.2.1 Optical Uplink Connector).

Due to hardware restrictions, the uplink can be configured only to one of the options shown in the following paragraphs. Other configurations can be implemented on request.

Please note: the following figures show the view of the connector ***from the front***.

Please note: naming starts with "Uplink Port3", as Uplink Port1 and 2 are located on the base board of the **NAT-MCH**.

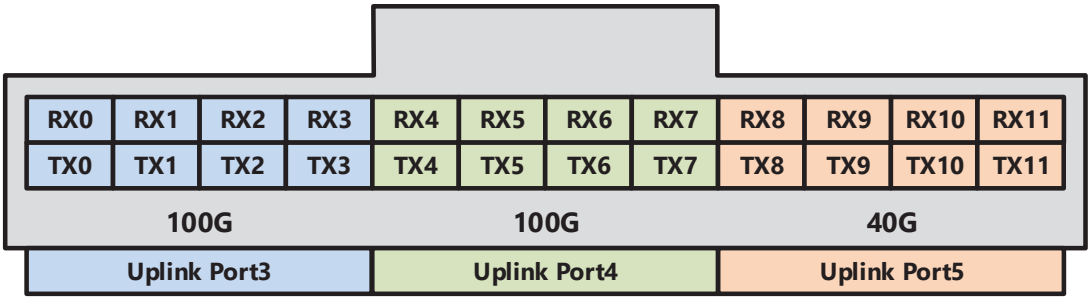
The uplink-status is reflected via three LEDs at the front panel (Uplink 3-5).

The 4th LED shows the status of a downlink to the CPU on the **NAT-MCH-BASE6 /-BASE12**.
Please note: this connection is not available with the **NAT-MCH-PHYS /-PHYS80**.

4.4.1. Uplink Port Assignments 25G-Transceiver

Option #1: two x4 ports with up to 100G each AND one x4 port with up to 40G.

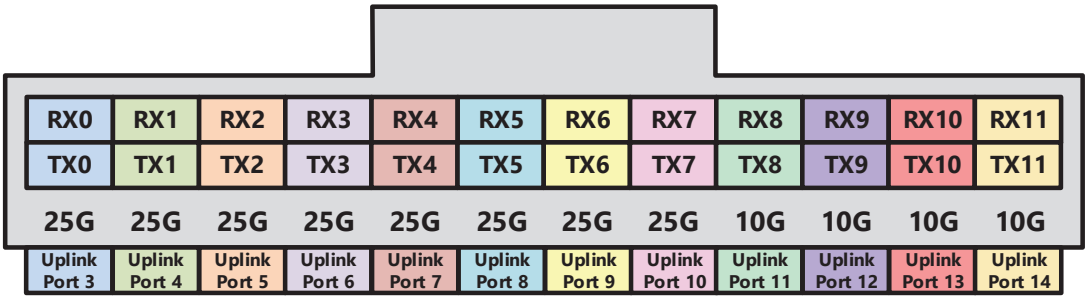
Figure 2 – 25G-Uplink Port Assignment #1



or

Option #2: eight x1 ports with up to 25G each AND four x1 ports with up to 10G each.

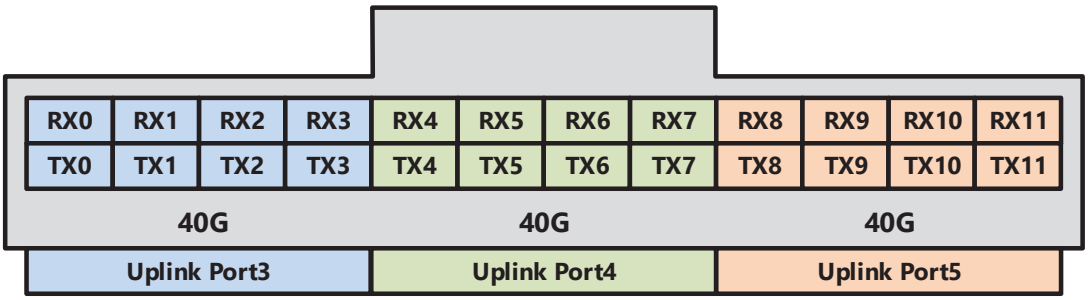
Figure 3 – 25G-Uplink Port Assignment #2



4.4.2. Uplink Port Assignments 10G-Transceiver

Option #1: three x4 ports up to 40 GbE.

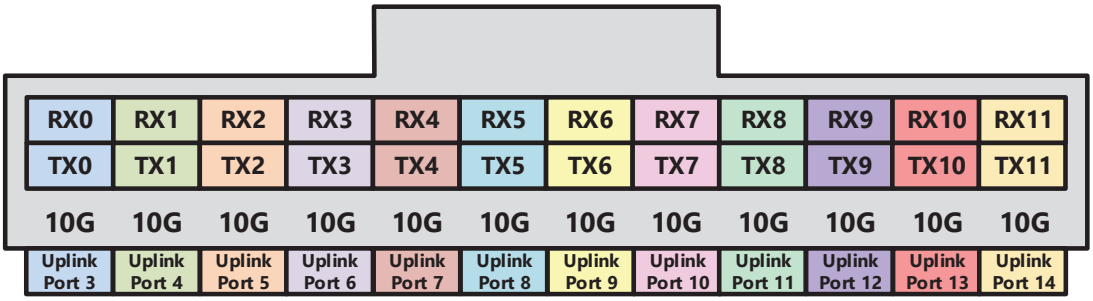
Figure 4 – 10G-Uplink Port Assignment #1



or

Option #2: twelve x1 ports up to 10GbE each.

Figure 5 – 10G-Uplink Port Assignment #2



4.4.3. MTP/MPO to SFP+ Compatibility

The MTP/MPO interface is fully compatible to an SFP+ interface with 850nm multimode SR. There are different options to connect the **NAT-MCH-40G-XAUI** optical uplink port to external equipment.

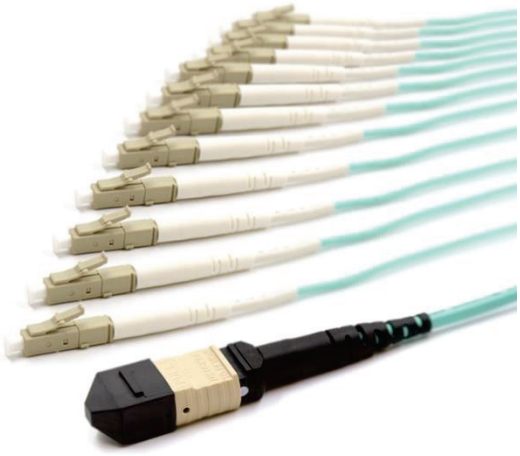
Table 2 – MPO to SFP+ Port Mapping*

Interface	LC Connectors
Optical Uplink #0	12/24
Optical Uplink #1	11/23
Optical Uplink #2	10/22
Optical Uplink #3	9/21
Optical Uplink #4	8/20
Optical Uplink #5	7/19
Optical Uplink #6	6/18
Optical Uplink #7	5/17
Optical Uplink #8	1/13
Optical Uplink #9	2/14
Optical Uplink #10	4/16
Optical Uplink #11	3/15

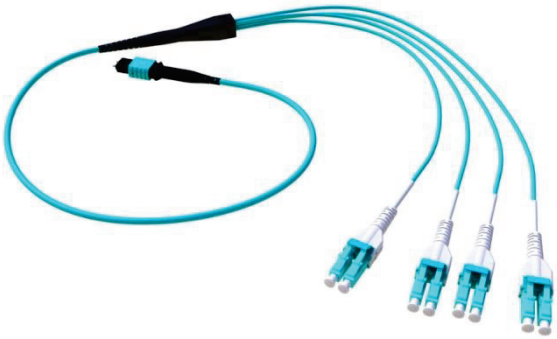
* With cable type Sylex 01x MTP(F) - 24x LC/PC 24F OM4 FANOUT 02.0M FL10

Other examples for off-the-shelf fan-out fibres, that can be used to divide the MPO-Interface into connectors with several SerDes lanes, can be found below.

Figure 6 – Fan-Out Fiber



https://fibertronics.com/1m-mtp-male-to-24-lc-upc-24-fiber-multimode-om3-50125-breakout-cable



https://www.sylex.sk/product/mtp-cxp-mtp-qsfp-kabel/

https://www.fs.com/de/products/69995.html

A fan-out adapter box features one MTP/MPO interface and several LC connectors, so existing cabling can be used. An example can be found below.

Figure 7 – Adapter Box

https://www.fs.com/de/products/57024.html

For connecting two MTP/MPO connectors, an example can be found below.

Figure 8 – MPO Cable Connector

https://www.fs.com/de-en/products/61898.html

4.5. FPGA

The **NAT-MCH-40G-XAUI** features a Lattice MACHXO2-FPGA for LED control.

4.6. Microcontroller

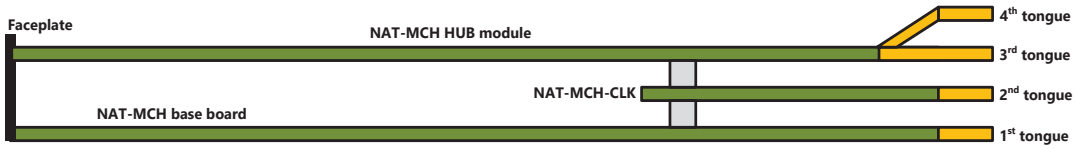
An Atmel ATmega128 microcontroller works as IPMI controller.

4.7. Interface to Mezzanines

The **NAT-MCH-40G-XAUI** interfaces with the **NAT-MCH-CLK** module, the **NAT-MCH-CLK-PHYS** module, or a **NAT-MCH-CLK** spacer, which on its part is connected to the **NAT-MCH** baseboard.

The arrangement of the mezzanines is shown in the figure below.

Figure 9 – Arrangement of Mezzanine Modules



5. HARDWARE

5.1. Front Panel and LEDs

The **NAT-MCH-40G-XAUI** is equipped with various LEDs described in the following sections.

Figure 10 – NAT-MCH-40G-XAUI: Front Panel – Base12 (Preliminary)

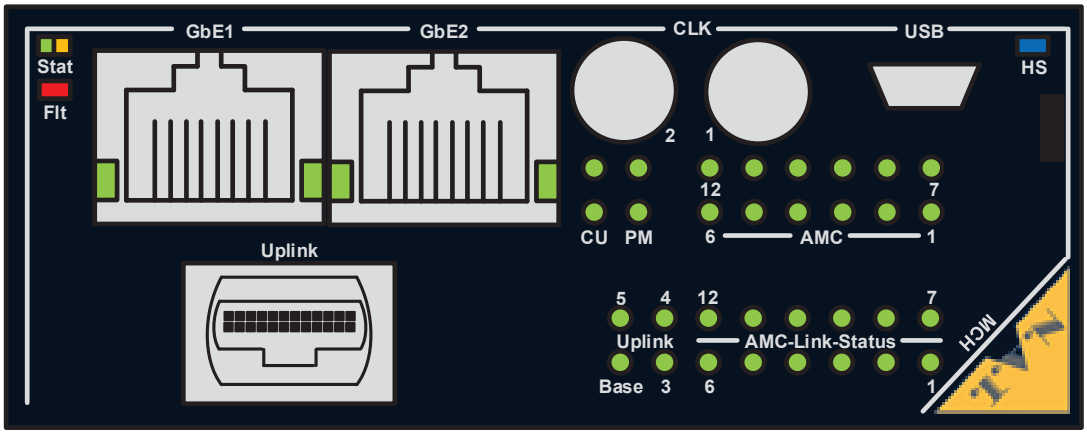


Table 3 – LED Functionality (Preliminary)

LED	Color	Function
3x Uplink-Status	OFF	no link established
	Green slow blink	1G link established
	Green fast flash	10G link established
	Green solid ON	25G link established
	Orange slow blink	40G link established
	Orange fast flash	100G link established
	Red solid ON	Fault
12x AMC-Status	OFF	no link established
	Green slow blink	1G link established
	Green fast flash	10G link established
	Orange slow blink	40G link established
	Red solid ON	Fault
Downlink-Status to **NAT-MCH-BASE** (Base6/Base12 only)	OFF	no link established
	Green slow blink	1G link established
	Red solid ON	Fault

5.2. Component-, Connector-, and Switch-Location

Figure 11 – Location Diagram – Top

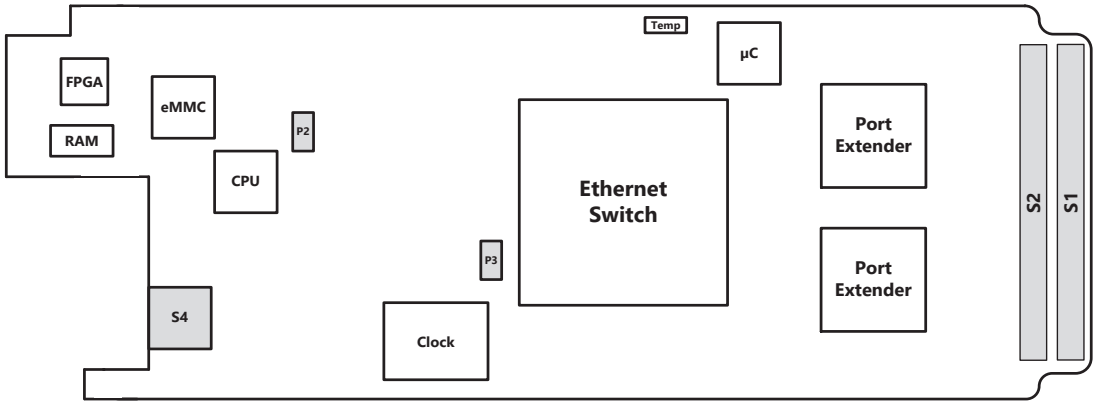
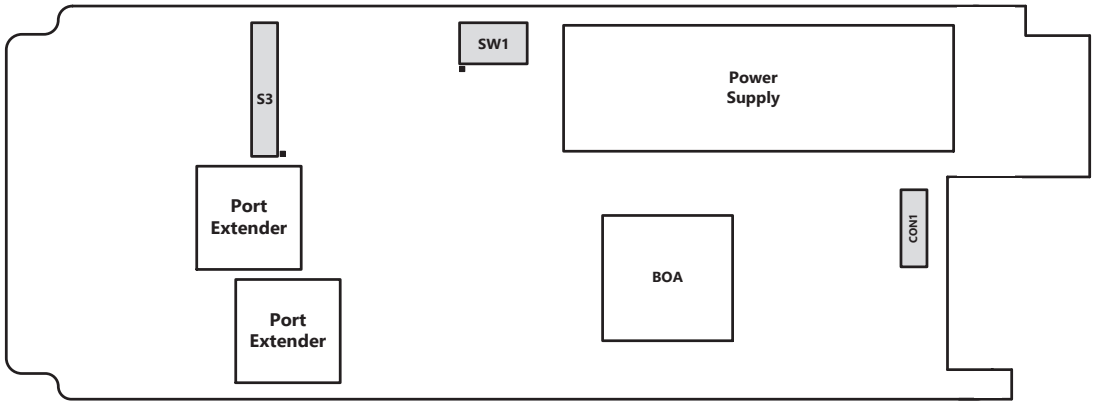


Figure 12 – Location Diagram – Bottom

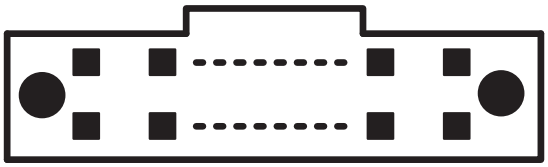


Please refer to the following tables to look up the connector pin assignment of the **NAT-MCH-40G-XAUI**.

5.2.1. Optical Uplink Connector

As an option, the **NAT-MCH-40G-XAUI** features an MTP/MPO connector.

Figure 13 – Optical Uplink Connector (view on front panel)



For detailed information on the uplink port assignment, please refer to chapter 4.4 Optical Transceiver (optional).

5.2.2. CON1: Debug Header

Connector CON1 offers a debug interface for internal use only.

Figure 14 – CON1: Debug Header

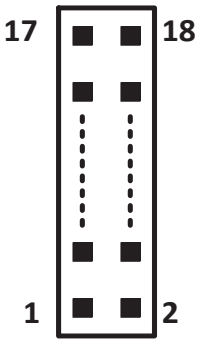


Table 4 – CON1: Debug Header – Pin Assignment

Pin #	Signal	Signal	Pin #
1	MII_MDC	3V3	2
3	MII_TXCLK	MII_RXCLK	4
5	MII_TXD0	MII_RXD0	6
7	MII_TXD1	MII_RXD1	8
9	MII_TXD2	MII_RXD2	10
11	MII_TXD3	MII_RXD3	12
13	MII_TXDEN	MII_RXDV	14
15	UART2_TX	UART2_RX	16
17	GND	MII_MDIO	18

5.2.3. P2: CPU Programming Port

P2 connects to the programming interface of the Marvell 88F3720 CPU.

Figure 15 – P2: CPU Programming Port

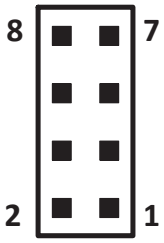


Table 5 – P2: CPU Programming Port – Pin Assignment

Pin #	Signal	Signal	Pin #
1	2V5	ARM_TDO	2
3	ARM_CLK	ARM_TMS	4
5	RST	ARM_TDI	6
7	GND	GND	8

5.2.4. P3: Ethernet Switch Programming Port

P3 connects the programming interface of the Marvell 98EX5520 Ethernet switch.

Figure 16 – P3: Ethernet Switch Programming Port

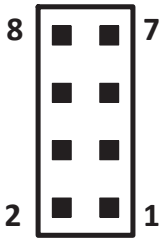


Table 6 – P3: Ethernet Switch Programming Port – Pin Assignment

Pin #	Signal	Signal	Pin #
1	SWITCH_TDO	3V3	2
3	SWITCH_TDI	SWITCH_JRST#	4
5	SWITCH_TMS_CORE	SWITCH_TCK	6
7	GND	SWITCH_TMS_CPU	8

5.2.5. S1: MCH Edge Connector (3rd Tongue)

The **NAT-MCH-40G-XAUI** connects to the 3rd tongue of the backplane via S1.

Figure 17 – S1: MCH Edge Connector (3rd Tongue)

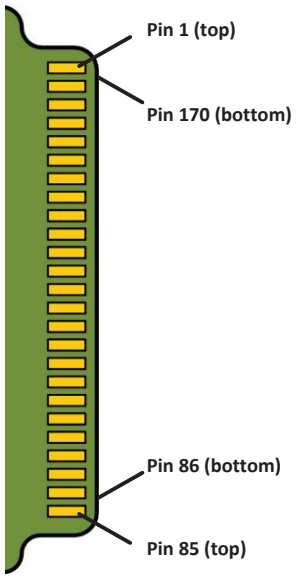


Table 7 – S1: MCH Edge Connector (3rd Tongue) – Pin Assignment

Pin #	Signal	Signal	Pin #
1	GND	GND	170
2	RSVD	nc	169
3	RSVD	nc	168
4	GND	GND	167
5	RSVD	nc	166
6	RSVD	nc	165
7	GND	GND	164
8	TxFUD_P	C_RxFUD_P	163
9	TxFUD_N	C_RxFUD_N	162
10	GND	GND	161
11	TxFUE_P	C_RxFUE_P	160
12	TxFUE_N	C_RxFUE_N	159
13	GND	GND	158
14	TxFD-1_P	C_RxFD-1_P	157
15	TxFD-1_N	C_RxFD-1_N	156
16	GND	GND	155
17	TxFE-1_P	C_RxFE-1_P	154
18	TxFE-1_N	C_RxFE-1_N	153
19	GND	GND	152
20	TxFF-1_P	C_RxFF-1_P	151
21	TxFF-1_N	C_RxFF-1_N	150
22	GND	GND	149

Pin #	Signal	Signal	Pin #
23	TxFG-1_P	C_RxFG-1_P	148
24	TxFG-1_N	C_RxFG-1_N	147
25	GND	GND	146
26	TxFD-2_P	C_RxFD-2_P	145
27	TxFD-2_N	C_RxFD-2_N	144
28	GND	GND	143
29	TxFE-2_P	C_RxFE-2_P	142
30	TxFE-2_N	C_RxFE-2_N	141
31	GND	GND	140
32	TxFF-2_P	C_RxFF-2_P	139
33	TxFF-2_N	C_RxFF-2_N	138
34	GND	GND	137
35	TxFG-2_P	C_RxFG-2_P	136
36	TxFG-2_N	C_RxFG-2_N	135
37	GND	GND	134
38	TxFD-3_P	C_RxFD-3_P	133
39	TxFD-3_N	C_RxFD-3_N	132
40	GND	GND	131
41	TxFE-3_P	C_RxFE-3_P	130
42	TxFE-3_N	C_RxFE-3_N	129
43	GND	GND	128
44	TxFF-3_P	C_RxFF-3_P	127
45	TxFF-3_N	C_RxFF-3_N	126
46	GND	GND	125
47	TxFG-3_P	C_RxFG-3_P	124
48	TxFG-3_N	C_RxFG-3_N	123
49	GND	GND	122
50	TxFD-4_P	C_RxFD-4_P	121
51	TxFD-4_N	C_RxFD-4_N	120
52	GND	GND	119
53	TxFE-4_P	C_RxFE-4_P	118
54	TxFE-4_N	C_RxFE-4_N	117
55	GND	GND	116
56	TxFF-4_P	C_RxFF-4_P	115
57	TxFF-4_N	C_RxFF-4_N	114
58	GND	GND	113
59	TxFG-4_P	C_RxFG-4_P	112
60	TxFG-4_N	C_RxFG-4_N	111
61	GND	GND	110
62	TxFD-5_P	C_RxFD-5_P	109
63	TxFD-5_N	C_RxFD-5_N	108
64	GND	GND	107
65	TxFE-5_P	C_RxFE-5_P	106
66	TxFE-5_N	C_RxFE-5_N	105
67	GND	GND	104
68	TxFF-5_P	C_RxFF-5_P	103
69	TxFF-5_N	C_RxFF-5_N	102
70	GND	GND	101
71	TxFG-5_P	C_RxFG-5_P	100

Pin #	Signal	Signal	Pin #
72	TxFG-5_N	C_RxFG-5_N	99
73	GND	GND	98
74	TxFD-6_P	C_RxFD-6_P	97
75	TxFD-6_N	C_RxFD-6_N	96
76	GND	GND	95
77	TxFE-6_P	C_RxFE-6_P	94
78	TxFE-6_N	C_RxFE-6_N	93
79	GND	GND	92
80	TxFF-6_P	C_RxFF-6_P	91
81	TxFF-6_N	C_RxFF-6_N	90
82	GND	GND	89
83	TxFG-6_P	C_RxFG-6_P	88
84	TxFG-6_N	C_RxFG-6_N	87
85	GND	GND	86

5.2.6. S2: MCH Edge Connector (4th Tongue)

The **NAT-MCH-40G-XAUI** connects to the 4th tongue of the backplane via S2.

Figure 18 – S2: MCH Edge Connector (4th Tongue)

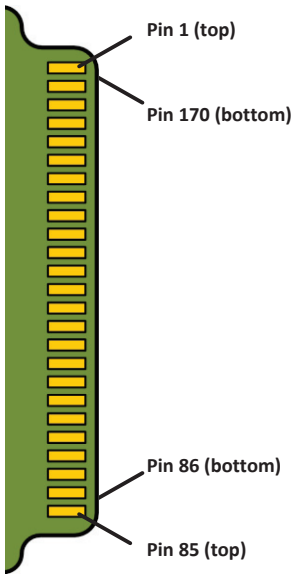


Table 8 – S2: MCH Edge Connector (4th Tongue)

Pin #	Signal	Signal	Pin #
1	GND	GND	170
2	RSVD	nc	169
3	RSVD	nc	168
4	GND	GND	167
5	RSVD	nc	166
6	RSVD	nc	165
7	GND	GND	164
8	TxFUF_P	C_RxFUF_P	163
9	TxFUF_N	C_RxFUF_N	162
10	GND	GND	161
11	TxFUG_P	C_RxFUG_P	160
12	TxFUG_N	C_RxFUG_N	159
13	GND	GND	158
14	TxFD-7_P	C_RxFD-7_P	157
15	TxFD-7_N	C_RxFD-7_N	156
16	GND	GND	155
17	TxFE-7_P	C_RxFE-7_P	154
18	TxFE-7_N	C_RxFE-7_N	153
19	GND	GND	152
20	TxFF-7_P	C_RxFF-7_P	151
21	TxFF-7_N	C_RxFF-7_N	150
22	GND	GND	149
23	TxFG-7_P	C_RxFG-7_P	148
24	TxFG-7_N	C_RxFG-7_N	147
25	GND	GND	146
26	TxFD-8_P	C_RxFD-8_P	145
27	TxFD-8_N	C_RxFD-8_N	144
28	GND	GND	143
29	TxFE-8_P	C_RxFE-8_P	142
30	TxFE-8_N	C_RxFE-8_N	141
31	GND	GND	140
32	TxFF-8_P	C_RxFF-8_P	139
33	TxFF-8_N	C_RxFF-8_N	138
34	GND	GND	137
35	TxFG-8_P	C_RxFG-8_P	136
36	TxFG-8_N	C_RxFG-8_N	135
37	GND	GND	134
38	TxFD-9_P	C_RxFD-9_P	133
39	TxFD-9_N	C_RxFD-9_N	132
40	GND	GND	131
41	TxFE-9_P	C_RxFE-9_P	130
42	TxFE-9_N	C_RxFE-9_N	129
43	GND	GND	128
44	TxFF-9_P	C_RxFF-9_P	127
45	TxFF-9_N	C_RxFF-9_N	126
46	GND	GND	125
47	TxFG-9_P	C_RxFG-9_P	124

Pin #	Signal	Signal	Pin #
48	TxFG-9_N	C_RxFG-9_N	123
49	GND	GND	122
50	TxFD-10_P	C_RxFD-10_P	121
51	TxFD-10_N	C_RxFD-10_N	120
52	GND	GND	119
53	TxFE-10_P	C_RxFE-10_P	118
54	TxFE-10_N	C_RxFE-10_N	117
55	GND	GND	116
56	TxFF-10_P	C_RxFF-10_P	115
57	TxFF-10_N	C_RxFF-10_N	114
58	GND	GND	113
59	TxFG-10_P	C_RxFG-10_P	112
60	TxFG-10_N	C_RxFG-10_N	111
61	GND	GND	110
62	TxFD-11_P	C_RxFD-11_P	109
63	TxFD-11_N	C_RxFD-11_N	108
64	GND	GND	107
65	TxFE-11_P	C_RxFE-11_P	106
66	TxFE-11_N	C_RxFE-11_N	105
67	GND	GND	104
68	TxFF-11_P	C_RxFF-11_P	103
69	TxFF-11_N	C_RxFF-11_N	102
70	GND	GND	101
71	TxFG-11_P	C_RxFG-11_P	100
72	TxFG-11_N	C_RxFG-11_N	99
73	GND	GND	98
74	TxFD-12_P	C_RxFD-12_P	97
75	TxFD-12_N	C_RxFD-12_N	96
76	GND	GND	95
77	TxFE-12_P	C_RxFE-12_P	94
78	TxFE-12_N	C_RxFE-12_N	93
79	GND	GND	92
80	TxFF-12_P	C_RxFF-12_P	91
81	TxFF-12_N	C_RxFF-12_N	90
82	GND	GND	89
83	TxFG-12_P	C_RxFG-12_P	88
84	TxFG-12_N	C_RxFG-12_N	87
85	GND	GND	86

5.2.7. S3: Connector to 1st/2nd PCB

Via S3, the **NAT-MCH-40G-XAUI** connects to the **NAT-MCH-Base** / **NAT-MCH-CLK** module.

Figure 19 – S3: Connector to 1st/2nd PCB

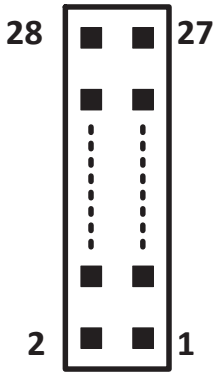


Table 9 – S3: Connector to 1st/2nd PCB – Pin Assignment

Pin #	Signal	Signal	Pin #
1	nc	nc	2
3	GND	GND	4
5	BASE_TA_N	C_BASE_RA_N	6
7	BASE_TA_P	C_BASE_RA_P	8
9	+12V	+12V	10
11	+12V	+12V	12
13	PCIeCLK_HUB_P	+3.3V_MP	14
15	PCIeCLK_HUB_N	SPICLK	16
17	GND	nc	18
19	MOSI	MISO	20
21	GND	/SPISEL_HUBPCB	22
23	SCL	nc	24
25	SDA	nRESET_HUBPCB	26
27	GND	GND	28

5.2.8. S4: MicroSD-Card Slot

S4 is a MicroSD-Card slot on the **NAT-MCH-40G-XAUI**.

Figure 20 – S4: MicroSD-Card Slot

Table 10 – S4: MicroSD-Card Slot – Pin Assignment

Pin #	Signal	Signal	Pin #
1	eMMC_D2_b	eMMC_D3_b	2
3	eMMC_CMD_b	3V3	4
5	eMMC_CLK_b	GND	6
7	eMMC_D0_b	eMMC_D1_b	8

5.2.9. SW1: General Settings

The function of DIP SW1 is tbd.

Figure 21 – SW1: General Settings

Table 11 – SW1 – Operating Parameters

Switch #	Function
SW1-1	***tbd***
SW1-2	***tbd***
SW1-3	***tbd***
SW1-4	***tbd***
SW1-5	***tbd***
SW1-6	***tbd***

Note:

Default configuration is labelled with ***bold, italic letters***.

5.3. Port Assignment

The Ethernet switch on the **NAT-MCH-40G-XAUI** features up to 72 SerDes lanes, which – depending on the operating mode – are merged to ports. The following table gives a selection of port merging and assignment to the external interfaces and the port extenders (PIPE) in reference to the operating modes used on the **NAT-MCH-40G-XAUI**.

Table 12 – Ethernet Switch Port Assignment

SerDes Lane #	max. SerDes Lane Speed	x1 Port #	x2 Port #	x4 Port #	Interface
0	25G	0	0	0	Optical Uplink #0
1		1			Optical Uplink #1
2		2	2		Optical Uplink #2
3		3			Optical Uplink #3
4		4	4	4	Optical Uplink #4
5		5			Optical Uplink #5
6		6	6		Optical Uplink #6
7		7			Optical Uplink #7
8				8	PIPE #4 Lanes 12-15
9					
10					
11					
12				12	PIPE #3 Lanes 12-15
13					
14					
15					
16				16	PIPE #1 Lanes 12-15
17					
18					
19					
20				20	PIPE #2 Lanes 12-15
21					
22					
23					
24	12.5G	24	24	24	Update 2nd MCH – Fabric D
25		25			Update 2nd MCH – Fabric E
26		26	26		Update 2nd MCH – Fabric F
27		27			Update 2nd MCH – Fabric G
28		28			NAT-MCH-BASE GbE-Switch 1000Base-X
65		65			Local CPU 1000Base-X
68		68	68	68	Optical Uplink #11
69		69			Optical Uplink #10 RX / #9 TX
70		70	70		Optical Uplink #8 RX 7/ #10 TX
71		71			Optical Uplink #9 RX / #8 TX

Port assignments of the PIPEs are given in the following tables:

Table 13 – Port Extender #1 – Port Assignment

SerDes Lane #	x1 Port #	x2 Port #	x4 Port #	Interface
0	0	0	0	AMC#3 – Fabric G
1	1			AMC#3 – Fabric F
2	2	2		AMC#3 – Fabric E
3	3			AMC#3 – Fabric D
4	4	4	4	AMC#2 – Fabric G
5	5			AMC#2 – Fabric F
6	6	6		AMC#2 – Fabric E
7	7			AMC#2– Fabric D
8	8	8	8	AMC#1 – Fabric G
9	9			AMC#1 – Fabric F
10	10	10		AMC#1 – Fabric E
11	11			AMC#1– Fabric D
12	12	12	12	Switch SerDes Lane 16
13	13			Switch SerDes Lane 17
14	14	14		Switch SerDes Lane 18
15	15			Switch SerDes Lane 19

Table 14 – Port Extender #2 – Port Assignment

SerDes Lane #	x1 Port #	x2 Port #	x4 Port #	Interface
0	0	0	0	AMC#6 – Fabric G
1	1			AMC#6 – Fabric F
2	2	2		AMC#6 – Fabric E
3	3			AMC#6 – Fabric D
4	4	4	4	AMC#5 – Fabric G
5	5			AMC#5 – Fabric F
6	6	6		AMC#5 – Fabric E
7	7			AMC#5– Fabric D
8	8	8	8	AMC#4 – Fabric G
9	9			AMC#4 – Fabric F
10	10	10		AMC#4 – Fabric E
11	11			AMC#4– Fabric D
12	12	12	12	Switch SerDes Lane 20
13	13			Switch SerDes Lane 21
14	14	14		Switch SerDes Lane 22
15	15			Switch SerDes Lane 23

Table 15 – Port Extender #3 – Port Assignment

SerDes Lane #	x1 Port #	x2 Port #	x4 Port #	Interface
0	0	0	0	AMC#7 – Fabric D
1	1			AMC#7 – Fabric E
2	2	2		AMC#7 – Fabric F
3	3			AMC#7 – Fabric G
4	4	4	4	AMC#8 – Fabric D
5	5			AMC#8 – Fabric E
6	6	6		AMC#8 – Fabric F
7	7			AMC#8 – Fabric G
8	8	8	8	AMC#9 – Fabric D
9	9			AMC#9 – Fabric E
10	10	10		AMC#9 – Fabric F
11	11			AMC#9 – Fabric G
12	12	12	12	Switch SerDes Lane 12
13	13			Switch SerDes Lane 13
14	14	14		Switch SerDes Lane 14
15	15			Switch SerDes Lane 15

Table 16 – Port Extender #4 – Port Assignment

SerDes Lane #	x1 Port #	x2 Port #	x4 Port #	Interface
0	0	0	0	AMC#10 – Fabric D
1	1			AMC#10 – Fabric E
2	2	2		AMC#10 – Fabric F
3	3			AMC#10 – Fabric G
4	4	4	4	AMC#11 – Fabric D
5	5			AMC#11 – Fabric E
6	6	6		AMC#11 – Fabric F
7	7			AMC#11 – Fabric G
8	8	8	8	AMC#12 – Fabric D
9	9			AMC#12 – Fabric E
10	10	10		AMC#12 – Fabric F
11	11			AMC#12 – Fabric G
12	12	12	12	Switch SerDes Lane 8
13	13			Switch SerDes Lane 9
14	14	14		Switch SerDes Lane 10
15	15			Switch SerDes Lane 11

SerDes modes supported by the Ethernet switch are listed below.

Table 17 – Ethernet Switch SerDes Modes

Port Speed (Gbps)	Port Mode	Standard Electrical Interface	# of Lanes	SerDes Speed (GHz)	Connected to	AN Standard	FEC
107	107GBASE-KR4	Marvell Proprietary version of 100GBASE-KR4 that supports 100 GbE packet rate and compensates for the overhead proprietary forwarding headers	4	27.5	• Backplane	Marvell Proprietary N/A	• No FEC • RS-FEC

100	CAUI-4	IEEE 802.3bm	4	25.78125	• Chip-to-Chip
					• Chip-to-Module
					• Based on Transceiver:
					  • 100GBASE-SR4
					  • 100GBASE-LR4
					  • 100GBASE-ER4
					  • 100GBASE-CWDM4
					  • 100GBASE-PSM
						N/A	• No FEC
							• RS-FEC

	100GBASE-R4	100GBASE-CR4 IEEE 802.3bj clause 92 with or without RS-FEC			• Cable Direct Attach (copper)	IEEE 802.3ap	• No FEC • RS-FEC
		100GBASE-KR4 IEEE 802.3bj clause 93 with or without RS-FEC			• Backplane	IEEE 802.3ap	• No FEC • RS-FEC
	QSFP28G	SFF-8679 with the electrical interface compliant with 100GBASE-KR4 (IEEE 802.3bj clause 93) and CEI-28G-VSR (OIF CEI 3.1)			• Backplane	IEEE 802.3ap	• No FEC • RS-FEC

Port Speed (Gbps)	Port Mode	Standard Electrical Interface	# of Lanes	SerDes Speed (GHz)	Connected to	AN Standard	FEC
50	LAUI-2	IEEE 802.3bm	2	25.78125	• Backplane	N/A	• No FEC • RS-FEC
	50GBASE-R2	50GBASE-CR2 IEEE 802.3by			• Cable Direct Attach (copper)	Consortium	• No FEC • RS-FEC
		50GBASE-KR2 IEEE 802.3by			• Backplane	Consortium	• No FEC • RS-FEC
50	50GBASE-KR4	Marvell proprietary	4	12.890625	• Backplane • Cable Direct Attach (copper)	Marvell Proprietary N/A	• No FEC • FC FEC

40	40GBASE-R4	XLAUI
		IEEE 802.3ba Annex 83A
			4	10.3125	• Chip-to-Chip
					• QSFP+ Optic Transceiver:
					  • SR4
					  • LR4
						N/A	• No FEC
							• FC FEC

		XLPPI
		IEEE 802.3ba Annex 86A
					QSFP+ Optic Transceiver:
					  • SR4
					  • LR4
						N/A	• No FEC
							• FC FEC

		40GBASE-CR4 IEEE 802.3ba Annex 85A			• Cable Direct Attach (copper)	IEEE 802.3ap	• No FEC • FC FEC
		40GBASE-KR4 IEEE 802.3ba Annex 84			• Backplane	IEEE 802.3ap	• No FEC • FC FEC
40	40GBASE-KR2	40GBASE-KR2	2	20.625	• Backplane	Marvell Proprietary N/A	• No FEC • FC FEC

Port Speed (Gbps)	Port Mode	Standard Electrical Interface	# of Lanes	SerDes Speed (GHz)	Connected to	AN Standard	FEC
25	25GBASE-R	25GBASE-CR 25GBASE-CRS IEEE802.3by	1	25.78125	• Cable Direct Attach (copper)	IEEE 802.3ap	• No FEC • RS-FEC • FC FEC
		25GBASE-KR IEEE802.3by			• Backplane	IEEE 802.3ap	• No FEC • RS-FEC • FC FEC
12.5	12.5GBASE-KR	Marvell proprietary	1	12.890625	• Backplane • Cable Direct Attach (copper)	Marvell Proprietary N/A	• No FEC • FC FEC
11.8	12GBASE-KR	Marvell Proprietary version of 10GBASE-KR that supports 10 GbE packet rate and compensates for the overhead proprietary forwarding headers Supports XHGS	1	12.1875	• Backplane • Cable Direct Attach (copper)	Marvell Proprietary N/A	• No FEC • FC FEC

10	10GBASE-R	SFI
		SFF-8431 Rev 4.1
			1	10.3125	• SFP+ Optic Transceiver
					  • SR
					  • LR
					  • ER
						N/A	• No FEC
							• FC FEC

		XFI SFF INF-8077i IEEE.Std-802.3ae			• XFP Optic Transceiver	N/A	• No FEC • FC FEC
		10GBASE-CR Marvell proprietary			• Cable Direct Attach (copper)	Marvell Proprietary N/A	• No FEC • FC FEC
		10GBASE-KR IEEE 802.3ap clause 49			• Backplane	IEEE 802.3ap	• No FEC • FC FEC
5	5GBASE-KR	5GBASE-KR	1	5.1562	• Backplane • Cable Direct Attach (copper)	IEEE 802.3ap	• No FEC • FC FEC
2.5	2500BASE-KX	IEEE P802.3cb 2.5Gb/s and 5Gb/s Backplane	1	3.125	• Long Reach Interconnect	IEEE 802.3ap	• No FEC

Port Speed (Gbps)	Port Mode	Standard Electrical Interface	# of Lanes	SerDes Speed (GHz)	Connected to	AN Standard	FEC
		and Copper Cables Task Force					
1	10/100/1000	1000BASE-KX IEEE 802.3ap	1	1.25	• Backplane	IEEE 802.3ap	• No FEC

SerDes modes supported by the PIPEs are listed below.

Table 18 – PIPE SerDes Modes

Port Speed (Gbps)	Port Mode	Standard Electrical Interface	# of Lanes	SerDes Speed (GHz)	Connected to
107	107GBASE-KR4	With or without RS-FEC Marvell proprietary version of 100GBASE-KR4 that supports 100 GbE packet rate and compensates for the overhead proprietary forwarding headers	4	27.5	• Backplane
100	100GBASE-R4	100GBASE-CR4 IEEE 802.3bj clause 92 with or without RS-FEC	4	25.78125	• Cable Direct Attach (copper)
		100GBASE-KR4 IEEE 802.3bj clause 93 with or without RS-FEC			• Backplane
53	53GBASE-KR2	With or without RS-FEC Marvell proprietary version of 55GBASE-KR2 that supports 50 GbE packet rate and compensates for the overhead proprietary forwarding headers	2	27.5	• Backplane

Port Speed (Gbps)	Port Mode	Standard Electrical Interface	# of Lanes	SerDes Speed (GHz)	Connected to
50	50GBASE-KR2	Marvell proprietary 50GBASE-KR2 with or without RS-FEC IEEE 802.3by	2	25.78125	• Backplane
50	50GBASE-KR4	Marvell proprietary	4	12.890625	• Backplane • Cable Direct Attach (copper)
40	40GBASE-KR2	Proprietary 40GBASE-KR2	2	20.625	• Backplane

40	40GBASE-R4	XLAUI
		40GBASE-SR4
		40GBASE-LR4
		IEEE 802.3ba Annex 83A
			4	10.3125	• Chip-to-Chip
					• QSFP+ Optic Transceiver:
					  • SR4
					  • LR4

		XLPPI IEEE 802.3ba Annex 86A			QSFP+ Optic Transceiver: • SR4 • LR4
		40GBASE-CR4 IEEE 802.3ba Annex 85A			• Cable Direct Attach (copper)
		40GBASE-KR4 IEEE 802.3ba Annex 84			• Backplane
26.6	26.6GBASE-KR	With or without RS-FEC Marvell proprietary version of 27.5GBASE-KR that supports 25 GbE packet rate and compensates for the overhead proprietary forwarding headers	1	27.5	• Backplane
25	25GBASE-KR	With or without proprietary RS-FEC or Fire Code (clause 74)	1	25.78125	• Cable Direct Attach (copper) • Backplane
12.5	12.5GBASE-KR	Marvell proprietary	1	12.1875	• Backplane • Cable Direct Attach (copper)
11.8	12GBASE-KR	Marvell proprietary version of 10GBASE-KR that supports 10 GbE packet rate and compensates for the overhead proprietary forwarding headers Supports XHGS	1	12.1875	• Backplane • Cable Direct Attach (copper)

Port Speed (Gbps)	Port Mode	Standard Electrical Interface	# of Lanes	SerDes Speed (GHz)	Connected to
10	10GBASE-R	10GBASE-SR SFF-8431 Rev 4.1 SFI	1	10.3125	External optical module, connected via SFF-8431 Rev 4.1 Chip-to-Module
		10GBASE-LR			
		10GBASE-ER			
		SFF INF-8077i XFI IEEE.Std-802.3ae			• XFP Optic Transceiver
		10GBASE-CR Marvell proprietary			• Cable Direct Attach (copper)
		10GBASE-KR IEEE 802.3ap clause 49			• Backplane
10	10GBASE-X2	RXAUI Marvel proprietary	2	6.25	• Short Reach Interconnect
		RXAUI-LR Marvel proprietary			• Long Reach Interconnect
10	10GBASE-X4	XAUI IEEE 802.3 Section 47	4	3.125	• XAUI PHY
		10GBASE-KX4			• Backplane
		10GBASE-CX4			• Cable Direct Attach (copper)
5	5GBASE-KR	IEEE P802.3cb 2.5Gb/s and 5Gb/s Backplane and Copper Cables Task Force	1	5.1562	• Backplane • Chip-to-Module
2.5	2500BASE-KX	IEEE P802.3cb 2.5Gb/s and 5Gb/s Backplane and Copper Cables Task Force	1	3.125	• Long Reach Interconnect
1	10/100/1000	1000BASE-KX IEEE 802.3ap	1	1.25	• Backplane

6. FIRMWARE UPDATE

6.1. How to update the 40G Firmware

The update process depends on what is being updated. Usually only the **NAT-MCH** Base firmware has to be updated. But it is also possible that the 40G module itself needs to be updated.

6.2. Updating MCH-Base

The **NAT-MCH** Base firmware is updated as usual, either via web interface or CLI. Please refer to the corresponding section of the **NAT-MCH** User's Manual (https://www.nateurope.com/manuals/nat_mch_man_usr.pdf).

6.3. Updating the MCH-40G module

1. Make sure the 40G module is accessible via Ethernet. For that your network interface needs to be configured to have an IP address belonging to the 192.168.1.0/24 network. You can check accessibility of the 40G module by pinging it, i.e.

   ping 192.168.1.200

2. Copy Image-initramfs-nat40g.bin (containing the kernel and initramdisk), flash-image.bin (containing the bootloader), and nat40g.dtb (device tree) onto the 40G module and make sure the new files are synced to the boot partition:

   ssh-keygen -R 192.168.1.200

   scp Image-initramfs-nat40g.bin flash-image.bin nat40g.dtb root@192.168.1.200:/mnt/boot/

   ssh root@192.168.1.200 "flashcp -v /mnt/boot/flash-image.bin /dev/mtd0 && sync && echo sync done"

3. Wait for *sync done* to appear on your console. Only by then the update has successfully finished.

7. SPECIFICATIONS AND COMPLIANCES

7.1. Internal Reference Documentation

- **NAT-MCH** User's Manual:
  https://www.nateurope.com/manuals/nat_mch_man_usr.pdf
- **NAT-MCH-BASE6 /-BASE12:**
  https://www.nateurope.com/manuals/nat_mch_base_v3x_man_hw.pdf
- **NAT-MCH-PHYS/PHYS80:**
  please contact N.A.T.
- **NAT-MCH-CLK:**
  https://www.nateurope.com/manuals/nat_mch_clk_v4x_man_hw.pdf
- **NAT-MCH-CLK-PHYS**:
  https://www.nateurope.com/manuals/nat_mch_clk_phys_man_hw.pdf

7.2. External Reference Documentation

- Atmel ATmega128 Microcontroller Data Sheet, Rev. 2467X–AVR–06/11, 06/2011
- Lattice MACHXO2 FPGA Family Data Sheet, DS1035 V3.3, 03/2017
- Marvell 88F3720 CPU Product Brief, Marvell_88F37xx_PB, 08/2016
- Marvell 98PX1012 Port Extender Product Brief, 03/2017
- Marvell 98EX5520 Ethernet Switch Product Brief, Marvell_88EX55xx_PB, 07/2013
- Finisar FBOTD10SL1L00 BOA Transceiver Product Guide, 03/2017

7.3. Cable Recommendations

- https://fibertronics.com/1m-mtp-male-to-24-lc-upc-24-fiber-multimode-om3-50125-breakout-cable
- https://www.sylex.sk/product/mtp-cxp-mtp-qsfp-kabel/
- https://www.fs.com/de/products/69995.html
- https://www.fs.com/de/products/57024.html
- https://www.fs.com/de-en/products/61898.html

7.4. Standards Compliance

- PICMG AMC.0 Rev. 2.0
- PICMG AMC.1 Rev. 1.0
- IPMI Specification v1.5 Rev. 1.0
- PICMG HPM.1

7.5. Compliance to RoHS Directive

Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) predicts that all electrical and electronic equipment being put on the European market after June 30th, 2006 must contain lead, mercury, hexavalent chromium, poly-brominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) and cadmium in maximum concentration values of 0.1% respective 0.01% by weight in homogenous materials only.

As these hazardous substances are currently used with semiconductors, plastics (i.e. semi-conductor packages, connectors) and soldering tin any hardware product is affected by the RoHS directive if it does not belong to one of the groups of products exempted from the RoHS directive.

Although many of hardware products of N.A.T. are exempted from the RoHS directive it is a declared policy of N.A.T. to provide all products fully compliant to the RoHS directive as soon as possible. For this purpose since January 31st, 2005 N.A.T. is requesting RoHS compliant deliveries from its suppliers. Special attention and care has been paid to the production cycle, so that wherever and whenever possible RoHS components are used with N.A.T. hardware products already.

7.6. Compliance to WEEE Directive

Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) predicts that every manufacturer of electrical and electronical equipment which is put on the European market has to contribute to the reuse, recycling and other forms of recovery of such waste so as to reduce disposal. Moreover this directive refers to the Directive 2002/95/EC of the European Commission on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

Having its main focus on private persons and households using such electrical and electronic equipment the directive also affects business-to-business relationships. The directive is quite restrictive on how such waste of private persons and households has to be handled by the supplier/manufacturer; however, it allows a greater flexibility in business-to-business relation-ships. This pays tribute to the fact with industrial use electrical and electronical products are commonly integrated into larger and more complex environments or systems that cannot easily be split up again when it comes to their disposal at the end of their life cycles.

As N.A.T. products are solely sold to industrial customers, by special arrangement at time of purchase the customer agreed to take the responsibility for a WEEE compliant disposal of the used N.A.T. product. Moreover, all N.A.T. products are marked according to the directive with a crossed out bin to indicate that these products within the European Community must not be disposed with regular waste.

If you have any questions on the policy of N.A.T. regarding the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the "Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) or the Directive 2002/95/EC of the European Commission on "Waste Electrical and Electronic Equipment" (WEEE) please contact N.A.T. by phone or e-mail.

7.7. Compliance to CE Directive

Compliance to the CE directive is declared. A 'CE' sign can be found on the PCB.

7.8. Product Safety

The board complies with EN60950 and UL1950.

7.9. Compliance to REACH

The REACH EU regulation (Regulation (EC) No 1907/2006) is known to N.A.T. GmbH. N.A.T. did not receive information from their European suppliers of substances of very high concern of the ECHA candidate list. Article 7(2) of REACH is notable as no substances are intentionally being released by NAT products and as no hazardous substances are contained. Information remains in effect or will be otherwise stated immediately to our customers.

7.10. Abbreviation List

Table 19 – Abbreviation List

Abbreviation	Description
AMC	Advanced Mezzanine Card
ARM	Processor Architecture with reduced instruction set
BOA	Board-Mount Optical Assembly
CPU	Central Processing Unit
DDR4 DRAM	Double Data Rate Dynamic RAM
eMMC	Embedded Multimedia Card
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
I^2C	Inter-Integrated Circuit
IPMI	Intelligent Platform Management Interface
µC	Microcontroller
µTCA/MTCA/MicroTCA	Micro Telecommunications Computing Architecture
MDIO	Management Data Input/Output
MicroSD Card	Micro Secure Digital Memory Card
MCH	µTCA/MTCA Carrier Hub
MII	Media Independent Interface
MPO	Multiple-Fiber Push-On/Pull-off - Optical Fiber Connector
PCB	Printed Circuit Board
PCI(e)	Peripheral Component Interconnect (Express)
PIPE	Passive Intelligent Port Extenders
RAM	Random Access Memory
SerDes	Serializer/Deserializer
UART	Universal Asynchronous Receiver/Transmitter
XAUI	10 GbE (via 4x 3.125 GB/s)

8. DOCUMENT'S HISTORY

Table 20 – Document's History

Rev	Date	Description	Author
1.0	27.05.2020	• Initial release	se
	15.09.2020	• Minor changes	se
1.1	22.09.2020	• Added chapter 5.2.1 Optical Uplink Connector • Added chapter 7.3 Cable Recommendations	se
1.2	25.02.2021	• Minor changes • Updated chapter 5.3 Port Assignment	se
	18.08.2021	• Updated chapter 4.4 Optical Transceiver (optional) • Updated Figure 10 – NAT-MCH-40G-XAUI: Front Panel – Base12 (Preliminary) • Updated chapter 5.2.1 Optical Uplink Connector • Updated chapter 7.3 Cable Recommendations	se
1.3	7.09.2021	• Minor changes and typo correction • Updated Table 1 – Technical Data • Updated chapter 4.4 Optical Transceiver (optional) • Updated chapter 5.2.1 Optical Uplink Connector • Added chapter 6 Firmware Update	se