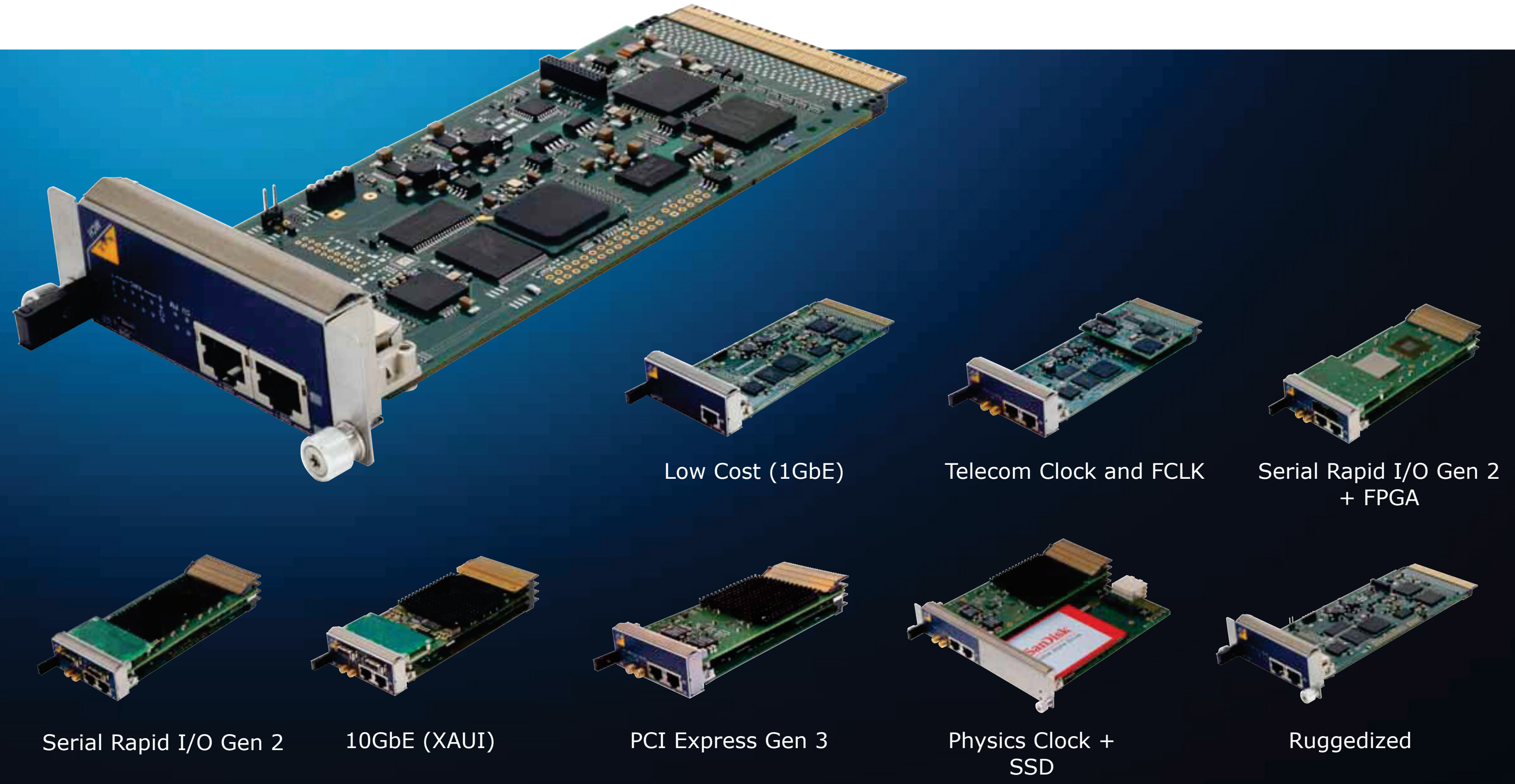
NAT-MCH

N.A.T. MicroTCA Carrier Hub NAT-MCH



Overview

The N.A.T. MicroTCA Carrier Hub **NAT-MCH** is the central management and data switching engine for all MicroTCA systems. The **NAT-MCH** is designed to provide any functionality as defined by the MicroTCA specifications MTCA.0, MTCA.1, MTCA.2, MTCA.3 and MTCA.4, serving up to the maximum of 13 Advanced Mezzanine Cards (AMCs), 1-4 Power Modules and two Cooling Units. Because of its scalable and flexible design the **NAT-MCH** can be used in any kind of MicroTCA system, supporting telecom and non-telecom environments as well as redundant and non-redundant architectures. The mandatory carrier manager is implemented in the on-board Freescale ColdFire CPU. For MicroTCA systems operating in a detached or stand-alone mode, a shelf manager as well as a system manager are provided. Alongside the processor, the MCH base module incorporates a managed, non-blocking and low-latency Gigabit Ethernet L2 switch for base channel connectivity.

Following the building block model (next page) the **NAT-MCH** can be individually configured to meet exact system requirements. Comprehensive software support like a Java based GUI interfacing to the Open HPI compliant top level API of the **NAT-MCH** completes the product.

Fabric Switch Module Options

· PCI-Express (PCIe Gen 3)
· Serial Rapid IO (SRIO Gen 2)
· 10 Gigabit Ethernet (XAUI)

Clock Distribution Options

· Telecom Mezzanine
· Physics Mezzanine

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Product Configurations

NAT-MCH

Overview and Purpose

The **NAT-MCH** is a MicroTCA (uTCA®/MTCA) Carrier Hub in the form factor of a single or double width and mid- or full-size Advanced Mezzanine Card (AMC). It provides the central management and data switching for all MicroTCA systems. The **NAT-MCH** comprises a base module and numerous optional daughter cards which can be mounted on the base module.

The **NAT-MCH** is MTCA.0, MTCA.1, MTCA.2, MTCA.3 and MTCA.4 compliant and delivers switching and hub functionality for the various system fabrics as defined in the AMC.x standard series, i.e. 1Gigabit Ethernet (GbE), PCI-Express (PCIe Gen 3), Serial Rapid I/O (SRIO Gen 2), 10Gigabit Ethernet (XAUI) or custom protocols based on Xilinx Kintex-7 FPGA. The **NAT-MCH** can also provide a centralized clock distribution to all AMCs in the system.

CPU, memory and O/S

The **NAT-MCH** base board is equipped with a CPU from the Freescale ColdFire processor family. The CPU operates at a core frequency of 266 MHz. The **NAT-MCH** provides 32/64MB SDRAM and 16/32/64MB FLASH memory. The **NAT-MCH** operates on the field proven real-time kernel OK1 developed by N.A.T..

Gigabit Ethernet Switch and 10GbE (XAUI) Support

The Gigabit Ethernet Switches incorporated in the **NAT-MCH** both provide layer 2, non-blocking, low-latency switching, supporting VLAN as well as a port based rate control. The **NAT-MCH** supports Fabric A (1GbE) and Fabrics D-G (10GbE XAUI) according to MTCA.0, MTCA.1 and MTCA.4 and PICMG SFP.1 R1.0, serving up to 13 AMCs as well as the update channel from the second MCH in redundant environments. Also supported are uplink ports at the front panel of the **NAT-MCH** in order to interconnect to other carriers, shelves or systems.

PCI Express Gen 3 Switch

The PCI Express Switching option allows PCIe Gen 3 connectivity for up to 12 AMCs at PCIe rates from x1 to x4. The PCIe chipsets provide a Quality of Service (QoS) module and are configurable in terms of a non-transparent port for multi-host support. The PCIe option can optionally provide a Spread Spectrum Clock (100MHz mean) or a fixed 100MHz clock. The clock can be provided compliant to HCSL or MLVDS signalling levels. The PCIe hub provides clustering support for 6 independent clusters with one configurable non-transparent upstream port. Each cluster offers its own transparent upstream port.

SRIO Gen 2 Switch

Alternatively the **NAT-MCH** can be equipped with a Serial Rapid I/O (SRIO Gen 2) daughter board to support uncontended low latency point-to-point connectivity between up to 12 AMC pipes. The SRIO hub supports x1 and x4 fat pipes. A mixture of AMC modules with SRIO Gen 1 & Gen 2 is supported.

Custom Protocol Switch (based on Xilinx Kintex-7 FPGA)

The **NAT-MCH-FPGA** combines the fast and low latency SRIO Gen II switching with a fully-customizable Kintex-7 FPGA. The special FPGA hub module is intended to be used for switching or multiplexing CPRI (Common Public Radio Interface), OBSAI (Open Base Station Architecture Initiative), standard (e.g. SRIO, XAUI) or any customized serial protocols. Additionally, this hub module provides two high speed optical uplinks via SFP+ receptacles. Beside the high speed serial connections, the Kintex-7 FPGA has access to two independent DDR3 memories (up to 4Gbit each), a low jitter PLL

Technical Data

CPU and memory

- Freescale ColdFire MCF54452 CPU @ 266MHz
- DDR2 RAM: 32/64MB
- FLASH: 16/32/64MB

IPMI and Compliance

- 13 AMCs
- 2 cooling units
- 1-4 power modules
- PICMG AMC.0
- PICMG 2.9
- update to 2nd MCH

Operating System and API

- O/S: OK1
- API: HPI compliant

Supported Fabrics and Compliance

Fabric A: Gigabit Ethernet
- 13 AMCs
- PICMG AMC.2
- PICMG SFP.1

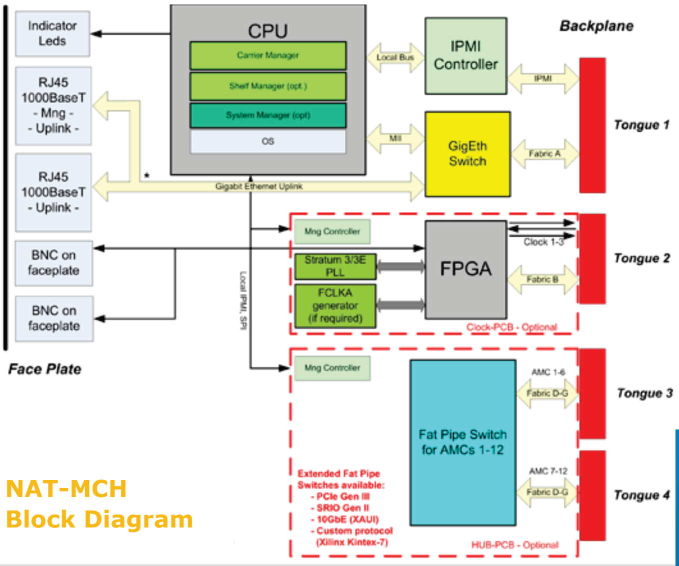
Fabric D-G:
- Serial Rapid IO Gen 2, x1 or x4 (PICMG AMC.4)
- PCI Express Gen 3, x1 or x4 (PICMG AMC.1)
- 10GbE (XAUI) (PICMG AMC.2)
- customized serial protocol (Xilinx Kintex-7 FPGA)
- 12 AMCs

Clock Distribution

- Telecom: Stratum 3/3E PLL with reference from either 1 of the 12 AMCs or external clock via front panel or free running
- PCIe: Spread Spectrum Clock (100MHz mean) or oscillator (100MHz fixed), HCSL or MLVDS signalling
- low latency and low jitter

Indicator LEDs

- 3 standard AMC LEDs
- 12 bi-colour LEDs for AMC slot stati
- 2 bi-colour LEDs for cooling units
- 2 bi-colour LEDs for power modules



NAT-MCH Block Diagram

and a Gigabit Ethernet connection to the MCH base module switch. This allows implementing complex user functionality and therefore can save a full AMC slot.

Clock Distribution

Besides the PCIe clock the **NAT-MCH** also offers a sophisticated clock distribution module for special requirements, such as communication applications. Thus the module allows a flexible selection of telecom and non-telecom clocking structures as defined in MTCA.0. The on-board Stratum 3/3E type PLL sources its clock reference from any of the 12 AMCs or from an external clock, via the front panel BNC type connector. With respect to the PCIe clock, the **NAT-MCH** supports both signal levels, HCSL (as required by PCI-SIG) and MLVDS (as requested by the MTCA.0 specification). Additionally, N.A.T. offers the Clock Mezzanine for Physics for applications requiring low jitter and constant latency.

Management

The **NAT-MCH** incorporates a MicroTCA Carrier Management Controller (MCMC) which supports the management for up to 13 AMCs, 2 cooling units and 1-4 power modules. The support of a 13th AMC requires a redundant system where the redundant MCH slot is used by this AMC. Special care has been taken to support numerous aspects of system architectures, i.e. E-Keying, redundancy, load sharing, clocking, fail-over scenarios or system integrity. External system or shelf managers can connect to the **NAT-MCH** through any of the Ethernet front panel ports. For remote control and visualization on N.A.T. has its JAVA based application NATview. Like any other remote management tool (i.e. ipmitool (open source) or any tool based on the HPI recommendation of the Service Availability Form (SAF)) NATview accesses the **NAT-MCH** via the Remote Management Control Protocol (RMCP) as required by the MTCA.0 specification.

Configuration

The **NAT-MCH** can be comfortably configured using the included web interface with any standard web browser or by the command line interface via serial connection (USB) or a Telnet connection.

Carrier Manager

- management of up to 13 AMCs, 2 cooling units and 1-4 power modules
- supports redundant architectures
- supports fail-over procedure

Shelf and System Manager

- on-board
- for detached or stand-alone operation
- hook-in for external managers via 1GbE port at front panel or backplane GbE

Front Panel Connectors

- 1GbE management connection
- 1GbE system up-link for Fabric A
- external clock reference (bi-directional)
- serial debug connector (USB)
- Fat Pipe uplink for Fabric D-G

NATview
Visualization tool for any MicroTCA system

Overview

NATview allows the user to view and manipulate the components of the MicroTCA system in a graphical way. NATView runs on Oracle JAVA 1.6. It has been successfully tested on Windows, Linux, and MacOS X.

System Overview

- Tree structured sensor data including fans and temperatures
- MCH Scanner – find your MCH in your network!
- New toolbar for easier access

Events and Alarms

- intelligent alarm monitoring
- SEL access
- Various events filters

Sensors

- Display the current sensor values and thresholds
- Value history
- Auto updaters

FRU Information

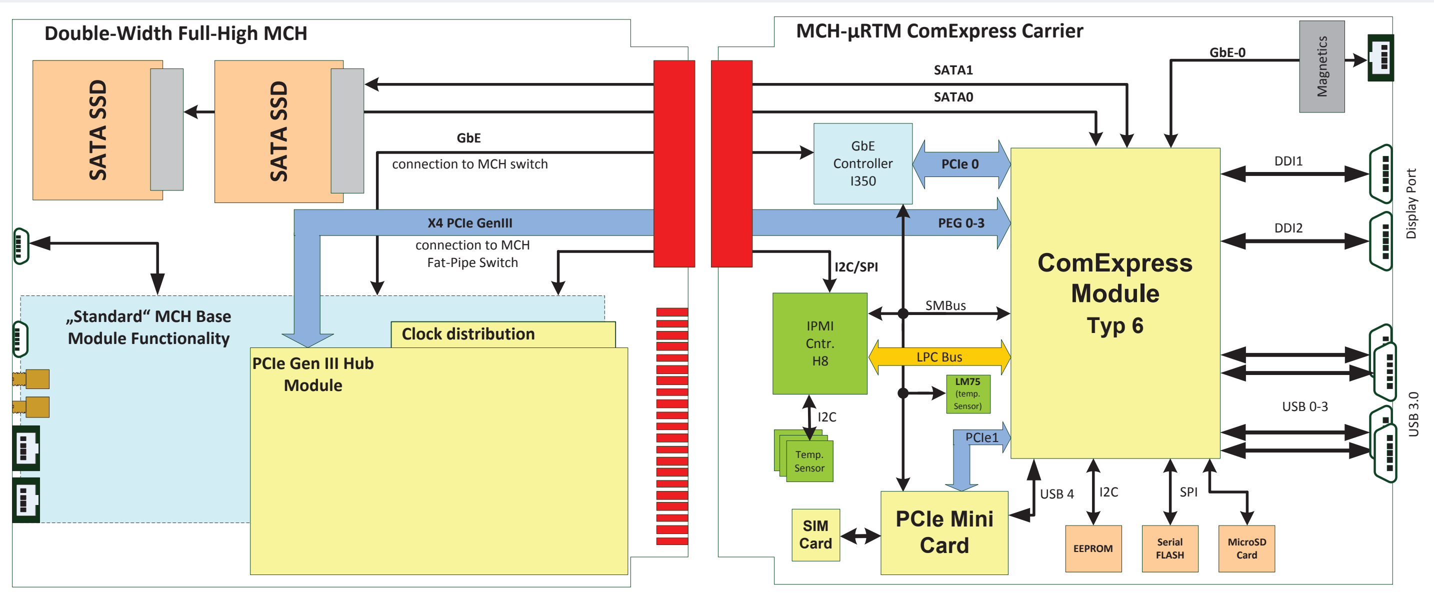
- FRU Editor
- Backplane Connection Viewer
- Collect system information with a single mouse click.
- Easily add your own components

System Manager

Technical Data

NAT-MCH

Physics Clock + SSD



The new double-width MCH can be utilized as standalone product in all systems requiring the double-width form factor. It is ideally suited for MTCA.4 applications allowing the use of MicroTCA rear transition modules (µRTM). Combining this MCH with the µRTM COM Express Carrier, allows working with the idle space behind the MCH. The COM Express carrier can be equipped with any type 6 Computer on the module (COM) Express module fitting best to the system requirements.

The benefit of using COM Express modules is the broad range of configurations (processor architecture, performance, memory, etc.), a rich offering by various manufactures, long-term availability and system configuration flexibility.

Key Features MCH:

- NAT-MCH in double-width, full-size
- with standard CLK and Hub Module (PCIe Gen 3)
- RS232 and USB for MCH serial console
- optional: 2x SATA Flash Drives (SSD), accessible by COM Express Module
- support of µRTM COM Express Carrier for standard COM Express Module Type 6
- direct access to Fat Pipe via PCIe Gen 3 Switch on MCH Hub Module for µRTM
- access to backplane Ethernet via MCH-Switch and on-board GbE Controller for µRTM

Key Features µRTM COM Express:

access to interfaces provided by MCH (via RTM connector)

- 2x SATA devices
- x4 PCIe Gen3 connection between MCH switch and COM Express PEG 0-3 interface
- access to MCH Ethernet Switch via on board Ethernet controller, using COM Express PCIe 0 interface

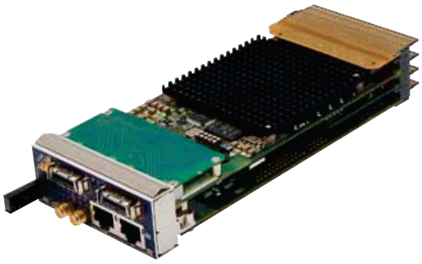
front panel interfaces

- Gigabit Ethernet (COM Express GbE-0 interface)
- 2x Display port
- 4x USB 3.0

PCIe Mini card support (including SIM) for wireless applications

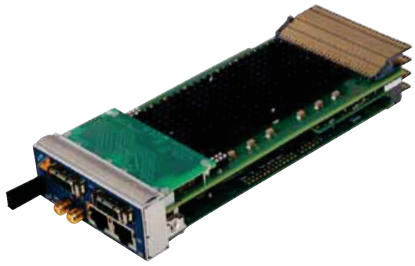
- MicroSD card support
- IPMI controller

Technical Data
NAT-MCH

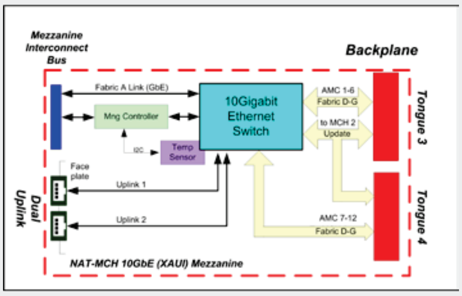


10GbE (XAUI)

PCI Express Gen 3



Serial Rapid I/O Gen 2



10GbE (XAUI) Switch

The **NAT-MCH 10GbE Hub Mezzanine** provides high performance, low latency and robust Ethernet packet switching service for MTCA systems.

Key Features:

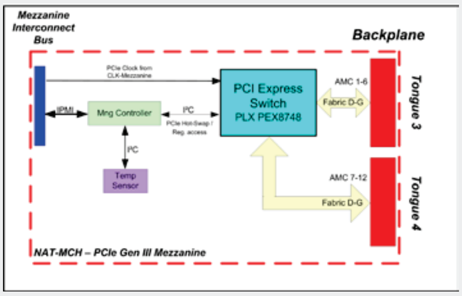
- **10GbE Ethernet** port for 12 AMC slots
- 2 uplink ports on front panel

Layer 2 Bridging Features:

- VLAN priority (802.1Q, P)
- link aggregation (802.3aad)
- duplex flow control (802.3x)
- user defined monitoring and filter rules
- Jumbo Frame Support
- 240 Gbps bandwidth
- per AMC slot selection of:
  - XAUI (10GbE)
  - 2.5 GbE
  - 1 Gb
- 2 uplink ports on front panel:
  - 10 GBase-CX4 (copper)
  - SFP+ (optical)

Security:

- MAC address security port access control (802.1x)

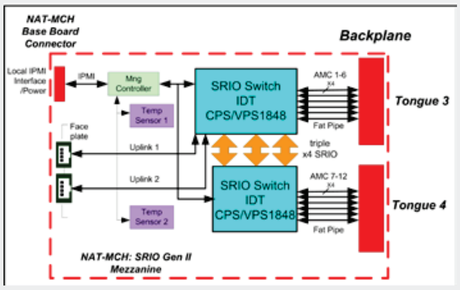


PCIe Gen 3 Switch

The **PCI Express Switching Mezzanine** is an AMC.1 compliant module of the **NAT-MCH** that enables users to add scalable high bandwidth, non-blocking interconnection to a wide variety of applications including servers, storage, video streaming, blade servers and embedded control products. The PCIe Hub module supports full non-transparent bridging functionality to allow implementation of multi-host systems and intelligent I/O modules in applications such as communications, storage and blade servers.

Key Features:

- **PCIe Gen 3**
- support for 12 AMC modules, Fabrics D-G
- non-blocking switch fabric
- upstream port configurable to any of the 12 AMC slots
- PCIe hot plug support for each AMC slot
- secondary (failover) host possible
- clustering support for 6 independent clusters with one configurable non-transparent upstream port; each cluster offers its own transparent upstream port
- supports x1 and x4 width ports to any AMC (x8 requires custom backplane)
- configuration option for Spread Spectrum Clock (SSC) or 100MHz fixed PCIe clock
- PCIe clock can be provided as Fabric Clock (FCLKA) to the AMC slots, via clock module



SRIO Gen 2 Switch

The **SRIO Gen 2 Mezzanine module** provides a non-blocking high performance data switching functionality for up to 12 AMCs. The non-hierarchical structure of SRIO allows for superior bandwidth between each end point. Additionally, SRIO data integrity and health checks are performed in hardware.

Key Features:

- **SRIO Gen 2**
- flexible port width: x1 and x4
- 20 Gb/s bandwidth per port (x4)
- operating baud rate per data lane 1.25 Gbaud, 2.5 Gbaud or 3.125 Gbaud, 5.0 Gbaud and 6.25 Gbaud
- transport layer error management
- low latency packet transport
- power down modes and routing capabilities per port
- decentralized communication model: pere-to-pere
- 2 uplink ports at front panel

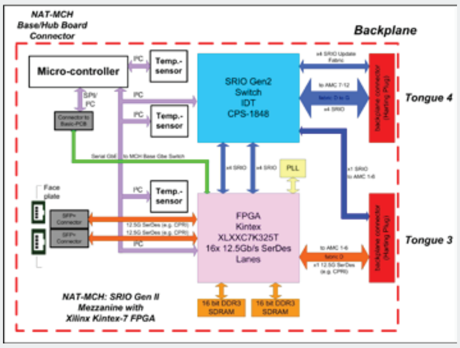
Technical Data

NAT-MCH

Serial Rapid I/O Gen 2 + FPGA

Telecom Clock and FCLK

Physics Clock + SSD



Custom Protocol Switch (based on Xilinx Kintex-7 FPGA)

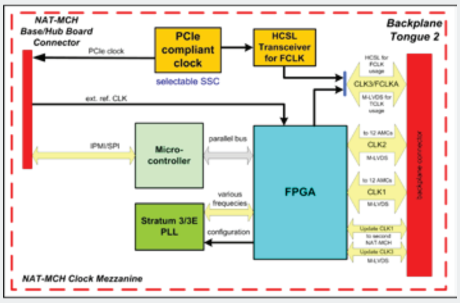
The **NAT-MCH**-FPGA combines the described SRIO Gen 2 switching features and a fully-customizable Kintex-7 FPGA. This special FPGA hub module is intended to be used for switching or multiplexing CPRI, OBSAI, as well as other standard protocols (e.g. SRIO, XAUI) or any fully customized serial protocol.

Key Features Xilinx Kintex-7 FPGA:

- customizable high speed serial connection (up to 12,5 Gb/s) to AMC1-6
- two high speed optical uplinks via SFP+
- dual x4 bridging data path between switch and FPGA
- 1Gb Ethernet connection to MCH base switch
- two independent DDR3 memories for user application (up to 4Gb each)
- on board low jitter PLL (Texas Instruments CDCE72010)

SRIO GenII Switch:

- x1 SRIO GenII Switch connection to AMC1-6
- x4 SRIO GenII switch connection to AMC 7-12

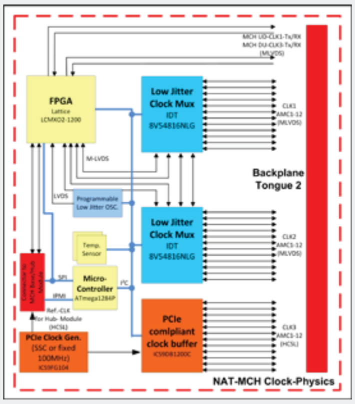


Standard Clock Mezzanine

The Clock Mezzanine Module allows a flexible selection of the telecom and non-telecom clocking structures as defined in MTCA.0. The on-board Stratum 3/3E type PLL can operate free running or logged on a reference from any of the 12 AMCs or on an external clock via the front panel SMA type connector. In conjunction with the PCIe Hub module it provides a PCIe compliant fabric clock (FCLKA) to all AMC slots. This can be either a 100MHz fixed or 100MHz Spread Spectrum clock (SSC). The PCIe clock can be provided complying to HCSL or MLVDS signalling levels.

Key Features:

- support of AMC clocks CLK1, CLK2 and CLK3 for up to 12 AMCs
- update clock for a second **NAT-MCH** in redundant systems
- reference clock In/Output on front panel
- stratum 3/3E type PLL clock source for telecom applications
- variable switching and distribution of clocks by on-board FPGA
- reference for the Stratum 3/3E PLL can be either CLK1 or CLK2 from any AMC or sourced from front panel
- PCI Express compliant clock signal can be distributed via FCLKA (CLK3) to all 12 AMCs



Physics Clock Mezzanine

Beside the standard Clock Mezzanine, N.A.T. offers the Clock Mezzanine for Physics. The development of this module is driven by the demands of physics group requiring very low jitter and constant latency. These features are realised by using a specialized Clock Multiplexer developed in cooperation with IDT (Integrated Device Technology Inc.).

Key Features:

- CLK1 connections for all 12 AMC multiplexed by one device.
- CLK2 connections for all 12 AMC multiplexed by one device.
- two direct multiplexer interconnections
- fixed low jitter reference clock
- connection to front panel clock interface
- PCIe reference clock distribution for 12 AMCs via CLK3 (AMC.0 R2.0 - FCLKA)