PREMIUM

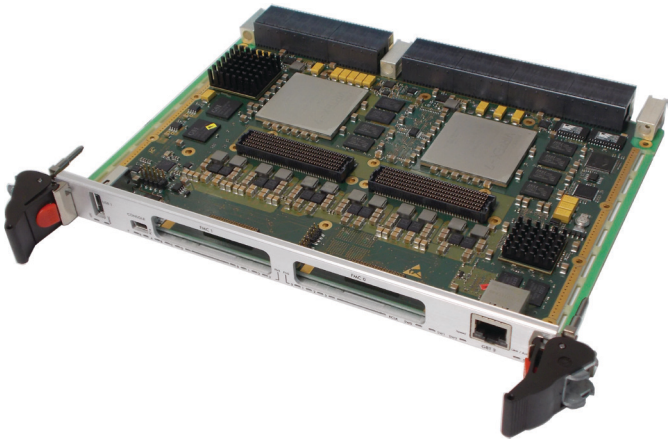
IC-FEP-VPX6b

Virtex®-7 & QorIQ™ 6U VPX processing unit

At the top of our Front End Processing range, the **IC-FEP-VPX6b** renews the proven architecture of the **IC-FEP-VPX6a** while increasing the processing capability by offering two user programmable Virtex®-7 FPGAs and one QorIQ T1042 processor.

Designed for high performance Signal Processing applications, **IC-FEP-VPX6b** delivers the best that the current technology can provide.

Associated with the other building blocks of our OpenVPX product ranges (Intel® and Freescale™ SBCs, Ethernet Switches & Routers, IO boards/FMC, Graphic), the **IC-FEP-VPX6b** running our Signal Processing Reference Design (including signal acquisition, Processing, DMA Engine, data storage, signal generation...) is the ideal platform for customers who want to streamline development by concentrating their efforts on most critical tasks.



Description

The **IC-FEP-VPX6b** is controlled by a QorIQ T1042 quad-core supporting four integrated 64-bit e5500 Power Architecture® processor cores with high-performance data path acceleration architecture (DPAA) and network peripheral interfaces required for demanding processing application.
(*Option: T2081 with four dual threaded e6500 64-bit cores implementing Altivec technology; up to 4GB DDR3*)

The QorIQ provides the usual external interfaces: Ethernet, Serial and USB ports. Moreover, one eUSB slot allows to plug an optional SSD module.

The PCIe advanced switch allows versatile coupling between the processor, the FPGAs and the fabric links of P1 VPX connector. (Non transparent configuration possible for VPX fabric link).
Other Fabric Links of the VPX backplane are directly connected to the FPGAs GTH transceivers. Moreover, the two FPGAs are directly interconnected via 8 GTH lanes and 35 LVDS signals.

Each Virtex®-7 FPGAs of the **IC-FEP-VPX6b** is coupled with two DDR3 SDRAM memory banks supporting up to 1800 MT/s transfers and two DDRII+ SRAM memory banks.

Each Virtex®-7 FPGA is interfaced with four SPI Mirror flash memories: three for local bitstreams storage (1 reserved for IC bitstream, 2 for user bitstreams) and one for user parameters.

The FMC sites of the **IC-FEP-VPX6b** are fully compliant with the FPGA Mezzanine Card standard (VITA 57.1), allowing to install FMC modules provided by IC, third-partie or developped by customers.

Each FMC can optionaly be equipped with a novel IOs connector to route sixteen differential pairs (100 Ohms) from the FMC module directly to the VPX backplane.

Main features

Processing Units

- One **QorIQ processor T1042, e5500** quad core with:
  - 2 GB of DDR3L SDRAM with ECC *(up to 4GB)*
  - 3 * 1GB Mirrorbit SPI Flashes (Boot, BackUp & User, *option: 2GB possible*)
  - 32GB (MLC) or 16GB (SLC) Nand flash (user)
  - optional Nand Solid-state Disk (eUSB module)
- two **Xilinx Virtex-7 XC7VX690T**, both offering:
  - two banks of DDR3 : 64-bit wide/2GB each
  - two banks of SRAM DDRII+: 18-bit wide/72 Mbits *(up to 144Mb)*
  - SPI mirror flash memories

  (VX330T or VX485T possible with restriction)

  the two FPGA are interconnected through:
  - 8 * GTH lanes
  - 35 * LVDS

- **one Gen2 PCIe switch** *(Gen2/3)*
- **one Giga Ethernet L2 switch**

VPX Interfaces

- 4 * PCIe x4 port (from PCIe switch)
- GTH ports (4 * GTH x4 from each FPGA)
- General purpose IOs
  - 2*16LVDS (16 from each FPGA)
  - 2*16 differential pairs (16 from each optional FMC IOs connector)
  - 3 * QorIQ Serdes (1*PCie x1 & 2 Sata or 2*PCie x1 & 1 Sata)
- 4 * Ethernet ports (2 * 1000BT & 2 * 1000BX - from switch)
- 1 * RS485/RS232 port
- 2 * USB 2.0 ports
- PIC µ-controller for System Management (per VITA 46.11)

FMC interfaces (HPC for each site, one per FPGA)

- 80 LVDS
- 4 reference clocks
- 2 * GTH x4 links
- optional connector for IOs report to the backplane

Front panel interfaces

- 1 * USB 2.0, 1 * Ethernet 1000BT, 1 * console port and leds

The **IC-FEP-VPX6b** is a VPX 6U / 4HP 1" board compliant with 6U module definitions of the VITA 46.0 standard. It is available in air-cooled and conduction-cooled grades.

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IC INTERFACE CONCEPT
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IC-FEP-VPX6b

Virtex®-7 & QorIQ™ 6U VPX processing unit with two FMC sites

On-board firmware

UBoot

Our basic firmware takes in charge Freescale's new QorIQ initialization. This on-board firmware is an efficient set of software stored in a secured flash.

OS support

Interface Concept provides LSP Linux® distribution (Yaeld development tool chain) and VxWorks® 6.9.

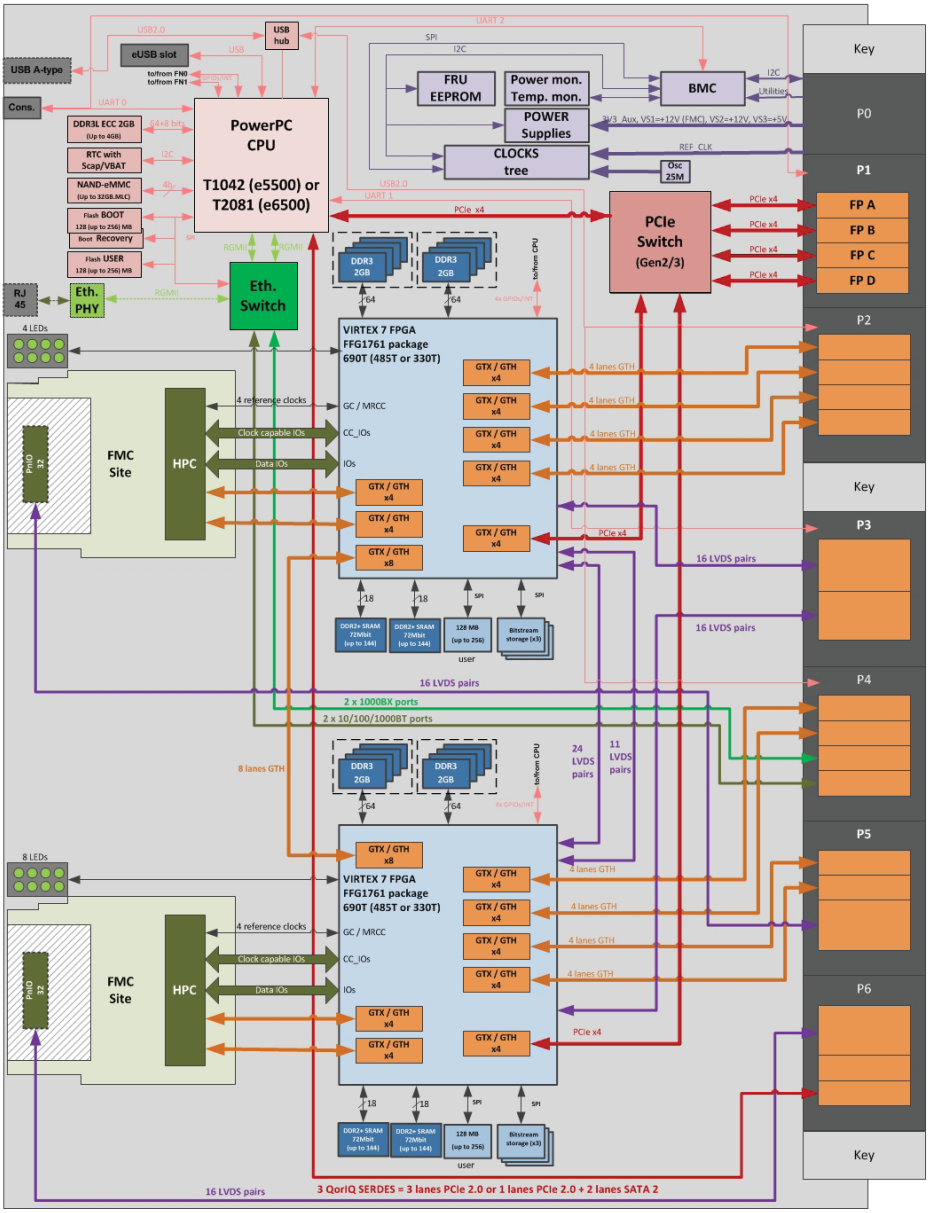
Firmware

The **IC-FEP-VPX6b** hardware platform is compatible with Xilinx development tools Vivado.
Interface Concept provides VHDL code for system services (DDR3, SRAM, PCIe, Aurora, IC FMC interfaces, etc.) and reference designs such as PCIe DMA Engine, signal capture & processing, etc.

Multiware

In order to empower customers to concentrate their efforts on most critical tasks, Interface Concept has developed a Fabric Management Software implemeing optimized services between PCIe domains over non transparent bridges NTB such as: DMA transfers, Ethernet emulation over PCIe, management of shared memory, messages and semaphores, etc. (consult us for details)

Block Diagram



Environment Specifications:

Please consult the **IC-FEP-VPX6b** page at **www.interfaceconcept.com**.

Ordering Information:

Please contact our sales department : tel. **+33 (0)2 98 573 030** - email : **info@interfaceconcept.com**

This document supersedes any earlier documentation relating to the products referred to herein. The information contained in this document is current at the date of publication. It may subsequently be updated or withdrawn without notice.

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