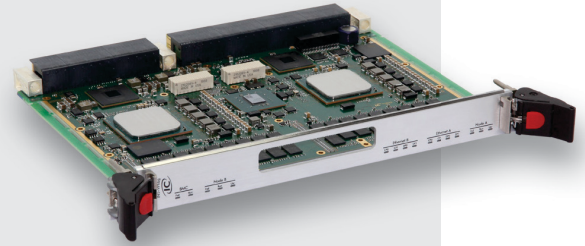


IC-INT-VPX6g

6U VPX Dual Intel® Xeon®-D & Xilinx® Kintex® SBC

- 6U VPX
- Dual Intel® Xeon® D-1539/1559 processor
- up to 128 GB DDR4 with ECC
- Xilinx Kintex®-7 FPGA
- 40 GbE & PCIe Gen3 interfaces
- XMC slot



Overview

The **IC-INT-VPX6g** is a 6U VPX Single Board Computer (SBC) with a dual processing node and an on-board FPGA. This board is the result of Interface Concept's extensive expertise in the High Performance Embedded Computing (HPEC) field.

Combined with Interface Concept VPX 6U Ethernet switches (ComEth products) and FPGA boards (IC-FEP products), the **IC-INT-VPX6g** provides integrators with the ideal Digital Signal Processing (DSP) board to build High Performance Computers.

Powered by Intel®'s 14nm Xeon®D processor technology and operating within the umbrella of the OpenVPX standard, the **IC-INT-VPX6g** is a comprehensive dual-processor design for applications requiring the highest processing capabilities with a controlled power consumption.

Description

The **IC-INT-VPX6g**'s two computing nodes (A & B) consist of a dual twelve-core Xeon® D-1559 processor or dual eight-core Xeon® D-1539 processor which are equipped with up to 64GB DDR4/node, meaning 128GB DDR4 in total.

The two processors are interconnected via a 4-lane PCIe Gen3 link and a Xilinx Kintex®-7 Core function FPGA, which is itself also connected to the P3/P4 VPX connector via SERDES and Multiple Purpose IOs and Multi-Gigabit Transceivers.

The FPGA can be used to integrate additional functions, among which ARINC818, HDLC or SFPDP which Interface Concept can provide as a separate IP.

The **IC-INT-VPX6g** also features two on-board high speed 10/40GbE controllers which interface to the P1 connector.

The **IC-INT-VPX6g** complies with the OpenVPX™ standard and supports the following interfaces on the Data, Control and Expansion planes:

Control Plane:

- one 1000BASE-T interface and one 1000BASE-KX/10GBASE-KR per node

Data Plane:

- two 40GBASE-KR4 or four 10GBASE-KR per node (also supports two 10GBASE-KX4 or four 1GBASE-KX)

Expansion plane:

- one 4-lane PCIe Gen2/3 port on the VPX P2 connector per node

For further customizations, an XMC slot is available and connected to node A via a 4-lane PCIe interface and to node B by a 1-lane PCIe interface.

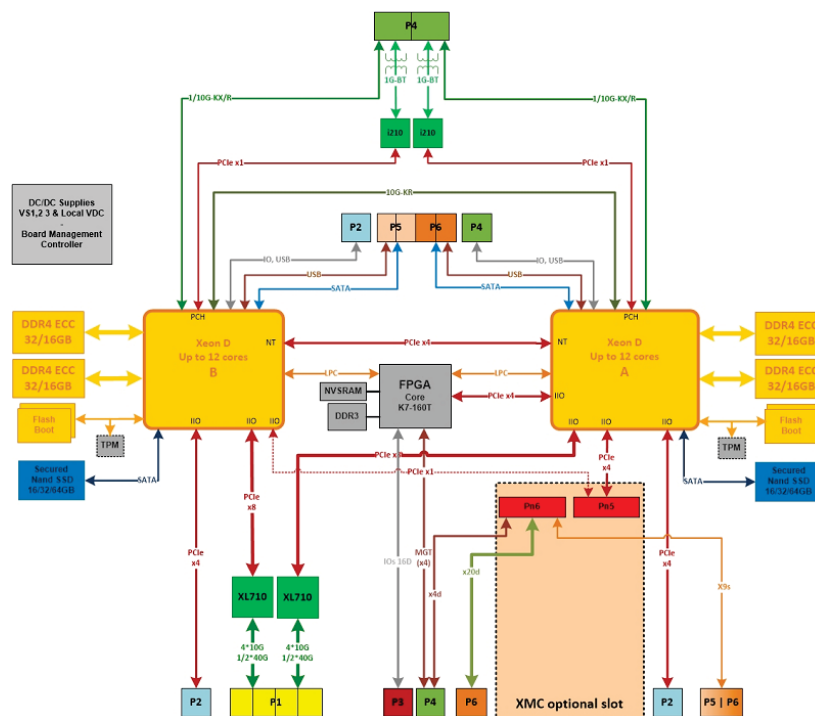
The **IC-INT-VPX6g** also provides additional storage and communication features for each processing node such as a scalable SATA NAND SDD, GPIOs, USB and SATA ports.

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Computer

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Block Diagram



Main features

Processing Unit

- 2* Intel Xeon® D-1539 or D-1559
- D-1539: 8-core 45 W @ 1,60 GHz
- D-1559: 12-core 35 W @ 1,50 GHz
- 64 GB DDR4 with ECC per node
- 32 GB SLC SSD SATA
- 4* SATA Gen3 ports [RB_P5 and P6]
- 4* USB2 ports [RB_P2, P4, P5 and P6]
- 8* GPIOs [RB_P2 and P4]

1*XMC 2.0 Slot (VITA 61)

- PCIe x4 Gen3 to CPU-A (Pn5)
- (Pn6) X12d + X8d to RB_P6 (VITA 46.9)
- (Pn6) X4d to RB_P4, X9s to RB_P5,P6

1*FPGA Kintex®-7 (XC7K160T)

- 16 LVDS pairs [RB_P3]
- 4 MGTs [RB_P4]
- 512MB DDR3L
- 512Kb NVSRAM

Data Plane

- 2*40GBASE-KR4 (rear P1A, P1B) from CPU-B
 - 2*40GBASE-KR4 (rear P1C, P1D) from CPU-A
- Other configurations possible :
- 4*+ 4* 10GBASE-KR
 - 2*+ 2* 10GBASE-KX4
 - 4*+ 4* 1GBASE-KX

Control Plane

- 2 * 1000BASE-KX [RB_P4] (one per CPU)
- 2 * 10/100/1000BASE-T [RB_P4] (one per CPU)

Expansion Plane (PCIe Gen2/3)

- 4 lanes on [RB_P2B] (from CPU-A)
- 4 lanes on [RB_P2A] (from CPU-B)

The **IC-INT-VPX6g** is a 6U x 5HP (1") VPX board compliant with 6U module definitions of the VITA 46.0 standard (0.80" or 0.85": please consult us).

The **IC-INT-VPX6g** board is available in air-cooled and conduction-cooled (without any front I/O) versions.

On-board firmware

Interface Concept Single Board Computers based on Intel CPUs, use the new UEFI firmware technology.

This Boot Loader, **developed and tested by our R&D team**, implements all the initializations and optimized PBITs while

ensuring the shortest boot time before launching the UEFI shell or loading the Operating System from storage devices (CD, DVD, HDD, USB...) or network.

When the final application is running, Runtime services remain in memory thus allowing the user to access UEFI variables for monitoring (e.g. PBIT results) or setup operations.

On request, Interface Concept can customize the Boot Loader to keep only what is strictly necessary for customer's applications.

OS support

Interface Concept provides LSP Linux® distributions (IC SDK, others...) and VxWorks® 7.0. Other BSPs can be supported on request.

Multware

In order to empower customers to concentrate their efforts on their most critical tasks, Interface Concept has developed a Fabric Management Software implementing optimized services between PCIe domains over non transparent bridges (NTB) such as: DMA transfers, Ethernet emulation over PCIe, management of shared memory, messages and semaphores, etc. (Please consult us for details)

Grades

Criterion	Coating	Operation Temperature	Rec. Airflow	Oper. HR% no cond.	Storage Temperature	Sinusoidal Vibration	Random Vibration	Shock 1/2 Sin. 11ms
Standard	Optional	0 to 55°C	1 .. 2 m/s	5 to 90%	-45 to 85°C	2G [20..2000]Hz	0.002g2 /Hz [10..2000]Hz	20G
Extended	Yes	-20 to 65°C	2 .. 3 m/s	5 to 95%	-45 to 85°C	2G [20..2000]Hz	0.002g2 /Hz [10..2000]Hz	20G
Rugged	Yes	-40 to 75°C or 85° C (*)	2 .. 5 m/s	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.05g2 /Hz [10..2000]Hz	40G
Conduction-Cooled 71°C	Yes	-40 to 71°C at the thermal interface (*)	-	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.05g2 /Hz [10..2000]Hz	40G
Conduction-Cooled 85°C	Yes	-40 to 85° C at the thermal interface (*)	-	5 to 95%	-45 to 100°C	5G [20..2000]Hz	0.1g2 /Hz [10..2000]Hz	40G

(*) : Temperature grades are subject to availability according to IC products. Please consult us.

All information contained herein is subject to change without notice.

For more information, please contact:



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