TPMC317

Conduction Cooled

6 Channel SSI, Incremental Encoder, Counter

Version 1.0

User Manual

Issue 1.0.2

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TPMC317-10R

Conduction Cooled

6 Channel SSI, Incremental Encoder, Counter

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial Issue	February 2009
1.0.1	Added: "7.2 Clock Output Wiring"	June 2010
1.0.2	General Revision	August 2014

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1   Product Description

The TPMC317 is a conduction cooled single-width 32 bit PMC module and offers six independent channels. Each of these channels can operate as a standard SSI interface controller, in a SSI 'Listen only' Mode, as an incremental encoder or general purpose counter.

The standard SSI interface controller outputs a clock burst to the absolute encoder and receives the returned positional data. The SSI interface controller operates with a programmable clock rate from 1µs to 15µs and programmable data word length from 1 bit to 32 bit.

In 'Listen only' Mode the channel listens to an existing SSI interface to observe its data transfer. It takes both the SSI clock and data as inputs. In 'Listen only' Mode the channel also has a programmable data word length from 1 bit to 32 bit; the SSI clock rate of the observed SSI interface can be in the range of 1µs to 15µs.

In both modes the data word can be encoded in Binary- or in Gray code and with odd, even or no parity.

The 32 bit incremental encoder counter is a preloadable up- and down counter. The counter is programmable for single, double and quadruple analysis of the encoder signals. In conjunction with the isolated 24V digital inputs it provides the possibility of automatic preload of the counter whenever the motion system passes a reference position.

The 32 bit general purpose preloadable up- and down counter can be fed with an internal clock or with external signals.

Both counter modes offer a 32 bit preload register, a 32 bit compare register and various count modes.
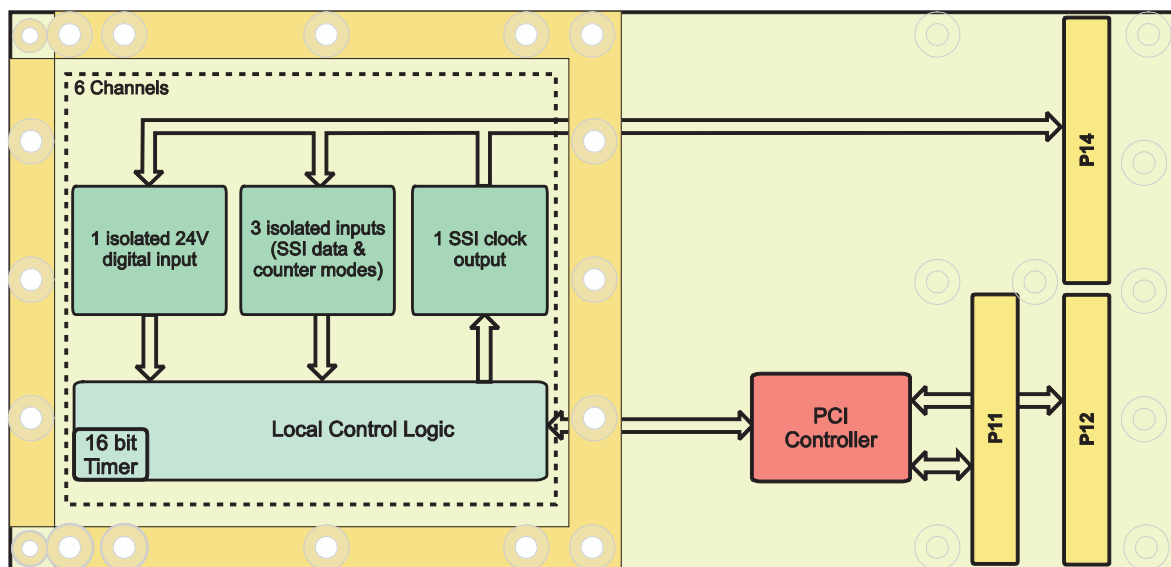
Figure 1-1 : Block Diagram

A 'Multiple Channel Read' function latches the actual values of all enabled channels whose values can then be read without interfering with normal function. In addition the TPMC317 provides a 16 bit down-counter with preload register which allows timing intervals of up to 65ms. It can be used as reference timer for closed loop applications or as trigger for the Multiple Channel Read function.

All data inputs are isolated. The level of the input signals can be RS422 or TTL. The input signals pass a digital filter for noise suppression before they are further used. The level of the SSI clock output signals is RS422.

2 Technical Specification

PMC Interface	
Mechanical Interface	PCI Mezzanine Card (PMC) Interface confirming to IEEE P1386/P1386.1 Single Size
Electrical Interface	PCI Rev. 2.2 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage
On Board Devices	
PCI Target Chip	PCI9030 (PLX Technology)
I/O Interface	
Number of Channels	6 isolated channels with 3 input lines and 1 output line per channel
Input Levels	RS422 differential and TTL single-ended
ESD Protection	±15kV—Human Body Model ±8kV—IEC 1000-4-2, Contact Discharge ±15kV—IEC 1000-4-2, Air-Gap Discharge
Number of Isolated Digital Inputs	6 digital inputs: reference input or general purpose input depending on mode
Maximum Input Frequency	5 MHz
Input Voltage	24V DC typical
Input Current	4.2mA @ 24V input voltage
Input Switching Level	12V typical, 7.5V minimum, 14V maximum
Interval Timer	Programmable with timing intervals up to 65ms
I/O Connector	PMC P14 I/O (64 pin Mezzanine Connector)
Physical Data	
Power Requirements	130 mA typical @ +5V DC 60 mA typical @ +3.3V DC
Temperature Range	Operating -40°C to +85°C Storage -40°C to +85°C
MTBF	430 000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.
Humidity	5 – 95 % non-condensing
Weight	60 g

Figure 2-1 : Technical Specification

3 Local Space Addressing

3.1 PCI9030 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9030 local spaces.

PCI9030 Local Space	PCI9030 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	2 (0x18)	MEM	256	32	BIG	Local Register Address Space
1	3 (0x1C)	-	-	-	-	Not Used
2	4 (0x20)	-	-	-	-	Not Used
3	5 (0x24)	-	-	-	-	Not Used

Table 3-1 : PCI9030 Local Space Configuration

3.2 Local Register Address Space

PCI Base Address: **PCI9030 PCI Base Address 2 (Offset 0x18 in PCI Configuration Space).**

Offset to PCI Base Address 2	Register Name	Size (Bit)
0x00	Control Register 0	32
0x04	Data Register 0	32
0x08	Status Register 0	32
0x0C	Counter Preload Register 0	32
0x10	Counter Compare Register 0	32
0x14	Counter Command Register 0	32
0x18	Control Register 1	32
0x1C	Data Register 1	32
0x20	Status Register 1	32
0x24	Counter Preload Register 1	32
0x28	Counter Compare Register 1	32
0x2C	Counter Command Register 1	32
0x30	Control Register 2	32
0x34	Data Register 2	32
0x38	Status Register 2	32
0x3C	Counter Preload Register 2	32
0x40	Counter Compare Register 2	32
0x44	Counter Command Register 2	32

Offset to PCI Base Address 2	Register Name	Size (Bit)
0x48	Control Register 3	32
0x4C	Data Register 3	32
0x50	Status Register 3	32
0x54	Counter Preload Register 3	32
0x58	Counter Compare Register 3	32
0x5C	Counter Command Register 3	32
0x60	Control Register 4	32
0x64	Data Register 4	32
0x68	Status Register 4	32
0x6C	Counter Preload Register 4	32
0x70	Counter Compare Register 4	32
0x74	Counter Command Register 4	32

Offset to PCI Base Address 2	Register Name	Size (Bit)
0x78	Control Register 5	32
0x7C	Data Register 5	32
0x80	Status Register 5	32
0x84	Counter Preload Register 5	32
0x88	Counter Compare Register 5	32
0x8C	Counter Command Register 5	32
0x90	Digital Input Register	32
0x94	Interval Timer Control Register	32
0x98	Interval Timer Preload Register	32
0x9C	Interval Timer Data Register	32
0xA0	Global Control Register	32
0xA4	Interrupt Enable Register	32
0xA8	Interrupt Status Register	32
0xAC	Test Register	32

Table 3-2 : Local Register Address Space

3.3 Control Register

The Control Register is divided into two parts: bits[15:0] are dedicated for SSI control; bits [31:16] are dedicated for Counter control.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Counter Setup															
	0	0	0	POL		ICM			SCM		CLKDIV		INPUT			

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SSI Setup															
	BREAK	MODE		BC					CODE	ZB	EO	PAR		CR		

Bit	Symbol	Description	Access	Reset Value
31:29	**-**	**Reserved, always reads as '0'**	**-**	**0**
28:26	**POL [2:0]**	**A,B,I Polarity** **The Input Polarity Control can be used to adapt the input to the input source polarity.** Bit Input Polarity 26 A 0 = high active, 1 = low active 27 B 0 = high active, 1 = low active 28 I 0 = high active, 1 = low active	**R/W**	**000**
25:23	**ICM [2:0]**	**Index Control Mode** **The Index Control Mode determines how the counter interprets events on the I-input.** **Reference modes are only valid when Input Mode = Quadrature Count** ICM Mode None Reference Mode 000 Ignore I-input 001 Load on I 010 Latch on I 011 Gate on I 100 Reset on I Reference Modes 101 Reference mode 110 Auto reference mode 111 Index mode **See chapter '6.3.3 Index Control Modes' for details.**	**R/W**	**000**
22:21	**SCM [1:0]**	**Special Count Mode** SCM Mode 00 No special mode active / cycling counter 01 Divide-by-N 10 Single Cycle **See chapter '6.3.2 Special Count Modes' for details.**	**R/W**	**00**
20:19	**CLKDIV [1:0]**	**Internal Clock Prescaler** CLKDIV Prescaler Clock frequency 00 1x 32 MHz 01 2x 16 MHz 10 4x 8 MHz 11 8x 4 MHz	**R/W**	**00**

Bit	Symbol	Description	Access	Reset Value
18:16	INPUT [2:0]	**Counter Input Mode** **The Input Mode determines the input source and how the counter interprets these input signals. The Quadrature mode can be used with a 1x, 2x or 4x resolution multiplier.** | INPUT	Input Mode	Input Source
---	---	---
000	Counter disabled	-
001	Timer Mode Up	Internal Clock Prescaler
010	Timer Mode Down	Internal Clock Prescaler
011	Direction Count	Input A & Input B
100	Up/Down Count	Input A & Input B
101	Quadrature Count 1x	Input A & Input B
110	Quadrature Count 2x	Input A & Input B
111	Quadrature Count 4x	Input A & Input B | **See chapter '6.3.1 Input Modes' for details.**	R/W	000
15	BREAK	**Break on Read Error (Listen only)** **1 = The channel stops to listen on read errors** **0 = Read errors are ignored and the channel resumes to listen**	R/W	0
14	MODE	**1 = SSI 'Listen only' Mode** **0 = Standard SSI Interface Controller**	R/W	0
13	BC5	**Number of Data Bits** **Bits are used to program the number of bits of the serial absolute encoder. It can be read and written by software. The data bits must be programmed in the range from 1 to 32.** **BC5…BC0 = 0x01 to 0x20 means 1 to 32 bit.** **BC5…BC0 = 0x00 not valid** **BC5…BC0 = 0x21 to 0x3F not valid**	R/W	0
12	BC4			
11	BC3			
10	BC2			
9	BC1			
8	BC0			
7	CODE	**SSI Data word coding** **1 = Gray Code** **The data word is converted into binary code** **0 = Binary Code**	R/W	0
6	ZB	**Parity Bit with Zero Bit, controls the clock cycles** **1 = two additional clock cycles** **0 = one additional clock cycle** **are provided to get the parity bit**	R/W	0
5	EO	**Controls the parity detection** **1 = odd parity** **0 = even parity** **This bit is ignored if bit 4 is set to '0'.**	R/W	0
4	PAR	**Encoder with parity - If encoder provides a parity bit:** **1 = detect parity errors** **0 = do not detect parity errors / no parity bit**	R/W	0

Bit	Symbol	Description	Access	Reset Value
3	CR3	**Clock Rate for encoder serial clock speed**	R/W	0
2	CR2	**The clock can be programmed in steps of 1µs in the range of 1 to 15. A value of 0 for the clock rate will stop the operation of the SSI interface.**		
1	CR1			
0	CR0	**The 'Listen only' Mode will ignore the Clock Rate setting; in this mode the Clock Rate will be detected automatically.**		

Table 3-3 : Control Register

Note that a value of 0x00 or a value from 0x21 to 0x3F for BC5...BC0 is not valid and will stop the operation of the SSI Interface.

3.4 Data Register

Bit	Symbol	Description	Access	Reset Value
31:0	-	**Data Register**	**R/W**	0

Table 3-4 : Data Register

When the channel is disabled, the Data Register returns 0x00000000 on read accesses.

3.4.1 Data Register in SSI Mode

The serial data of the absolute encoder is shifted into the Data Register.

In Standard SSI Interface mode a write access to the Data Register initiates a data transfer from the absolute encoder independently of the other channels.

In 'Listen only' SSI Interface mode a read access to the Data Register sets the Busy bit to '1' and the channel is listening again.

The data register may not contain valid data, if the serial data transfer is in progress (the corresponding Busy bit is read as '1').

3.4.2 Data Register in Counter Mode

The Data Register contains the actual counter value.

While a Multiple Channel Read is in progress, this register may contain latched data. In 'Latch on I' control mode this register contains latched data after a control mode event. See chapter 'Data Register Lock' for details.

3.5 Status Register

The Status Register is divided into two parts: bits[15:0] are dedicated for SSI status; bits[31:16] are dedicated for Counter status.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
						Counter Status										
	0	0	0	0	0	0	0	0	SGL	OVFL	DRL	DIR	SGN	MAT	CRY	BOR

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						SSI Status										
	0	0	0	0	0	0	0	0	0	0	0	0	0	RER	PRY	BSY

Bit	Symbol	Description	Access	Reset Value
31:24	**-**	**Reserved, always reads as '0'**	**-**	**0**
23	**SGL**	**Single Cycle active** **In Single Cycle counting mode this bit is set to '1' when the counter is active. It is reset to '0', when the counter has counted down to zero.**	**R**	**0**
22	**OVFL**	**Data Register Latch Overflow** **When a Latch Mode event occurs while the Data Register Lock is still active, the data in the Data Register will be retained and this bit will be set to indicate that data was lost. This bit must be reset by writing a '1' to this bit.**	**R/C**	**0**
21	**DRL**	**Data Register Latch** **This bit is set to '1', when the Data Register is locked due to a 'Latch on I' or a Multiple Channel Read. This bit is cleared after a read access to the Data Register or by writing a '1' to this bit.**	**R/C**	**0**
20	**DIR**	**Count Direction** **This bit indicates the counting direction of the counter.** **'1' indicates up, '0' indicates down. In the 'Up/Down Count' mode this bit indicates the direction at the last count. In the 'Direction Count' mode this bit corresponds to the I-input.**	**R**	**0**
19	**SGN**	**Sign** **The Sign bit is set to '1' when the counter overflows, and is set to '0' when the counter underflows.** **After reset or power-up this bit should be considered as "don't care" until the first Carry or Borrow occurred.**	**R**	**0**

Bit	Symbol	Description	Access	Reset Value
18	**MAT**	**Match** This bit is set to '1' when the counter value matches the value of the Counter Compare Register. This bit must be reset by writing a '1' to this bit.	**R/C**	**0**
17	**CRY**	**Carry** This bit is set to '1' when the counter changes from 0xFFFFFFFF to 0x00000000. This bit must be reset by writing a '1' to this bit.	**R/C**	**0**
16	**BOR**	**Borrow** This bit is set to '1' when the counter changes from 0x00000000 to 0xFFFFFFFF. This bit must be reset by writing a '1' to this bit.	**R/C**	**0**
15:3	**-**	**Reserved, always reads as '0'**	**-**	**0**
2	**RER**	**Read Error** **1 = Data is invalid because of an error during the last transmission** **0 = Data OK** **This bit is only valid for channels in 'Listen only' mode. For channels in Standard SSI Interface Controller mode this bit will always read '0'** **Reasons for a read error are:** **- The number of data bits set in the control register does not match the actual size of the received transmission.** **- Only a partial transmission was received (this could happen when the mode is switched and a transmission is in progress on the observed SSI-interface).**	**R**	**0**
1	**PRY**	**Parity Error** **1 = Parity Error at the last data transmission** **0 = No Parity Error at the last data transmission** **During a transmission the parity error bit is not valid.** **The parity error status is updated only if the parity enable bit of the corresponding channel is set to '1'. Otherwise the parity status is read as '0'.**	**R**	**0**
0	**BSY**	**Busy Bit** **0 = Data Ready (set after every completed transmission, even if a parity or a read error was issued)** **In Standard SSI Interface Controller mode Busy Bit = '1' indicates a transmission in progress.** **In 'Listen only' Mode the Busy Bit is set to '1' when a transmission is in progress. It is set to '0' when transmission was received and stays '0' until the data word was read.**	**R**	**0**

Table 3-5 : SSI Status Register

3.6 Counter Preload Register

Bit	Symbol	Description	Access	Reset Value
31:0	**-**	**Counter Preload Register** **The value of this register can be loaded into the counter by:** **- Setting bit 1 (LCNT) of the Counter Command Register** **- An impulse on the I-input when the 'Load on I'-mode is active** **- Automatically in the 'Divide-by-N'-mode every time the counter creates a borrow or a carry** **- Reference modes**	**R/W**	**0**

Table 3-6 : Counter Preload Register

3.7 Counter Compare Register

Bit	Symbol	Description	Access	Reset Value
31:0	**-**	**Counter Compare Register** **Every time the counter matches the Counter Compare Register value, bit 18 (MAT) of the Status Register is set to '1' and, if enabled, an interrupt is generated.**	**R/W**	**-1**

Table 3-7 : Counter Compare Register

3.8 Counter Command Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
									Reserved							
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								Reserved							LCNT	RCNT
	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit	Symbol	Description	Access	Reset Value
31:2	**-**	**Reserved, always reads as '0'**	**-**	**0**
1	**LCNT**	**Load Counter** **Write '1' to load the counter with the value of the Counter Preload Register.**	**W**	**0**
0	**RCNT**	**Reset Counter** **Write '1' to reset the counter.**	**W**	**0**

Table 3-8 : Counter Command Register

Commands are performed by writing a '1' to the according bit.

3.9 Digital Input Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				Digital Input Interrupt Control						Digital Input Status					
	0	0	0	0	DIIC5	DIIC4	DIIC3	DIIC2	DIIC1	DIIC0	DI5	DI4	DI3	DI2	DI1	DI0

Bit	Symbol	Description	Access	Reset Value
31:12	**-**	**Reserved, always reads as '0'**	**-**	**0**
11 **10** **9** **8** **7** **6**	**DIIC5** **DIIC4** **DIIC3** **DIIC2** **DIIC1** **DIIC0**	**Digital Input Interrupt Control** **Selects interrupt on rising or falling edge for corresponding 24V digital input.** **1 = selects interrupt for rising edge** **0 = selects interrupt for falling edge**	**R/W**	**0**
5 **4** **3** **2** **1** **0**	**DI5** **DI4** **DI3** **DI2** **DI1** **DI0**	**These bits reflect the actual state of the digital 24V inputs.** **In "Reference Mode" and "Auto Reference Mode" the digital 24V inputs are used as reference inputs.** **In all other modes the digital 24V inputs can be used as general purpose inputs.**	**R**	**-**

Table 3-9 : Digital Input Register

3.10 Interval Timer Control Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
								Reserved								
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						Reserved										
	0	0	0	0	0	0	0	0	0	0	0	0	0	ITDIV		ITEN

Bit	Symbol	Description	Access	Reset Value
31:3	**-**	**Reserved, always reads as '0'**	**-**	**0**
2:1	**ITDIV**	**Interval Timer Clock Divider** Value Mode 0 0 8 MHz 0 1 4 MHz 1 0 2 MHz 1 1 1 MHz	**R/W**	**0**
0	**ITEN**	**Interval Timer Enable** **'0' disables the Interval Timer** **'1' enables the Interval Timer**	**R/W**	**0**

Table 3-10: Interval Timer Control Register

3.11 Interval Timer Preload Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
								Reserved								
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						Interval Timer Preload Register										
						ITPRE										

Bit	Symbol	Description	Access	Reset Value
31:16	**-**	**Reserved, always reads as '0'**	**-**	**0**
15:0	**ITPRE**	**Interval Timer Preload Register**	**R/W**	**0**

Table 3-11: Interval Timer Preload Register

3.12 Interval Timer Data Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
								Reserved								
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							Interval Timer Data Register									
								ITDR								

Bit	Symbol	Description	Access	Reset Value
31:16	**-**	**Reserved, always reads as '0'**	**-**	**0**
15:0	**ITDR**	**Interval Timer Data Register** **This register contains the actual Interval Timer Value.**	**R/W**	**0**

Table 3-12: Interval Timer Data Register

3.13 Global Control Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			Reserved								MCR				Manual	
	0	0	0	0	0	MCRTR	MCRST	ITRG	SL5	SL4	SL3	SL2	SL1	SL0	PRL5	PRL4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Counter Preload				Interface Control											
	PRL3	PRL2	PRL1	PRL0	IC5		IC4		IC3		IC2		IC1		IC0	

Bit	Symbol	Description	Access	Reset Value
31:27	**-**	**Reserved, always reads as '0'**	**-**	**0**
26	**MCRTR**	**Multiple Channel Read Trigger** **By writing '1' to this bit, a Multiple Channel Read is triggered.** **This is only valid for channels which are already enabled for a Multiple Channel Read. Do not set the SLx bits and the MCRTR bit on the same write access!**	**W**	**0**

25	MCRST	**Multiple Channel Read Status** **This bit indicates pending Multiple Channel Read data.** **When a SSI channel is enabled for Multiple Channel Read, it takes time for the conversion to complete. This bit indicates that the conversions of all enabled channels are complete.** **1 = Multiple Channel Read Data is valid (for all enabled channels)** **0 = The Data Registers of all enabled channels have been read out.** **To reset a multiple channel read sequence, write '1' to this bit**	**R/C**	**0**
24	ITRG	**Interval Timer as trigger for Multiple Channel Read** **1: Enable Interval Timer as trigger for multiple channel read** **0: Disable Interval Timer as trigger for multiple channel read**	**R/W**	**0**
23	SL5	**Enable Multiple Channel Read for the corresponding channel**	**R/W**	**0**
22	SL4	**1 = enables multi channel read** **0 = disables multi channel read**		
21	SL3			
20	SL2	**See chapter '6.4 Multiple Channel Read' for details.**		
19	SL1			
18	SL0			
17	PRL5	**Manual Counter Preload**	**W**	**0**
16	PRL4	**Writing a '1' issues a preload of the corresponding counter with the value of the Counter Preload Register. This preload method is only possible for channels in a 'None Reference Mode'.**		
15	PRL3			
14	PRL2			
13	PRL1	**Before using this preload method, the corresponding Counter Preload Registers must be loaded with valid data**		
12	PRL0			
11:10	IC5 [1:0]	**Interface Control**	**R/W**	**0**
9:8	IC4 [1:0]	IC Mode		
7:6	IC3 [1:0]	00 Channel disabled		
5:4	IC2 [1:0]	01 SSI Mode		
3:2	IC1 [1:0]	10 Counter Mode		
1:0	IC0 [1:0]	11 Channel disabled **(the selection between normal SSI mode and 'SSI listen only' mode is done the Channel Control Register)**		

Table 3-13: Global Control Register

3.14 Interrupt Enable Register

For pending interrupts and interrupt acknowledge see the Interrupt Status Register

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved								Enable Digital Input IRQ						Enable	
	0	0	0	0	0	0	0	TIEN	DIEN5	DIEN4	DIEN3	DIEN2	DIEN1	DIEN0	CIEN5	CIEN4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Control Mode IRQ				Enable Match IRQ						Enable SSI IRQ					
	CIEN3	CIEN2	CIEN1	CIEN0	MIEN5	MIEN4	MIEN3	MIEN2	MIEN1	MIEN0	SIEN5	SIEN4	SIEN3	SIEN2	SIEN1	SIEN0

Bit	Symbol	Description	Access	Reset Value
31:25	-	Reserved, always reads as '0'	-	0
24	TIEN	Interval Timer Interrupt	R/W	0
23	DIEN5	Enable 24V digital input Interrupt	R/W	0
22	DIEN4	1 = Digital Input Interrupt enabled		
21	DIEN3	0 = Digital Input Interrupt disabled		
20	DIEN2	An interrupt will be generated on an (rising or falling) edge of the digital input.		
19	DIEN1			
18	DIEN0			
17	CIEN5	Enable Control Mode Interrupt	R/W	0
16	CIEN4	1 = Control Mode Interrupt enabled		
15	CIEN3	0 = Control Mode Interrupt disabled		
14	CIEN2	An interrupt will be generated on a control mode event.		
13	CIEN1			
12	CIEN0			
11	MIEN5	Enable Match Interrupt	R/W	0
10	MIEN4	1 = Counter Match Interrupt enabled		
9	MIEN3	0 = Counter Match Interrupt disabled		
8	MIEN2	An interrupt will be generated when the counter value matches the Counter Compare Register.		
7	MIEN1			
6	MIEN0			

Bit	Symbol	Description	Access	Reset Value
5	SIEN5	**Enable SSI Interrupt**	**R/W**	**0**
4	SIEN4	**1 = SSI Data Valid Interrupt enabled**		
3	SIEN3	**0 = SSI Data Valid Interrupt disabled**		
2	SIEN2	**An interrupt will be generated when a SSI transmission completes and the Busy status bit is set to '0'.**		
1	SIEN1			
0	SIEN0			

Table 3-14: Interrupt Enable Register

3.15 Interrupt Status Register

The interrupt status is updated only if the interrupt enable bit of the corresponding channel is set to '1'. Otherwise the interrupt status is read as '0'.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved								Digital Input IRQ Status						Control	
	0	0	0	0	0	0	0	TISTA	DISTA5	DISTA4	DISTA3	DISTA2	DISTA1	DISTA0	CISTA5	CISTA4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Mode IRQ Status				Match IRQ Status						SSI IRQ Status					
	CISTA3	CISTA2	CISTA1	CISTA0	MISTA5	MISTA4	MISTA3	MISTA2	MISTA1	MISTA0	SISTA5	SISTA4	SISTA3	SISTA2	SISTA1	SISTA0

Bit	Symbol	Description	Access	Reset Value
31:25	**-**	**Reserved, always reads as '0'**	**-**	**0**
24	**TISTA**	**Pending Interval Timer Interrupts (Read), Interrupt acknowledge (Write)** **On a read-access this bit indicates a pending Interval Timer interrupt. A '1' indicates a pending interrupt.** **The interrupt is acknowledged by writing a '1' to this bit.**	**R/C**	**0**
23	**DISTA5**	**Pending Digital Input Interrupts (Read), Interrupt acknowledge (Write)** **On a read-access these bits indicate the channels with pending digital input interrupts. A '1' indicates a pending interrupt.** **The interrupts are acknowledged by writing a '1' to the according bit.**	**R/C**	**0**
22	**DISTA4**			
21	**DISTA3**			
20	**DISTA2**			
19	**DISTA1**			
18	**DISTA0**			

Bit	Symbol	Description	Access	Reset Value
17	CISTA5	**Pending Control Mode Interrupts (Read),**	**R/C**	**0**
16	CISTA4	**Interrupt acknowledge (Write)**		
15	CISTA3	**On a read-access these bits indicate the channels with pending control mode interrupts. A '1' indicates a pending interrupt.**		
14	CISTA2			
13	CISTA1	**The interrupts are acknowledged by writing a '1' to the according bit.**		
12	CISTA0			
11	MISTA5	**Pending Match Interrupts (Read),**	**R/C**	**0**
10	MISTA4	**Interrupt acknowledge (Write)**		
9	MISTA3	**On a read-access these bits indicate the channels with pending match interrupts. A '1' indicates a pending interrupt.**		
8	MISTA2			
7	MISTA1	**The interrupts are acknowledged by writing a '1' to the according bit.**		
6	MISTA0			
5	SISTA5	**Pending SSI Interrupts (Read),**	**R/C**	**0**
4	SISTA4	**Interrupt acknowledge (Write)**		
3	SISTA3	**On a read-access these bits indicate the channels with pending SSI interrupts. A '1' indicates a pending interrupt.**		
2	SISTA2			
1	SISTA1	**The interrupts are acknowledged by writing a '1' to the according bit.**		
0	SISTA0			

Table 3-15: Interrupt Status Register

3.16 Test Register

This register allows quick testing of the RS422/TTL in- and outputs. To check the digital input levels read the Digital Input Register.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Reserved								SSI Clock Outputs						Channel	
	0	0	0	0	0	0	0	TSTEN	CLK5	CLK4	CLK3	CLK2	CLK1	CLK0	I5	B5

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	5	Channel 4			Channel 3			Channel 2			Channel 1			Channel 0		
	A5	I4	B4	A4	I3	B3	A3	I2	B2	A2	I1	B1	A1	I0	B0	A0

Bit	Symbol	Description	Access	Reset Value
31:25	**-**	**Reserved, always reads as '0'**	**-**	**0**
24	**TSTEN**	**Enable Test Output** **1 = Test Output enabled** **0 = Test Output disabled**	**R/W**	**0**
23	**CLK5**	**SSI Clock outputs.** **When TSTEN is '1' these bits will control the SSI clock outputs.**	**R/W**	**0**
22	**CLK4**			
21	**CLK3**			
20	**CLK2**			
19	**CLK1**			
18	**CLK0**			
17	**I5**	**Channel 6 Inputs**	**R**	**0**
16	**B5**			
15	**A5**			
14	**I4**	**Channel 4 Inputs**	**R**	**0**
13	**B4**			
12	**A4**			
11	**I3**	**Channel 3 Inputs**	**R**	**0**
10	**B3**			
9	**A3**			
8	**I2**	**Channel 2 Inputs**	**R**	**0**
7	**B2**			
6	**A2**			
5	**I1**	**Channel 1 Inputs**	**R**	**0**
4	**B1**			
3	**A1**			
2	**I0**	**Channel 0 Inputs**	**R**	**0**
1	**B0**			
0	**A0**			

Table 3-16: Test Register

4 PCI9030 Target Chip

4.1 PCI Configuration Registers (PCR)

4.1.1 PCI9030 Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits							PCI writeable	Initial Values (Hex Values)
	31 24	23 16		15 8		7 0			
0x00	Device ID			Vendor ID				N	013D 1498
0x04	Status			Command				Y	0280 0000
0x08	Class Code				Revision ID			N	118000 00
0x0C	BIST	Header Type		PCI Latency Timer		Cache Line Size		Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers							Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers							Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0							Y	FFFFFF00
0x1C	PCI Base Address 3 for Local Address Space 1							Y	00000000
0x20	PCI Base Address 4 for Local Address Space 2							Y	00000000
0x24	PCI Base Address 5 for Local Address Space 3							Y	00000000
0x28	PCI CardBus Information Structure Pointer							N	00000000
0x2C	Subsystem ID			Subsystem Vendor ID				N	000A 1498
0x30	PCI Base Address for Local Expansion ROM							Y	00000000
0x34	Reserved					New Cap. Ptr.		N	000000 40
0x38	Reserved							N	00000000
0x3C	Max_Lat	Min_Gnt		Interrupt Pin		Interrupt Line		Y[7:0]	00 00 01 00
0x40	PM Cap.			PM Nxt Cap.		PM Cap. ID		N	4801 48 01
0x44	PM Data	PM CSR EXT		PM CSR				Y	00 00 0000
0x48	Reserved	HS CSR		HS Nxt Cap.		HS Cap. ID		Y[23:16]	00 00 4C 06
0x4C	VPD Address			VPD Nxt Cap.		VPD Cap. ID		Y[31:16]	0000 00 03
0x50	VPD Data							Y	00000000

Table 4-1 : PCI9030 Header

4.1.2 PCI Base Address Initialization

PCI Base Address Initialization is scope of the PCI host software.

PCI9030 PCI Base Address Initialization:

1. Write 0xFFFF_FFFF to the PCI9030 PCI Base Address Register.

2. Read back the PCI9030 PCI Base Address Register.

3. For PCI Base Address Registers 0:5, check bit 0 for PCI Address Space.

    Bit 0 = '0' requires PCI Memory Space mapping

Bit 0 = '1' requires PCI I/O Space mapping

For the PCI Expansion ROM Base Address Register, check bit 0 for usage.

Bit 0 = '0': Expansion ROM not used

Bit 0 = '1': Expansion ROM used

4. For PCI I/O Space mapping, starting at bit location 2, the first bit set determines the size of the required PCI I/O Space size.

   For PCI Memory Space mapping, starting at bit location 4, the first bit set to '1' determines the size of the required PCI Memory Space size.

   For PCI Expansion ROM mapping, starting at bit location 11, the first bit set to '1' determines the required PCI Expansion ROM size.

   For example, if bit 5 of a PCI Base Address Register is detected as the first bit set to '1', the PCI9030 is requesting a 32 byte space (address bits 4:0 are not part of base address decoding).

5. Determine the base address and write the base address to the PCI9030 PCI Base Address Register. For PCI Memory Space mapping the mapped address region must comply with the definition of bits 3:1 of the PCI9030 PCI Base Address Register.

After programming the PCI9030 PCI Base Address Registers, the software must enable the PCI9030 for PCI I/O and/or PCI Memory Space access in the PCI9030 PCI Command Register (Offset 0x04). To enable PCI I/O Space access to the PCI9030, set bit 0 to '1'. To enable PCI Memory Space access to the PCI9030, set bit 1 to '1'.

Offset in Config.	Description	Usage
0x10	PCI9030 LCR's MEM	Used
0x14	PCI9030 LCR's I/O	Used
0x18	PCI9030 Local Space 0	Used
0x1C	PCI9030 Local Space 1	Not used
0x30	Expansion ROM	Not used

Table 4-2 : PCI9030 PCI Base Address Usage

4.2 Local Configuration Register (LCR)

After reset, the PCI9030 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

> The PCI base address for the PCI9030 Local Configuration Registers is PCI9030 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9030 PCI Configuration Register Space) or PCI9030 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9030 PCI Configuration Register Space).

> Do not change hardware dependent bit settings in the PCI9030 Local Configuration Registers.

Offset from PCI Base Address	Register	Value
0x00	Local Address Space 0 Range	0x0FFF_FFF0
0x04	Local Address Space 1 Range	0x0FFF_FFC0
0x08	Local Address Space 2 Range	0x0FFF_FE00
0x0C	Local Address Space 3 Range	0x0000_0000
0x10	Expansion ROM Range	0x0000_0000
0x14	Local Address Space 0 Local Base Address (Remap)	0x0000_0001
0x18	Local Address Space 1 Local Base Address (Remap)	0x0000_1001
0x1C	Local Address Space 2 Local Base Address (Remap)	0x0000_2001
0x20	Local Address Space 3 Local Base Address (Remap)	0x0000_0000
0x24	Expansion ROM Local Base Address (Remap)	0x0000_0000
0x28	Local Address Space 0 Bus Region Descriptor	0x1500_C0A0
0x2C	Local Address Space 1 Bus Region Descriptor	0x1580_C062
0x30	Local Address Space 2 Bus Region Descriptor	0x1502_4120
0x34	Local Address Space 3 Bus Region Descriptor	0x0000_0000
0x38	Expansion ROM Bus Region Descriptor	0x0000_0000
0x3C	Chip Select 0 Base Address	0x0000_0009
0x40	Chip Select 1 Base Address	0x0000_1021
0x44	Chip Select 2 Base Address	0x0000_2081
0x48	Chip Select 3 Base Address	0x0000_2181
0x4C	Interrupt Control/Status	0x0041
0x4E	Serial EEPROM Write-Protected Address Boundary	0x0030
0x50	PCI Target Response, Serial EEPROM Control, and Initialization Control	0x0078_0000
0x54	General Purpose I/O Control	0x026D_B6D2
0x70	Hidden1 Register for Power Management Data Select	0x0000_0000
0x74	Hidden 2 Register for Power Management Data Scale	0x0000_0000

Table 4-3 : PCI9030 Local Configuration Register

4.3 Configuration EEPROM

After power-on or PCI reset, the PCI9030 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x27 : PCI9030 PCI Configuration Register Values

- Address 0x28 to 0x87 : PCI9030 Local Configuration Register Values

- Address 0x88 to 0xFF : Reserved

See the PCI9030 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x013D	0x1498	0x0280	0x0000	0x1180	0x0000	s.b.	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x4801	0x0000	0x0000
0x20	0x0000	0x4C06	0x0000	0x0003	0x0FFF	0xFF00	0x0000	0x0000
0x30	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x50	0x4180	0x0020	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0081	0x0000	0x0000	0x0000	0x0000
0x70	0x0000	0x0000	0x0030	0x0041	0x807C	0x4000	0x0000	0x0240
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 4-4 : Configuration EEPROM TPMC317-xx

Subsystem-ID Value (Offset 0x0C):   TPMC317-10   0x000A

TPMC317-50   0x0032

4.4 **Local Software Reset**

The PCI9030 Local Reset Output LRESETo# is used to reset the on board local logic.

The PCI9030 local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the PCI9030 local configuration register CNTRL (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of '1' resets the PCI9030 and issues a reset to the Local Bus (LRESETo# asserted). The PCI9030 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI9030 PCI and Local Configuration Registers are not reset. The PCI9030 PCI Interface is not reset.

5 Configuration Hints

5.1 Big / Little Endian

- PCI – Bus (Little Endian)

Byte 0	AD[7..0]
Byte 1	AD[15..8]
Byte 2	AD[23..16]
Byte 3	AD[31..24]

- Every Local Address Space (0...3) and the Expansion ROM Space can be programmed to operate in Big or Little Endian Mode.

Big Endian		Little Endian	
32 Bit		**32 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
Byte 2	D[15..8]	Byte 2	D[23..16]
Byte 3	D[7..0]	Byte 3	D[31..24]
16 Bit upper lane		**16 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
16 Bit lower lane			
Byte 0	D[15..8]		
Byte 1	D[7..0]		
8 Bit upper lane		**8 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
8 Bit lower lane			
Byte 0	D[7..0]		

Figure 5-1 : Local Bus Little/Big Endian

Standard use of the TPMC317:

Local Address Space 0	32 bit bus in Little Endian Mode
Local Address Space 1	not used
Local Address Space 2	not used
Local Address Space 3	not used
Expansion ROM Space	not used

To change the Endian Mode use the Local Configuration Registers for the corresponding Space. Bit 24 of the according register sets the mode. A value of 1 indicates Big Endian and a value of 0 indicates Little Endian.

Use the PCI Base Address 0 + Offset or PCI Base Address 1 + Offset:

Short cut Offset	Name	
LAS0BRD	0x28	Local Address Space 0 Bus Region Description Register
LAS1BRD	0x2C	Local Address Space 0 Bus Region Description Register
LAS2BRD	0x30	Local Address Space 0 Bus Region Description Register
LAS3BRD	0x34	Local Address Space 0 Bus Region Description Register
EROMBRD	0x38	Expansion ROM Bus Region Description Register

You could also use the PCI - Base Address 1 I/O Mapped Configuration Registers.

6 Functional Description

Each channel can either work as a SSI interface or as an encoder / general purpose counter. The choice between both modes is made in the Global Control Register on a per channel base. In addition to this main functionality the TPMC317 offers one isolated 24V digital input per channel plus an interval timer.

6.1 SSI Short Description

The Synchronous Serial Interface (SSI) is based on two differential signal lines, CLOCK and DATA. The CLOCK line is an input, the DATA line is an output of the absolute encoder.

T = Clock Period
n = Number of Data Bits
tm= Recovery Time
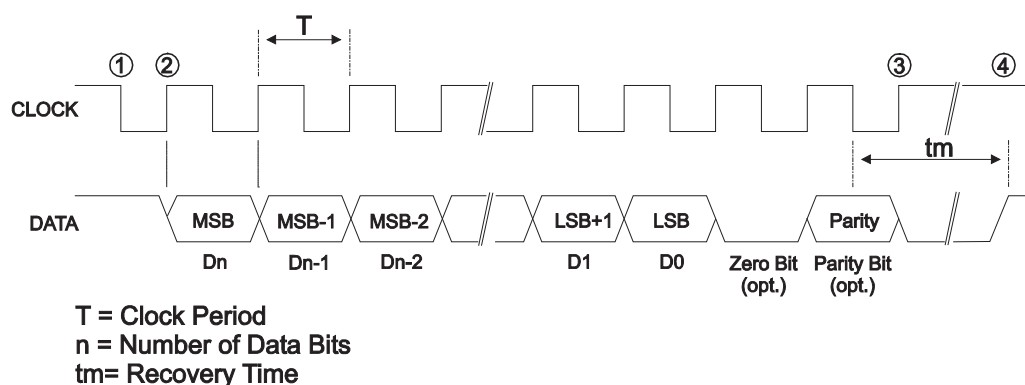
Figure 6-1 : SSI Timing Example

When not transmitting, the clock and data lines are high. To read out the positional data of an absolute encoder, the controller transmits a pulse train on the CLOCK line. The first falling edge of CLOCK ① latches the positional data of the absolute encoder. At the first rising edge of CLOCK ② the absolute encoder presents the most significant bit on the DATA line. On each subsequent rising edge in the CLOCK pulse train the next bit in order is transmitted to the controller.

In addition to the data bits the absolute encoder can transmit a parity bit for error detection. As an option a zero bit can be placed between the data and the parity bit.

After all bits are transmitted ③, the absolute encoder holds the data line low for 10-30µs (recovery time tm). After that the absolute encoder is ready for a new transmission ④. A new transmission must not started before ④.

The maximum achievable baud rate depends on the cable length. Cables are assumed to be twisted pair and screened.

Cable length (m)	Baud rate (kHz)
< 50	< 400
< 100	< 300
< 200	< 200
< 400	< 100

6.2 SSI Mode

6.2.1 Standard SSI Interface Controller Mode

In this mode a TPMC317 channel operates as a standard SSI interface controller. The SSI clock is an output and data signal is an input to the TPMC317.
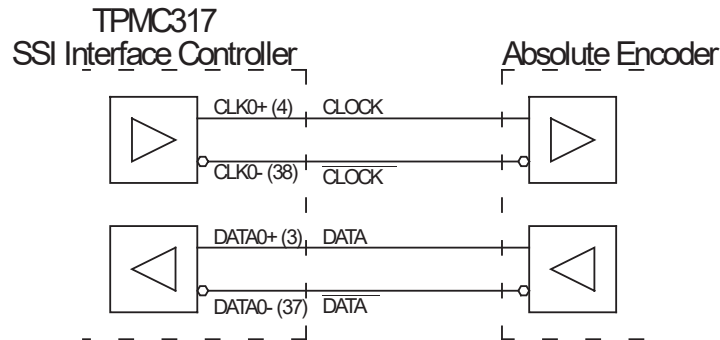

Figure 6-2 : Wiring Example: Channel 0, SSI Interface Controller Mode

This mode is enabled when the Interface Control in the Global Control Register is set to "01" and the MODE bit in the Control Register is set to '0':

Register	Symbol	Setting
Global Control Register	ICx	"01"
Control Register X	MODE	'0'

Table 6-1 : SSI Standard Mode Selection

In the Control Register the SSI interface must be set up, conforming to the settings required of the connected absolute encoder:

Register	Symbol	Setting
Control Register X	BC	Number of data bits
	CODE	Binary/Gray Code
	ZB	Additional Zero Bit
	EO	Even/Odd Parity
	PAR	Parity detection
	CR	Clock Rate

Table 6-2 : SSI Setup

A data transfer is initiated by a write to the Data Register. The SSI interface controller then generates a clock burst, on which the absolute encoder returns its positional data. The SSI Controller receives this data, processes it (parity check, gray- to binary code conversion) and indicates the end of the data transfer with the deassertion of the Busy bit. If enabled, an interrupt is asserted and the positional data can be read in the Data Register.

In this mode the "Read Error" status bit is always read as '0'.

6.2.2 SSI 'Listen only' Mode

In 'Listen only' Mode a TPMC317 channel listens to an existing SSI interface to observe the data transfer. Both the SSI clock and data signals are inputs to the TPMC317.
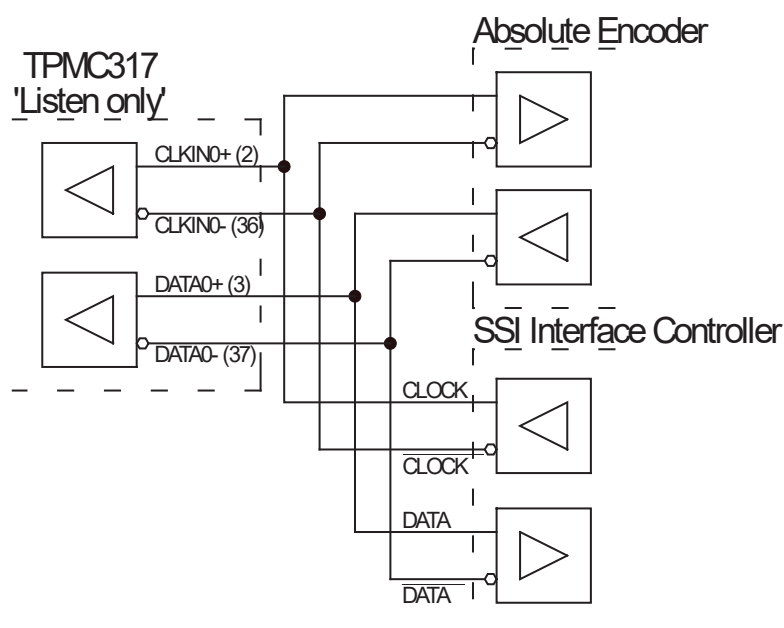

Figure 6-3 : Wiring Example: Channel 0, 'Listen only' Mode

This mode is enabled when the Interface Control in the Global Control Register is set to "01" and the MODE bit in the Control Register is set to '1'.

Register	Bit	Setting
Global Control Register	ICx	"01"
Control Register X	MODE	'1'

Table 6-3 : SSI 'Listen only' Mode Selection

In the Control Register the SSI interface must be set up, conforming to the settings required of the observed SSI interface:

Register	Symbol	Setting
Control Register X	BC	Number of data bits
	CODE	Binary/Gray Code
	ZB	Additional Zero Bit
	EO	Even/Odd Parity
	PAR	Parity detection
	CR	-

Table 6-4 : SSI 'Listen only' Setup

The clock rate setting in the Control Register is 'don't care'; the clock rate of the observed SSI interface will be detected automatically.

After the Control Register is set up, the channel listens (indicated by Busy = '1').

A data transfer is initiated by the observed SSI interface. The positional data will be received and processed (parity check, gray- to binary code conversion) and the end of the data transfer is indicated with the deassertion of the Busy bit. If enabled, an interrupt is asserted and the positional data can be read in the Data Register.

Reading the Data Register will set the Busy bit to '1' and the channel is listening again.

> **Note that in this mode the clock rate setting in the Control Register is ignored; the Clock Rate will be detected automatically. Writes to the Data Register are also ignored for channels in this mode.**

In case of a partial transmission a read error will be issued in the Status Register. To detect read errors, the width of the first SSI clock pulse is measured to detect the clock rate. This clock rate is multiplied by 4 and used as the initial value for a watchdog timer. Every new received bit resets the watchdog timer, until either the programmed data word length is reached (successful read) or a timeout occurs (read error). In case of a timeout the Read Error bit is set to '1'. Depending on the BREAK setting in the Control Register the channel ignores a read error and continues listening or it stops to listen.

Reasons for a read error are:

- The number of data bits set in the control register does not match the actual size of the received transmission.

- Only a partial transmission was monitored (this could happen when the mode is switched and a transmission is in progress on the observed SSI interface).

In the case that a SSI communication is in progress when the mode is switched to 'Listen only', a read error will be issued for the first reading.

6.2.3 SSI Mode behavior differences

	Standard SSI Interface Mode	'Listen only' Mode
Control Register	Control Register SSI bits fully used Bit 14 (MODE) is set to '0'	Clock rate setting in Control Register is 'don't care' Bit 14 (MODE) is set to '1'
Status Register	Busy bit = '1' during transmission	Busy bit = '1' during transmission or after the data word was read (channel is listening again)
Read Error Bit	Read Error bit is always '0'	Read Error bit is set to '1' on a erroneous transmission
Connections	Connect external SSI data outputs to TPMC317 'DATA' inputs. Connect external SSI Clock inputs to TPMC317 'CLK OUT' outputs.	Connect external SSI data to TPMC317 'DATA' inputs. Connect external SSI clock to TPMC317 'CLK IN' inputs.
Data Transfer Start	Data transfer is initiated by a write to the Data Register or a Multiple Channel Read	Data transfer is initiated by external SSI interface controller

Table 6-5 : Mode behavior differences

6.3 Counter Mode

The TPMC317 counter offers 4 input modes, 2 special count modes and 8 index control modes.

6.3.1 Input Modes

The input mode determines how the counter interprets the A and B input lines:

Input Mode	A Input	B Input	I Input
Timer	not used	not used	Available for Input Control Modes
Direction Count	Count	Count direction (up/down)	
Up/Down Count	Count UP	Count DOWN	
Quadrature Count	Quadrature A	Quadrature B	

Table 6-6 : Input Modes

Changing the input mode does not affect the counter reading. If no input mode is selected, the counter is disabled.

6.3.1.1 Timer Mode

In Timer mode the counter uses an internal clock prescaler as input:

Bits	Prescaler	Clock frequency
00	1x	32 MHz
01	2x	16 MHz
10	4x	8 MHz
11	8x	4 MHz

Table 6-7: Clock Prescaler

6.3.1.2 Direction Count

The counter acts as up/down counter. Counting pulses are generated when a transition from low to high of the A-input is detected. The B-input determines the count direction.

B-input	Count Direction
0	Down
1	Up

Table 6-8: Count Directions

6.3.1.3 Up/Down Count

The counter acts as up-/down counter. Counting pulses are generated when a transition from low to high of either the A- or the B-input is detected. The A-input counts up, the B-input counts down. Simultaneous transitions on the A- and B-input do not generate a counting pulse.

6.3.1.4 Quadrature Count

The counter acts as quadrature counter. A-input is quadrature input A, B-input is quadrature input B. The quadrature inputs can be interpreted as 1x, 2x or 4x counting. 1x lets the counter count once for each full cycle of the quadrature inputs, 2x lets the counter count once for each half cycle of the quadrature inputs and 4x lets the counter count once for each quarter cycle of the quadrature inputs. The count direction (increase or decrease) is determined by the relative phase of the A- and B-signals.

The maximum input frequency is 2 MHz. In 4x mode the counter counts with max. 8 MHz.
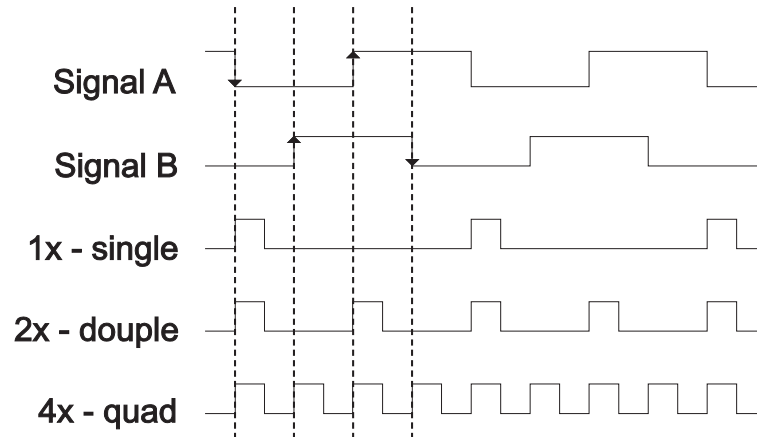

Figure 6-4: Quadrature Signals

6.3.2 Special Count Modes

In normal operation, the counter is a cycling counter. Two additional special count modes are available. The Count Modes are available for every Input Mode.

6.3.2.1 Divide-by-N

The counter is enabled in the Control Register and will run until it is disabled. The counter is loaded with the content of the preload register every time the counter creates a borrow or a carry.

6.3.2.2 Single Cycle

The counter is enabled in the Control Register and will start on following events:

- A manual preload or reset in the Counter Command Register

- A manual counter preload in the Global Control Register

- A control mode event in 'Load on I' or 'Reset on I' mode.

The counter will stop when it creates a borrow or a carry.

6.3.3 Index Control Modes

The Index Control Mode determines how events on the I-input are interpreted. With the exception of the 'Gate on I' mode, all modes react on a level change on the I-input. Due to the digital input filtering, a change in the input level is only detected, when the input line is stable for at least 100ns. The following table gives an overview of the index control mode events.

Index Control Mode	Polarity	
	high active (POL = 0)	low active (POL = 1)
No I-Control	-	-
Load on I	Rising edge	Falling edge
Latch on I	Rising edge	Falling edge
Gate on I	High level	Low Level
Reset on I	Rising edge	Falling edge
Reference Mode	Rising edge	Falling edge
Auto Reference Mode	Rising edge	Falling edge
Index Mode	Rising edge	Falling edge

Table 6-9: Index Control Mode events

The control modes 'Reference Mode', 'Auto Reference Mode' and 'Index Mode' are only valid when the input mode is quadrature count. They control the counter with the encoder index input in cooperation with a reference switch connected to the isolated 24V digital input.

An interrupt can be generated on a control mode event. This is only available for the Load-, Latch-, Gate- and Reset on I modes.

Index Control Mode	Interrupt generation
No Control Mode	No interrupt
Load Mode Latch Mode Reset Mode	Control mode event
Gate Mode	Gate closed

Table 6-10: Index control mode interrupt generation

6.3.3.1 No I-Control

In this mode the I-input is ignored.

6.3.3.2 Load on I

An event on the I-input loads the counter with the content of the Counter Preload Register. If the 'Single Cycle' mode is active, the event on the I-input will start the counter. The counter can also be preloaded by writing '1' to the 'Load Counter' (LCNT) bit in the Counter Command Register.

This control mode can be used to establish a known reference position in a mechanical system.

6.3.3.3 Latch on I

An event on the I-input loads and locks the Data Register with the actual counter value (see chapter 'Data Register Lock' for details. It will remain latched until the Data Register is read or the latch is released with the CDLT bit in the Status Register.

When a 'Latch on I' event occurs while the Data Register Lock is still active, the data in the Data Register will be retained and the Data Register Lock Overflow (OVFL) will be set to indicate that data was lost.

This control mode can be used to capture a position in a mechanical system.

6.3.3.4 Gate on I

The signal level on the I-input enables or disables counting. Remember that in this mode the I-input is level sensitive.

I-Input	Counter
0	Disabled
1	Enabled

Table 6-11: Gate Mode

In this mode an interrupt is generated (if enabled) when the gate is being closed (I-Input transition from '1' to '0').

When a signal with constant frequency is connected to the A- and B-inputs, this control mode can be used for impulse width measurements.

6.3.3.5 Reset on I

An event on the I-input resets (clears) the counter. If the 'Single Cycle' mode is active, the event on the I-input starts the counter.

The counter can also be reset by writing '1' to the 'Reset Counter' (RCNT) bit in the Counter Command Register.

This control mode can be used to establish a known home or reference position in a mechanical system.

6.3.3.6 Reference Mode

This mode controls the counter with the (isolated 24V digital) reference input and the encoder index signal. A specified reference input signal and a following index impulse produce a counter preload. The host software must set the motion direction during such a reference access to backwards.

The following figure shows the two normal preload accesses. An encoder motion area with eight index pulses and the corresponding reference input is described as an example. Two different 'start positions' (1a and 1b) are shown:

Position 1a

Direction is forward and the reference input is active. The host software must move into the area where the reference input is inactive. Now the direction must be changed. The next index pulse after entering the area with reference input active triggers the preload function for the counter.

Position 1b

Direction is backwards and the reference input is inactive. The host software must move further backwards, and after entering the area with reference input active the next index pulse triggers the preload function for the counter.
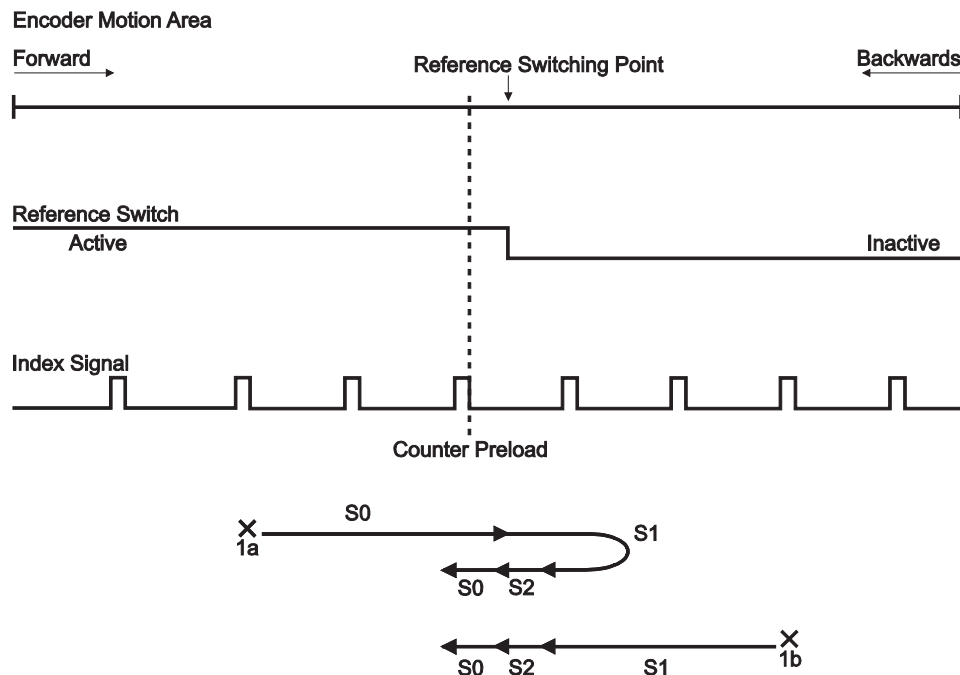

Figure 6-5: Reference mode preload example

A correct execution of the reference function can be monitored in the Control Register. After successful execution the mode is reset from Reference Mode to No I-Control Mode.

6.3.3.7 Auto Reference Mode

This mode is the automation of the Reference Mode. Every time the reference switching point and a following index pulse are crossed during backward direction, a new preload is generated. In "Auto Reference Mode" there is no change of the Index Control Mode in the Control Register!

6.3.3.8 Index Mode

In this mode the reference input is not used. Only the index impulse produces a counter preload. After setting this mode the next occurrence of the index signal independent from direction will preload the counter. A correct execution of this preload function can be monitored in the Control Register. After successful execution the mode is reset from Index Mode to No I-Control Mode.

6.3.4 Data Register Lock

The Data Register is loaded and locked with the actual counter value on following conditions:

- Latch in I Mode

- Multiple channel read

The Data Register is locked until following conditions are met:

- A read-access to the Data Register

- A write '1' to the RCNT bit in the Counter Command Register

Until the lock is released, the Data Register will not load again. The status of the Data Register lock can be monitored in the Status Register (DRL). When the lock is released, the Data Register retains its value until it is loaded again.

When a Multiple channel read is issued or a Latch Mode event occurs while a Data Register is locked, the Data Register content will be retained and the Data Register Lock Overflow (OVFL) will be set to indicate that data was lost.

6.4 Multiple Channel Read

The Multiple Channel Read option is enabled in the Global Control Register. A Multiple Channel Read is triggered by writing '1' to the MCRTR-bit. Alternatively the interval timer can be used to trigger a multiple channel read. For Counter mode the Multiple Channel Read latches the enabled counter channels. For SSI mode the Multiple Channel Read starts a conversion for the enabled SSI channels.

The data of counter channels is instantly available. SSI channels need time for the conversion to complete. To indicate that all data is available, the MCRST bit in the Global Control Register will be set to '1'. This bit will stay '1' until the Data Registers of all enabled channels were read. Then it changes back to '0'. To reset a Multiple Channel Read sequence beforehand, write '1' to the MCRST bit.

	SSI	Counter	SSI & Counter
Data availability	When all channel conversions are complete	Instantly	SSI: When all channel conversions are completed Counter: Instantly
Data availability indication	MCRST = '1'	MCRST = '1'	MCRST = '1' Counter data may already be read before MCRST = '1'

Table 6-12: Multiple Channel Read data availability

Example:

Channels 1-3 are configured for SSI mode, channels 4-6 are configured for counter mode. Channels 1, 4 and 6 are enabled for Multiple Channel Read. A write to the MCRTR bit starts the Multiple Channel Read. Channel 1 starts a conversion and the data of channels 4 and 6 are latched. The data of the enabled counter channels is instantly available and can be read at once. The SSI data is not available until MCRST is set to '1'. When all enabled channels were read, MCRST is reset to '0'.

There is no designated interrupt to indicate the completion of a Multiple Channel Read. Alternatively an interrupt can be set up for the SSI channel that takes the longest time to complete a conversion. If only counter channels are read, an interrupt is not necessary because the counter data is instantly available.

6.5 Interval Timer

The interval timer is a 16 bit preloadable counter with a programmable clock rate. On activation the counter loads from the Interval Timer Preload Register und starts counting down. When the counter reaches zero, it generates an interrupt (if enabled), is automatically preloaded again and continues counting.

With the 16 bit preload register and the programmable clock interval, interval times up to 65ms are possible. Calculate the interval times using the following formula:

Interval Time = Value of Interval Timer Preload Register * Clock period

ITDIV	Clock Frequency	Clock Period
00	8 MHz	125ns
01	4 MHz	250ns
10	2 MHz	500ns
11	1 MHz	1µs

Table 6-13: Interval Timer Clock Periods

The interval timer can be used as a reference timer in closed loop applications or as a trigger for a multiple channel read.

6.6 Isolated 24V Digital Inputs

The TPMC317 offers one isolated digital 24V input per channel. The inputs are electronically debounced. Each digital 24V input can generate an interrupt, triggered on rising or falling edge. Depending on the selected counter reference mode the input can be used as a general purpose input or as a reference input.

6.7 SSI/Counter Input Filtering

To avoid false counts caused by noisy input signals, the A- B- and I-inputs are digitally filtered. A change in the input level is only detected, when the input line is stable for at least 100ns.

7 Hardware Interface

7.1 Encoder/Counter Input Wiring

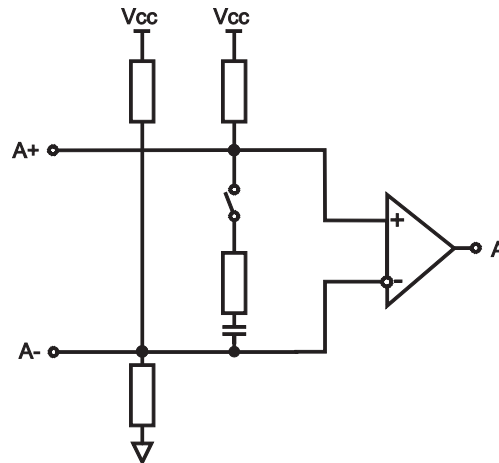The following schematic shows the principle input wiring for one encoder signal.

Figure 7-1 : Input Wiring

The 120Ω termination resistor is switchable via DIP switches. For single-ended/TTL signals the switch must be left open (default), for differential/RS422 signals the switch should be closed.

7.1.1 Termination Resistor DIP Switches

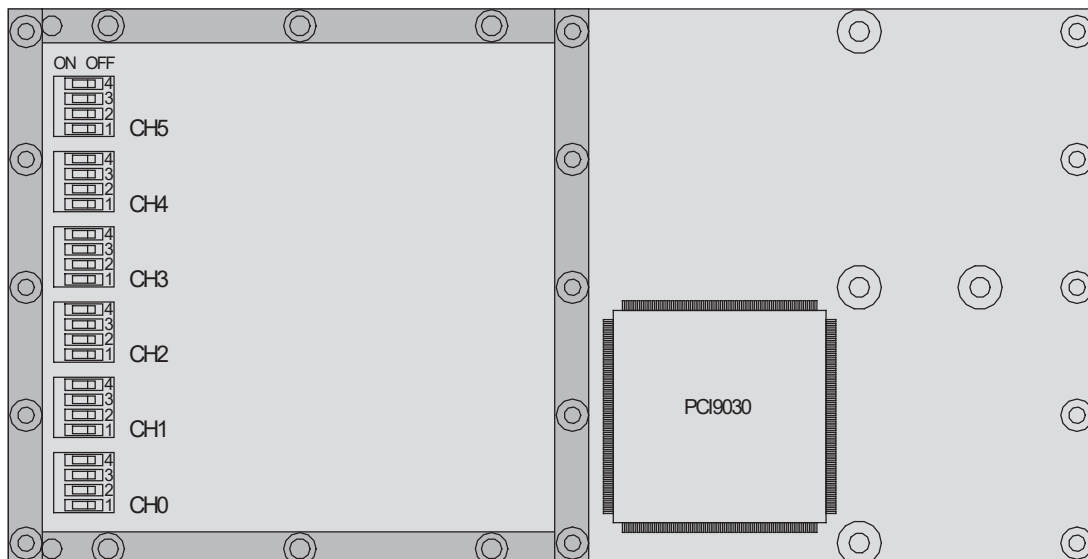The termination DIP switches are located near the I/O connector (refer to the following figure).

Figure 7-2 : Termination Resistor DIP Switches

Each channel has a dedicated DIP switch for its input signals.

Switch	Signal
1	ENC_A
2	ENC_B
3	ENC_I
4	not used

Table 7-1 : DIP Switch Signal Assignment

Switch Setting	Termination
ON	Enabled
OFF	Disabled

Table 7-2 : DIP Switch Settings

The Factory setting of the DIP switch is OFF, hence the input configuration is single-ended/TTL.

7.1.2 Single-Ended / TTL

The following schematic shows the principle input wiring for one single-ended/TTL encoder signal. For single-ended/TTL input, leave the inverting input (A-) open and connect the TTL signal to the noninverting input (A+).

The120Ω termination resistor must be switched off when using single-ended/TTL input signals!
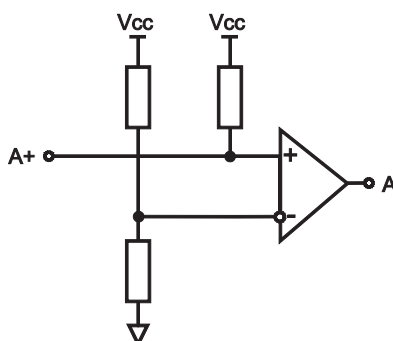

Figure 7-3 : Single-ended Input Wiring

The switching point lies at approx. 1.6V, with a hysteresis of about 0.4 mV.

7.1.3 Differential / RS422

The following schematic shows the principle input wiring for one differential/RS422 encoder signal. RS422 input signals should be terminated. The encoder input is fail-safe based, so that unused inputs can be left open.
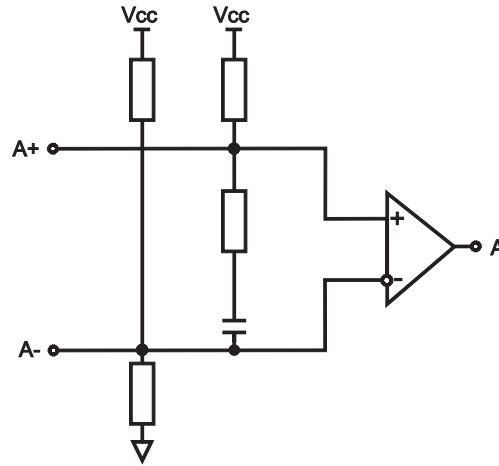

Figure 7-4 : Differential Input Wiring

It is recommended to terminate differential/RS422 input signals.

7.2   Clock Output Wiring

The TPMC317 adheres to the original SSI specification that featured galvanic insulation with optocouplers. Therefore, the clock inputs in the sensor did not need a ground reference. Nowadays the sensor's clock inputs are often build with conventional RS422 receivers, which do need a ground reference. The TPMC317's clock drivers are referenced to circuit ground, which is not available at the connector. In this case the clock's ground reference must be connected to the system ground, which must be available somewhere in the chassis.
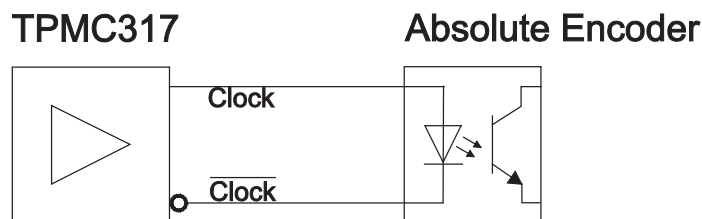

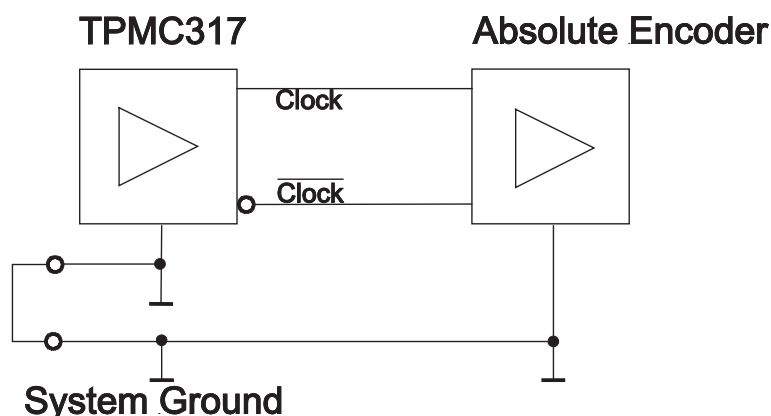Figure 7-5 : Clock Output Wiring with Optocoupler Input

Figure 7-6 : Clock Output Wiring with Differential Receiver Input

GND_I is an isolated input ground that can not be used as the clock output ground reference.

7.3   Digital Input Characteristics

The TPMC317 offers one digital 24V input per channel which is galvanically isolated by optocouplers. A high performance input circuit ensures a defined switching point and polarization protection against confusing the pole. The inputs are electronically debounced. Each of the four digital 24V inputs can generate an interrupt, triggered on rising or falling edge. Depending on the selected reference mode the input can be used as general purpose input or as reference input.

Parameter	Unit	Typical
Input isolation	-	Optocoupler as galvanic isolation
Input voltage	V	24
Input current	mA	4.2 (at 24V input voltage)
Switching level	V	12 (min. 7.5, max. 14)

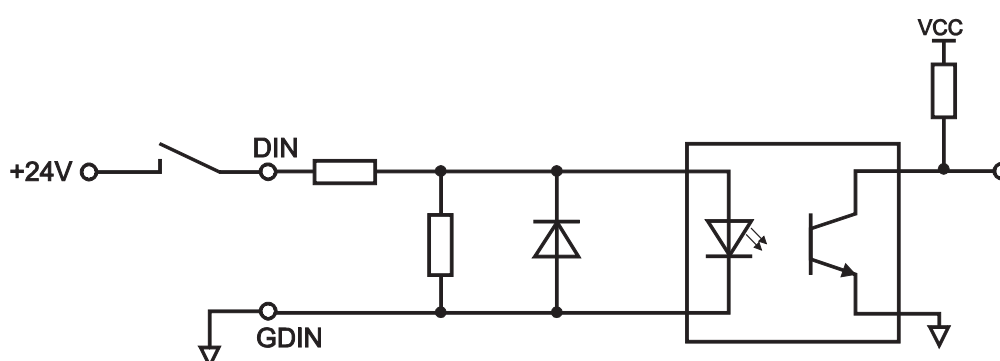Table 7-3 : Digital Input Characteristics

Figure 7-7 : Digital Input Wiring

8 Pin Assignment – I/O Connector

8.1 P14 Back I/O Connector

The TPMC317 P14 Back I/O connector is Standard 64 pin Mezzanine Connector.

Pin	SSI Signal	Counter Signal	Pin	SSI Signal	Counter Signal
1	-	ENC_A0+	2	-	ENC_A0-
3	CLK IN0+	ENC_B0+	4	CLK IN0-	ENC_B0-
6	DATA0+	ENC_I0+	6	DATA0-	ENC_I0-
7	CLK OUT0+	-	8	CLK OUT0-	-
9	-	ENC_A1+	10	-	ENC_A1-
11	CLK IN1+	ENC_B1+	12	CLK IN1-	ENC_B1-
13	DATA1+	ENC_I1+	14	DATA1-	ENC_I1-
15	CLK OUT1+	-	16	CLK OUT1-	-
17	-	ENC_A2+	18	-	ENC_A2-
19	CLK IN2+	ENC_B2+	20	CLK IN2-	ENC_B2-
21	DATA2+	ENC_I2+	22	DATA2-	ENC_I2-
23	CLK OUT2+	-	24	CLK OUT2 -	-
25	-	ENC_A3+	26	-	ENC_A3-
27	CLK IN3+	ENC_B3+	28	CLK IN3-	ENC_B3-
29	DATA3+	ENC_I3+	30	DATA3-	ENC_I3-
31	CLK OUT3+	-	32	CLK OUT3-	-
33	-	ENC_A4+	34	-	ENC_A4-
35	CLK IN4+	ENC_B4+	36	CLK IN4-	ENC_B4-
37	DATA4+	ENC_I4+	38	DATA4-	ENC_I4-
39	CLK OUT4+	-	40	CLK OUT4-	-
41	-	ENC_A5+	42	-	ENC_A5-
43	CLK IN5+	ENC_B5+	44	CLK IN5-	ENC_B5-
45	DATA5+	ENC_I5+	46	DATA5-	ENC_I5-
47	CLK OUT5+	-	48	CLK OUT5-	-
49	GND_I		50	GND_I	
51	GND_I		52	GND_I	
53	24V Digital Input 0		54	24V Digital Input 0 GND	
55	24V Digital Input 1		56	24V Digital Input 1 GND	
57	24V Digital Input 2		58	24V Digital Input 2 GND	
59	24V Digital Input 3		60	24V Digital Input 3 GND	
61	24V Digital Input 4		62	24V Digital Input 4 GND	
63	24V Digital Input 5		64	24V Digital Input 5 GND	

Table 8-1 : Pin Assignment P14 Back IO Connector