The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC378

Conduction cooled 8 channel isolated RS422 interface

Version 1.0

User Manual

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TPMC378-10R

Conduction cooled 8 channel isolated RS422 interface, P14 I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial Issue	April 2014
1.0.1	Corrected “Termination” description	July 2014

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1 Product Description

The TPMC378 is a conduction cooled single-width 32 bit PMC module offering 8 channels of high performance RS422 asynchronous serial interface with P14 I/O. Each of the eight channels is isolated from the system and against each other by isolated transceivers with integrated DC/DC converters.

Each RS422 channel supports a four wire interface (RX+, RX-, TX+, TX-) plus ground (GND). Two channels additionally support flow control with RTS+/- and CTS+/-.

Each channel has 64 byte transmit and receive FIFOs to significantly reduce the overhead required to provide data to and get data from the transmitters and receivers. The FIFO trigger levels are programmable and the baud rate is individually programmable up to 5.5296 Mbps for RS422 channels. The UART offers readable FIFO levels.

All channels generate interrupts on PCI interrupt INTA. For fast interrupt source detection the UART provides a special Global Interrupt Source Register.

All serial channels use ESD protected transceivers. ESD protection is up to ±15KV.

The TPMC378 can operate with 3.3V and 5.0V PCI I/O signaling voltage.

Software Support (TDRV002-SW-xx) for different operating systems is available.

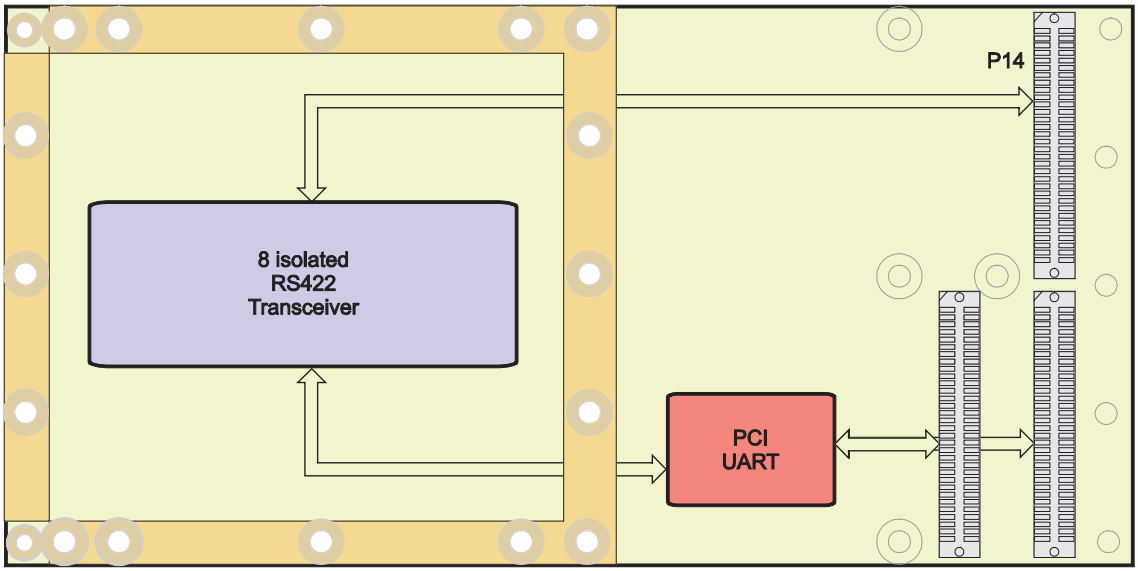

Figure 1-1: Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	Conduction Cooled PCI Mezzanine Card (PMC) Interface confirming to ANSI/VITA 20-2001 (R2005) Single Size	
Electrical Interface	PCI Rev. 2.3 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip	XR17D158 (Exar)	
Transceiver	ADM2582E (Analog Devices)	
I/O Interface		
Interface Type	Asynchronous serial interface	
Number of Channels	8	
Physical Interface	RS422	
Serial Channel I/O Signals	TxD+/-, RxD+/-, GND (2 channels: RTS+/-, CTS+/-)	
Termination	120Ω between RxD+ and RxD- of each channel (2 channels: also between CTS+, CTS-)	
Programmable Baud Rates	up to 5.5296 Mbps	
ESD Protection	±15kV - Human Body Model	
I/O Connector	PMC P14 I/O (64 pin Mezzanine Connector)	
Physical Data		
Power Requirements	180 mA typical @ +5V DC 650 mA typical @ +5V DC	(no load) (with loopback: CH0 connected to CH1, CH2 connected to CH3, …)
Temperature Range	Operating Storage	-40 °C to +85 °C -55 °C to +125 °C
MTBF	1.000.000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	64 g	

Table 2-1 : Technical Specification

3 Local Space Addressing

3.1 XR17D158 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the XR17D158 local spaces.

XR17D158 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0 (0x10)	MEM	4096	32	BIG	Device Configuration Space

Table 3-1 : XR17D158 Local Space Configuration

3.2 Device Configuration Space

PCI Base Address: XR17D158 PCI Base Address 0 (Offset 0x10 in PCI Configuration Space).

Device Configuration Space Content	PCI Address	Size (Bit)
UART 0 Register Set	PCI Base Address 0 + (0x0000 to 0x007F)	32
Device Configuration Registers	PCI Base Address 0 + (0x0080 to 0x009F)	32
UART 0 Register Set	PCI Base Address 0 + (0x0100 to 0x01FF)	32
UART 1 Register Set	PCI Base Address 0 + (0x0200 to 0x03FF)	32
UART 2 Register Set	PCI Base Address 0 + (0x0400 to 0x05FF)	32
UART 3 Register Set	PCI Base Address 0 + (0x0600 to 0x07FF)	32
UART 4 Register Set	PCI Base Address 0 + (0x0800 to 0x09FF)	32
UART 5 Register Set	PCI Base Address 0 + (0x0A00 to 0x0BFF)	32
UART 6 Register Set	PCI Base Address 0 + (0x0C00 to 0x0DFF)	32
UART 7 Register Set	PCI Base Address 0 + (0x0E00 to 0x0FFF)	32

Table 3-2 : Device Configuration Space

All registers can be accessed in 8, 16 or 32 bit width with exception to one special case: When reading the receive data together with its LSR register content, the host must read them in 16 or 32 bits format in order to maintain integrity of the data byte with its associated error flags.

3.2.1 UART Register Sets

The Device Configuration Space provides a register set for each of the 8 UARTs.

UART Register Set	Register Set Offset
Serial Channel 0	0x0000
Serial Channel 1	0x0200
Serial Channel 2	0x0400
Serial Channel 3	0x0600
Serial Channel 4	0x0800
Serial Channel 5	0x0A00
Serial Channel 6	0x0C00
Serial Channel 7	0x0E00

Table 3-3 : UART Register Set Offset

Offset Address	Description	Access	Data Width
0x000 – 0x00F	UART Channel Configuration Registers First 8 registers are 16550 compatible	R/W	8, 16, 32
0x010 – 0x07F	Reserved	-	-
0x080 – 0x093	Channel 0: Device Configuration Registers All other channels: Reserved	R/W	8, 16, 32
0x094 – 0x0FF	Reserved	-	-
0x100	Read FIFO – 64 bytes of RX FIFO data	R	8, 16, 32
	Write FIFO – 64 bytes of TX FIFO data	W	8, 16, 32
0x140 – 0x17F	Reserved	-	-
0x180 – 0x1FF	Read FIFO with errors – 64 bytes of RX FIFO data + LSR	R	16, 32

Table 3-4 : UART Register Set

3.2.2 Device Configuration Registers

The Device Configuration Registers control general operating conditions and monitor the status of various functions. This includes a 16 bit general purpose counter, multipurpose input/outputs, sleep mode, soft-reset and device identification, and revision. They are embedded inside the UART 0 Register Set.

Address	Register	Description	Access	Reset Value
0x080	INT0 [7:0]	Channel Interrupt Indicator	R	0x00
0x081	INT1 [15:8]	Interrupt Source Details	R	0x00
0x082	INT2 [23:16]		R	0x00
0x083	INT3 [31:24]		R	0x00
0x084	TIMERCNTL	Timer Control Register	R/W	0x00
0x085	TIMER	Reserved	-	0x00
0x086	TIMERLSB	Programmable Timer Value	R/W	0x00
0x087	TIMERMSB		R/W	0x00
0x088	8XMODE	Sampling Rate Select	R/W	0x00
0x089	REGA	Reserved	-	0x00
0x08A	RESET	UART Reset	W	0x00
0x08B	SLEEP	UART Sleep Mode Enable	R/W	0x00
0x08C	DREV	Device Revision	R	0x01
0x08D	DVID	Device Identification	R	0x28
0x08E	REGB	Simultaneous UART Write & EEPROM Interface	W	0x00
0x08F	MPIOINT	MPIO Interrupt Mask	R/W	0x00
0x090	MPIOLVL	MPIO Level Control	R/W	0x00
0x091	MPIO3T	MPIO Output Pin Tri-state Control	R/W	0x00
0x092	MPIOINV	MPIO Input Polarity Select	R/W	0x00
0x093	MPIOSEL	MPIO Input/Output Select	R/W	0xFF

Table 3-5 : Device Configuration Registers

For a detailed description of the Device Configuration Registers please refer to the XR17D158 data sheet which is available on the Exar website (www.exar.com).

3.2.3 UART Channel Configuration Registers

Each UART channel has its own set of internal UART configuration registers for its own operation control and status reporting. The following table provides the register offsets within a register set, access types and access control:

Address	Comment	Description	Access	Reset Value
16550 Compatible				
0x00	LCR[7] = 0	RHR – Receive Holding Register THR – Transmit Holding Register	R W	0xXX
	LCR[7] = 1	DLL – Baud Rate Generator Divisor Latch Low	R/W	0xXX
0x01	LCR[7] = 0	IER – Interrupt Enable Register	R/W	0x00
	LCR[7] = 1	DLM – Baud Rate Generator Divisor Latch High	R/W	0xXX
0x02		ISR – Interrupt Status Register	R	0x01
		FCR – FIFO Control Register	W	0x00
0x03		LCR – Line Control Register	R/W	0x00
0x04		MCR – Modem Control Register	R/W	0x00
0x05		LSR – Line Status Register	R	0x60
		Reserved	W	
0x06		MSR – Modem Status Register	R	0xX0
		MSR – Auto RS485 Delay (not supported by the TPMC378)	W	
0x07	User Data	SPR – Scratch Pad Register	R/W	0xFF
Enhanced Registers				
0x08		FCTR – Feature Control Register	R/W	0x00
0x09		EFR – Enhanced Function Register	R/W	0x00
0x0A		TXCNT – Transmit FIFO Level Counter	R	0x00
		TXTRG – Transmit FIFO Trigger Level	W	
0x0B		RXCNT – Receiver FIFO Level Counter	R	0x00
		RXTRG – Receiver FIFO Trigger Level	W	
0x0C		Xchar – Xon, Xoff Received Flags	R	0x00
		Xoff-1 – Xoff Character 1	W	
0x0D		Reserved	R	0x00
		Xoff-2 – Xoff Character 2	W	
0x0E		Reserved	R	0x00
		Xon-1 – Xon Character 1	W	
0x0F		Reserved	R	0x00
		Xon-2 – Xon Character 2	W	

Table 3-6 : UART Channel Configuration Registers

The address for a UART Channel Configuration Register x in a UART Register Set for channel y is:

PCI Base Address 0 (PCI Base Address for the UART Register Space)

+ UART Register Set Offset for channel y

+ Register Offset for register x

Addressing example:

The address for the LCR register of UART channel 5 is:

PCI Base Address (PCI Base Address for the Device Configuration Space)

+ 0x0A00 (Offset of the UART register set for serial channel 5)

+ 0x0003 (Offset of the LCR register within a UART register set)

For a detailed description of the serial channel registers please refer to the XR17D158 data sheet which is available on the Exar website (www.exar.com).

4 XR17D158 Target Chip

4.1 PCI Configuration Registers (PCR)

4.1.1 XR17D158 Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits								PCI writeable	Initial Values (Hex Values)
	31	24	23	16	15	8	7	0		
0x00	Device ID				Vendor ID				N	017A 1498
0x04	Status				Command				Y	0080 0000
0x08	Class Code						Revision ID		N	070200 ??
0x0C	BIST		Header Type		PCI Latency Timer		Cache Line Size		Y[7:0]	00 00 00 00
0x10	Memory Base Address Register (BAR)								Y	FFFFF000
0x14	I/O Base Address Register (Unimplemented)								N	00000000
0x18	Base Address Register 0 (Unimplemented)								N	00000000
0x1C	Base Address Register 1 (Unimplemented)								N	00000000
0x20	Base Address Register 2 (Unimplemented)								N	00000000
0x24	Base Address Register 3 (Unimplemented)								N	00000000
0x28	Reserved								N	00000000
0x2C	Subsystem ID				Subsystem Vendor ID				N	s.b. 1498
0x30	PCI Base Address for Local Expansion ROM								Y	00000000
0x34	Reserved						New Cap. Ptr.		N	000000 40
0x38	Reserved								N	00000000
0x3C	Max_Lat		Min_Gnt		Interrupt Pin		Interrupt Line		Y[7:0]	00 00 01 00

Table 4-1 : PCI Header

Device ID:	0x017A	TPMC377
Vendor ID:	0x1498	TEWS TECHNOLOGIES
Revision ID:		XR17D158 silicon revision
Subsystem ID:	0x000A	-10
Sybsystem Vendor ID:	0x1498	TEWS TECHNOLOGIES

4.2 Configuration EEPROM

After power-on or PCI reset, the XR17D158 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Vendor ID
- Vendor Device ID
- SubSystem Vendor ID
- SubSystem Device ID

See the XR17D158 Manual for more information.

Address	Configuration Register	Configuration Register Offset	Value
0x00	Vendor ID	0x02	0x1498
0x01	Device ID	0x00	0x0177
0x02	Subsystem Vendor ID	0x2E	0x1498
0x03	Subsystem ID	0x2C	s.b.

Table 4-2 : Configuration EEPROM TPMC378-10R

Subsystem ID Value (Offset 0x0C): TPMC378-10R 0x000A

The words following the configuration data contain:

- The module version and revision
- The UART clock frequency in Hz
- The physical interface attached to the serial channels
- The maximal baud rate of the transceivers in bps
- The supported control signals of the serial channels

For the physical interfaces and the control signals applies: Bit 7 represents UART channel 7 and bit 0 represents UART channel 0. The appropriate bit is set to ‘1’ for each UART channel attached to the physical interface represented by the word. Bit 15 to bit 8 are always ‘0’.

Address	Configuration Register	TPMC378-10R
0x04	Module Version	0x0100
0x05	Module Revision	0x0000
0x06	EEPROM Revision	0x0003
0x07	Oscillator Frequency (high)	0x02A3
0x08	Oscillator Frequency (low)	0x0000
0x09-0x0F	Reserved	-
0x10	RS232 Channels	0x0000
0x11	RS422 Channels	0x00FF
0x12	TTL Channels	0x0000
0x13	RS485 Full Duplex Channels	0x0000
0x14	RS485 Half Duplex Channels	0x0000
0x15-0x1E	Reserved	-
0x1F	Programmable Interfaces	0x0000
0x20	Max Data Rate RS232 (high)	0x0000
0x21	Max Data Rate RS232 (low)	0x0000
0x22	Max Data Rate RS422 (high)	0x0098
0x23	Max Data Rate RS422 (low)	0x9680
0x24	Max Data Rate TTL (high)	0x0000
0x25	Max Data Rate TTL (low)	0x0000
0x26	Max Data Rate RS485 Full Duplex (high)	0x0000
0x27	Max Data Rate RS485 Full Duplex (low)	0x0000
0x28	Max Data Rate RS485 Half Duplex (high)	0x0000
0x29	Max Data Rate RS485 Half Duplex (low)	0x0000
0x2A-0x2F	Reserved	-
0x30	RxD & TxD	0x00FF
0x31	RTS & CTS	0x0003
0x32	Full modem	0x0000
0x33-0x37	Reserved	-
0x38	Enhanced RTS & CTS (Front or Back I/O only)	0x0000
0x39	Enhanced Full modem (Front or Back I/O only)	0x0000
0x3A	Channels with enhanced RTS & CTS Support for RS232 only	0x0000
0x3B-0x3F	Reserved	-

Table 4-3 : Physical Configuration EEPROM Data

5 Configuration Hints

5.1 I/O Electrical Interface

5.1.1 ±15kV ESD Protection

The receiver inputs and transmitter outputs are characterized for ±15kV ESD protection using the Human Body Model.

5.1.2 Termination

The receive and the transmit line can be terminated with a 120? termination resistor.

5.1.3 Galvanic Isolation

Each of the four channels is isolated from the system and against each other by digital isolator and on board integrated DC/DC converter.

6 Programming Hints

6.1 UART Baud Rate Programming

Each of the 8 UART channels of the TPMC461 provides a programmable Baud Rate Generator. The clock of the XR17D158 UART can be divided by any divisor from 1 to 216 – 1. The divisor can be programmed by the UART channel DLM (Divisor MSB) and DLL (Divisor LSB) registers. After a reset bit 7 of the UART channels MCR register defaults to '0' and the divisor value is 0xFFFF.

The basic formula of baud rate programming is:

$$\text{Baud Rate} = \frac{44.2368\ \text{MHz}}{16 \cdot \text{Divisor} \cdot (1+3 \cdot \text{MCR}[7])}$$

Examples for standard baud rates are given in following chart:

Baud Rate MCR[7] = 0	Baud Rate MCR[7] = 1	Divisor	DLM Value	DLL Value
400	100	0x1B00	0x1B	0x00
600	150	0x1200	0x12	0x00
1200	600	0x0900	0x09	0x00
2400	600	0x0480	0x04	0x80
4800	1200	0x0240	0x02	0x40
9600	2400	0x0120	0x01	0x20
19.2k	4800	0x0090	0x00	0x90
38.4k	9600	0x0048	0x00	0x48
57.6k	14.4k	0x0030	0x00	0x30
115.2k	28.8k	0x0018	0x00	0x18
230.4k	57.6k	0x000C	0x00	0x0C
460.8k	115.2k	0x0006	0x00	0x06
921.6k	230.4k	0x0003	0x00	0x03
1.3824M	345.6k	0x0002	0x00	0x02
2.7648M	691.2k	0x0001	0x00	0x01

Table 6-1 : UART Baud Rate Programming

To calculate a divisor value for a given baud rate, use following formula:

$$\text{Divisor} = \frac{44.2368\ \text{MHz}}{16 \cdot \text{Baud Rate} \cdot (1+3 \cdot \text{MCR}[7])}$$

The sampling rate for a UART channel can be set to 8x (normal operation is 16x) in the 8XMODE register. Transmit and receive data rates will double by selecting 8x sample rate.

The maximum achievable baud rate is 5.5296 Mbps (Divisor = 0x0001 & 8x sampling rate).

These steps should be used to modify the DLM, DLL registers of an UART channel:

1. Write 0x80 to the LCR register of the UART channel (enable access to the DLM, DLL registers).

2. Program the DLM, DLL registers of the UART channel.

3. Write normal operation byte value to the LCR register of the UART channel.

These steps should be used to modify MCR register bit 7 of an UART channel (set baud rate generator prescaler):

1. Set UART channel EFR register bit 4 to '1' (enable modification of MCR register bits 5-7).

2. Modify UART channel MCR register bit 7.

3. Set UART channel EFR register bit 4 to '0' (latch modified MCR register setting).

6.2 RS422 Flow Control

Only UART channels 0 & 1 allow using RS422 with RTS/CTS flow control. On channels 2 – 7 the CTS# input is hardwired to ’1’, so that no RTS/CTS flow control is possible.

7 Pin Assignment – I/O Connector

7.1 Back I/O PMC Connector (P14)

Pin	Signal	Level
1	GND_0	-
2	TxD0-	RS422
3	TxD0+	RS422
4	RxD0-	RS422
5	RxD0+	RS422
6	GND_1	-
7	TxD1-	RS422
8	TxD1+	RS422
9	RxD1-	RS422
10	RxD1+	RS422
11	GND_2	-
12	TxD2-	RS422
13	TxD2+	RS422
14	RxD2-	RS422
15	RxD2+	RS422
16	GND_3	-
17	TxD3-	RS422
18	TxD3+	RS422
19	RxD3-	RS422
20	RxD3+	RS422
21	GND_4	-
22	TxD4-	RS422
23	TxD4+	RS422
24	RxD4-	RS422
25	RxD4+	RS422
26	GND_5	-
27	TxD5-	RS422
28	TxD5+	RS422
29	RxD5-	RS422
30	RxD5+	RS422
31	GND_6	-
32	TxD6-	RS422

Pin	Signal	Level
33	TxD6+	RS422
34	RxD6-	RS422
35	RxD6+	RS422
36	GND_7	-
37	TxD7-	RS422
38	TxD7+	RS422
39	RxD7-	RS422
40	RxD7+	RS422
41	-	-
42	-	-
43	RTS0-	RS422
44	RTS0+	RS422
45	CTS0-	RS422
46	CTS0+	RS422
47	RTS1-	RS422
48	RTS1+	RS422
49	CTS1-	RS422
50	CTS1+	RS422
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Table 7-1 : Pin Assignment Back I/O PMC Connector (P14)