The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC463

4 Channel Serial Interface RS232/RS422

Version 1.0

User Manual

Issue 1.0.12

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TPMC463-10R

4 Channel Serial RS232, front panel and P14 I/O

TPMC463-11R

4 Channel Serial RS422, front panel and P14 I/O

TPMC463-12R

2 Channel Serial RS232, 2 Channel Serial RS422, front panel and P14 I/O

TPMC463-20R

4 Channel Serial RS232, front panel and P14 I/O with non-standard RJ45 I/O pinout

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	October 2004
1.1	Expanded Configuration EEPROM data	November 2004
1.2	Expanded Configuration EEPROM data, I/O pinout clarification	April 2005
1.3	Back I/O pinout correction, included -2x modules	July 2005
1.4	Front I/O pinout clarification	September 2005
1.5	Configuration EEPROM data & Pinout clarification	October 2005
1.6	Channel numbering clarification	August 2006
1.7	New address TEWS LLC	September 2006
1.8	Front I/O pinout correction in chapter “Technical Specification”	June 2007
1.0.9	New notation for HW Engineering Documentation Releases	December 2008
1.0.10	Clarified the difference between front- and back-I/O RS422 signals	August 2010
1.0.11	General Revision	August 2014
1.0.12	Fixed typos Corrected “Size” in “Table 3 1: XR17D154 Local Space Configuration”	May 2020

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1 Product Description

The TPMC463 is a standard single-width 32 bit PMC module and offers 4 channels of high performance serial interface.

Three different standard modules are available: The TPMC463-10R provides 4 RS232 interfaces. The TPMC463-11R provides 4 RS422 interfaces. The TPMC463-12R provides 2 RS232 and 2 RS422 interfaces.

The TPMC463-20R provides 4 RS232 interfaces with non standard RJ45 I/O pinout (as used on Motorola CPU boards).

Other configurations are available as factory build option on a per channel base.

All modules offer front panel I/O with four RJ45 connectors and P14 I/O. Each RS232 channel supports TxD, RxD, CTS, RTS, DTR, CD, DSR/RI and GND. Each RS422 channel supports RxD+/-, TxD+/- and GND on front and RxD+/-, TxD+/-, RTS+/- and CTS+/- on back I/O.

Each channel has 64 byte transmit and receive FIFOs to significantly reduce the overhead required to provide data to and get data from the transmitters and receivers. The FIFO trigger levels are programmable and the baud rate is individually programmable up to 921.6 kbps for RS232 channels and 5.5296 Mbps for RS422 channels. The UART offers readable FIFO levels.

All channels generate interrupts on PCI interrupt INTA. For fast interrupt source detection the UART provides a special Global Interrupt Source Register.

All serial channels use ESD protected transceivers. ESD protection is up to ±15KV.

The TPMC463 can operate with 3.3V and 5.0V PCI I/O signaling voltage.

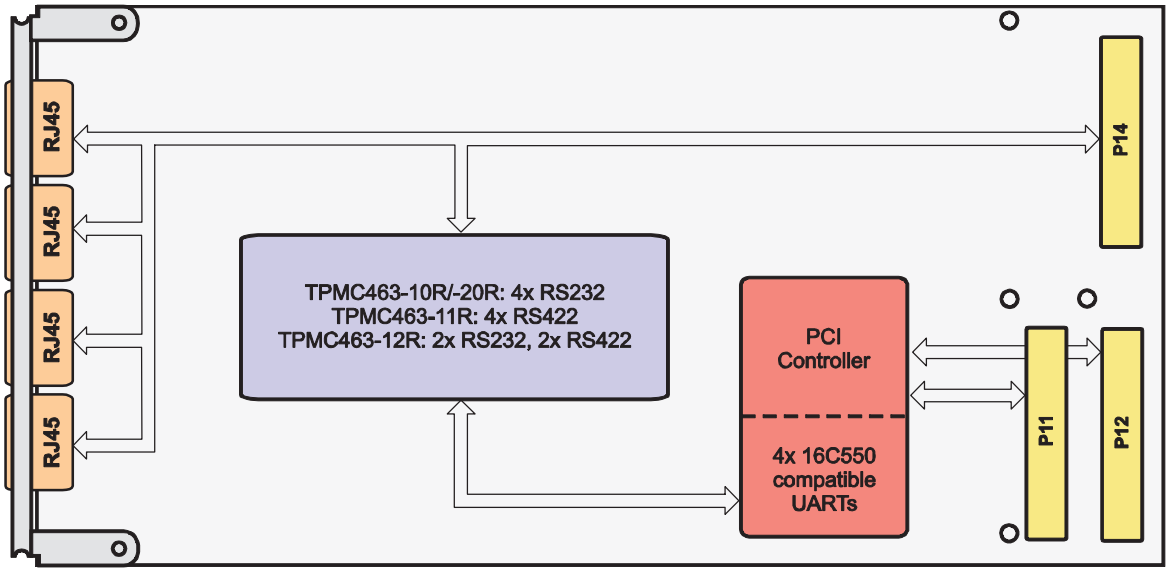

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface	
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size
Electrical Interface	PCI Rev. 2.3 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage
On Board Devices	
PCI Target Chip	XR17D154 (Exar)
Quad UART	XR17D154 (Exar)
Transceiver	RS232: MAX3245E (or equivalent) RS422: MAX3087E (or equivalent)
I/O Interface	
Interface Type	Asynchronous serial interface
Number of Channels	4
Physical Interface	TPMC463-10R: 4 RS232 TPMC463-11R: 4 RS422 TPMC463-12R: 2 RS232, 2 RS422 TPMC463-20R: 4 RS232
Serial Channel I/O Signals	RS232: TxD, RxD, RTS, CTS, DTR, CD, DSR/RI, GND RS422 (front I/O): TxD+/-, RxD+/-, GND RS422 (back I/O): TxD+/-, RxD+/-, RTS+/-, CTS+/-, GND
I/O Connector	4x RJ45 Modular Jack (AMP 406 732-1) PMC P14 I/O (64 pin Mezzanine Connector)
Front I/O Pinout	RS232 (TPMC463-10R/-12R): Compliant to TIA/EIA-561 (EIA-232D) RS232 (TPMC463-20R): Compliant to TIP866-TM-20
Termination	RS422: 120Ω between RxD+/- and CTS+/- of each channel
Programmable Baud Rates	RS232: up to 921.6 kbps RS422: up to 5.5296 Mbps
ESD Protection	RS232: ±15kV—Human Body Model ±8kV—IEC 1000-4-2, Contact Discharge ±15kV—IEC 1000-4-2, Air-Gap Discharge RS422: ±15kV—Human Body Model

Physical Data		
Power Requirements	TPMC463-10R: 30 mA typical @ +5V DC (no load) TPMC463-11R: 40 mA typical @ +5V DC (no load) TPMC463-12R: 35 mA typical @ +5V DC (no load) TPMC463-20R: 30 mA typical @ +5V DC (no load)	
Temperature Range	Operating Storage	-40°C to +85°C -55°C to +125°C
MTBF	TPMC463-10R: 370 000 h TPMC463-11R: 320 000 h TPMC463-12R: 350 000 h TPMC463-20R: 370 000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	66 g	

Table 2-1 : Technical Specification

3 Local Space Addressing

3.1 XR17D154 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the XR17D154 local space.

XR17D154 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0 (0x10)	MEM	2048	32	BIG	Device Configuration Space

Table 3-1 : XR17D154 Local Space Configuration

3.2 Device Configuration Space

PCI Base Address: XR17D154 PCI Base Address 0 (Offset 0x10 in PCI Configuration Space).

The TPMC463 uses the Exar XR17D154 Quad UART to provide and control the 4 channels.

Device Configuration Space Content	PCI Address	Size (Bit)
UART 0 Register Set	PCI Base Address 0 + (0x0000 to 0x007F)	32
Device Configuration Registers	PCI Base Address 0 + (0x0080 to 0x009F)	32
UART 0 Register Set	PCI Base Address 0 + (0x0100 to 0x01FF)	32
UART 1 Register Set	PCI Base Address 0 + (0x0200 to 0x03FF)	32
UART 2 Register Set	PCI Base Address 0 + (0x0400 to 0x05FF)	32
UART 3 Register Set	PCI Base Address 0 + (0x0600 to 0x07FF)	32

Table 3-2 : Device Configuration Space

All registers can be accessed in 8, 16 or 32 bit width with exception to one special case: When reading the receive data together with its LSR register content, the host must read them in 16 or 32 bits format in order to maintain integrity of the data byte with its associated error flags.

3.2.1 UART Register Sets

The Device Configuration Space provides a register set for each of the 4 UARTs.

UART Register Set	Register Set Offset
Serial Channel 0	0x0000
Serial Channel 1	0x0200
Serial Channel 2	0x0400
Serial Channel 3	0x0600

Table 3-3 : UART Register Set Offset

Offset Address	Description	Access	Data Width
0x000 – 0x00F	UART Channel Configuration Registers First 8 registers are 16550 compatible	R/W	8, 16, 32
0x010 – 0x07F	Reserved	-	-
0x080 – 0x093	Channel 0: Device Configuration Registers All other channels: Reserved	R/W	8, 16, 32
0x094 – 0x0FF	Reserved	-	-
0x100	Read FIFO – 64 bytes of RX FIFO data	R	8, 16, 32
	Write FIFO – 64 bytes of TX FIFO data	W	8, 16, 32
0x140 – 0x17F	Reserved	-	-
0x180 – 0x1FF	Read FIFO with errors – 64 bytes of RX FIFO data + LSR	R	16, 32

Table 3-4 : UART Register Set

3.2.2 Device Configuration Registers

The Device Configuration Registers control general operating conditions and monitor the status of various functions. This includes a 16 bit general purpose counter, multipurpose input/outputs (not supported by the TPMC463), sleep mode, soft-reset and device identification, and revision. They are embedded inside the UART 0 Register Set.

Address	Register	Description	Access	Reset Value
0x080	INT0 [7:0]	Channel Interrupt Indicator	R	0x00
0x081	INT1 [15:8]	Interrupt Source Details	R	0x00
0x082	INT2 [23:16]		R	0x00
0x083	INT3 [31:24]		R	0x00
0x084	TIMERCNTL	Timer Control Register	R/W	0x00
0x085	TIMER	Reserved	-	0x00
0x086	TIMERLSB	Programmable Timer Value	R/W	0x00
0x087	TIMERMSB		R/W	0x00
0x088	8XMODE	Sampling Rate Select	R/W	0x00
0x089	REGA	Reserved	-	0x00
0x08A	RESET	UART Reset	W	0x00
0x08B	SLEEP	UART Sleep Mode Enable	R/W	0x00
0x08C	DREV	Device Revision	R	0x01
0x08D	DVID	Device Identification	R	0x28
0x08E	REGB	Simultaneous UART Write & EEPROM Interface	W	0x00
0x08F	MPIOINT	MPIO Interrupt Mask	R/W	0x00
0x090	MPIOLVL	MPIO Level Control	R/W	0x00
0x091	MPIO3T	MPIO Output Pin Tri-state Control	R/W	0x00
0x092	MPIOINV	MPIO Input Polarity Select	R/W	0x00
0x093	MPIOSEL	MPIO Input/Output Select	R/W	0xFF

Table 3-5 : Device Configuration Registers

For a detailed description of the Device Configuration Registers please refer to the XR17D154 data sheet which is available on the Exar website (www.exar.com).

3.2.3 UART Channel Configuration Registers

Each UART channel has its own set of internal UART configuration registers for its own operation control and status reporting. The following table provides the register offsets within a register set, access types and access control:

Register Offset	Comment	Register	Access	Reset Value
16550 Compatible				
0x00	LCR[7] = 0	RHR – Receive Holding Register THR – Transmit Holding Register	R W	0xXX
	LCR[7] = 1	DLL – Baud Rate Generator Divisor Latch Low	R/W	0xXX
0x01	LCR[7] = 0	IER – Interrupt Enable Register	R/W	0x00
	LCR[7] = 1	DLM – Baud Rate Generator Divisor Latch High	R/W	0xXX
0x02		ISR – Interrupt Status Register FCR – FIFO Control Register	R W	0x01 0x00
0x03		LCR – Line Control Register	R/W	0x00
0x04		MCR – Modem Control Register	R/W	0x00
0x05		LSR – Line Status Register Reserved	R W	0x60
0x06		MSR – Modem Status Register – Auto RS485 Delay (not supported by the TPMC463)	R W	0xX0
0x07	User Data	SPR – Scratch Pad Register	R/W	0xFF
Enhanced Registers				
0x08		FCTR – Feature Control Register	R/W	0x00
0x09		EFR – Enhanced Function Register	R/W	0x00
0x0A		TXCNT – Transmit FIFO Level Counter TXTRG – Transmit FIFO Trigger Level	R W	0x00
0x0B		RXCNT – Receiver FIFO Level Counter RXTRG – Receiver FIFO Trigger Level	R W	0x00
0x0C		Xchar – Xon, Xoff Received Flags Xoff-1 – Xoff Character 1	R W	0x00
0x0D		Reserved Xoff-2 – Xoff Character 2	R W	0x00
0x0E		Reserved Xon-1 – Xon Character 1	R W	0x00
0x0F		Reserved Xon-2 – Xon Character 2	R W	0x00

Table 3-6 : UART Channel Configuration Registers

The address for a UART Channel Configuration Register x in a UART Register Set for channel y is:

PCI Base Address 0 (PCI Base Address for the UART Register Space)

+ UART Register Set Offset for *channel y*

+ Register Offset for *register x*

Addressing example:

The address for the LCR register of UART channel 2 is:

PCI Base Address	(PCI Base Address for the Device Configuration Space)
+ 0x0400	(Offset of the UART register set for serial channel 2)
+ 0x0003	(Offset of the LCR register within a UART register set)

For a detailed description of the serial channel registers please refer to the XR17D154 data sheet which is available on the Exar website (www.exar.com).

4 XR17D154 Target Chip

4.1 PCI Configuration Registers (PCR)

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	01CF 1498
0x04	Status		Command		Y	0080 0000
0x08	Class Code			Revision ID	N	070002 ??
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	N	00 00 00 00
0x10	Memory Base Address Register (BAR)				Y	FFFFF000
0x14	I/O Base Address Register (Unimplemented)				N	00000000
0x18	Base Address Register 0 (Unimplemented)				N	00000000
0x1C	Base Address Register 1 (Unimplemented)				N	00000000
0x20	Base Address Register 2 (Unimplemented)				N	00000000
0x24	Base Address Register 3 (Unimplemented)				N	00000000
0x28	Reserved				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	s.b. 1498
0x30	Expansion ROM Base Address (Unimplemented)				N	00000000
0x34	Reserved				N	00000000
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00

Table 4-1 : PCI Header

Device-ID:	0x01CF	TPMC463
Vendor-ID:	0x1498	TEWS TECHNOLOGIES
Revision ID:		XR17D154 silicon revision
Subsystem-ID:	0x000A	-10R
	0x000B	-11R
	0x000C	-12R
	0x0014	-20R
Subsystem Vendor-ID:	0x1498	TEWS TECHNOLOGIES

4.2 Configuration EEPROM

After power-on or PCI reset, the XR17D154 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Vendor ID
- Vendor Device ID
- SubSystem Vendor ID
- SubSystem Device ID

See the XR17D154 Manual for more information.

Address	Configuration Register	Configuration Register Offset	Value
0x00	Vendor ID	0x02	0x1498
0x01	Device ID	0x00	0x01CF
0x02	Subsystem Vendor ID	0x2E	0x1498
0x03	Subsystem ID	0x2C	s.b.

Table 4-2 : Configuration EEPROM TPMC463-xx

Subsystem-ID Value (Offset 0x0C): TPMC463-10R 0x000A

TPMC463-11R 0x000B

TPMC463-12R 0x000C

TPMC463-20R 0x0014

The words following the configuration data contain:

- The module version and revision
- The UART clock frequency in Hz
- The physical interface attached to the serial channels
- The maximal baud rate of the transceivers in bps
- The supported control signals of the serial channels

For the physical interfaces and the control signals applies: Bit 3 represents UART channel 3 and bit 0 represents UART channel 0. The appropriate bit is set to ‘1’ for each UART channel attached to the physical interface represented by the word. Bit 15 to bit 4 are always ‘0’.

Address	Configuration Register	TPMC463-10R	TPMC463-11R	TPMC463-12R	TPMC463-20R
0x04	Module Version	0x0100	0x0100	0x0100	0x0100
0x05	Module Revision	0x0000	0x0000	0x0000	0x0000
0x06	EEPROM Revision	0x0002	0x0002	0x0002	0x0002
0x07	Oscillator Frequency (high)	0x02A3	0x02A3	0x02A3	0x02A3
0x08	Oscillator Frequency (low)	0x0000	0x0000	0x0000	0x0000
0x09-0x0F	Reserved	-	-	-	-
0x10	RS232 Channels	0x000F	0x0000	0x0003	0x000F
0x11	RS422 Channels	0x0000	0x000F	0x000C	0x0000
0x12	TTL Channels	0x0000	0x0000	0x0000	0x0000
0x13	RS485 Full Duplex Channels	0x0000	0x0000	0x0000	0x0000
0x14	RS485 Half Duplex Channels	0x0000	0x0000	0x0000	0x0000
0x15-0x1E	Reserved	-	-	-	-
0x1F	Programmable Interfaces	0x0000	0x0000	0x0000	0x0000
0x20	Max Data Rate RS232 (high)	0x000F	0x000F	0x000F	0x000F
0x21	Max Data Rate RS232 (low)	0x4240	0x4240	0x4240	0x4240
0x22	Max Data Rate RS422 (high)	0x0098	0x0098	0x0098	0x0098
0x23	Max Data Rate RS422 (low)	0x9680	0x9680	0x9680	0x9680
0x24	Max Data Rate TTL (high)	0x0098	0x0098	0x0098	0x0098
0x25	Max Data Rate TTL (low)	0x9680	0x9680	0x9680	0x9680
0x26	Max Data Rate RS485 Full Duplex (high)	0x0000	0x0000	0x0000	0x0000
0x27	Max Data Rate RS485 Full Duplex (low)	0x0000	0x0000	0x0000	0x0000
0x28	Max Data Rate RS485 Half Duplex (high)	0x0000	0x0000	0x0000	0x0000
0x29	Max Data Rate RS485 Half Duplex (low)	0x0000	0x0000	0x0000	0x0000
0x2A-0x2F	Reserved	-	-	-	-
0x30	RxD & TxD	0x000F	0x000F	0x000F	0x000F
0x31	RTS & CTS	0x000F	0x0000	0x0003	0x000F
0x32	Full modem	0x000F	0x0000	0x0003	0x0000
0x33-0x37	Reserved	-	-	-	-
0x38	Enhanced RTS & CTS (Front or Back I/O only)	0x0000	0x000F	0x000C	0x0000
0x39	Enhanced Full modem (Front or Back I/O only)	0x0000	0x0000	0x0000	0x000F
0x3A	Channels with enhanced RTS & CTS Support for RS232 only	0x0000	0x0000	0x0000	0x0000
0x3B-0x3F	Reserved	-	-	-	-

Table 4-3 : Physical Configuration EEPROM Data

5 Configuration Hints

The following chart shows the UART interface mapping of the different variants of the TPMC463.

	TPMC463-10R		TPMC463-11R		TPMC463-12R		TPMC463-20R	
	RS232	RS422	RS232	RS422	RS232	RS422	RS232	RS422
UART0	X			X	X		X	
UART1	X			X	X		X	
UART2	X			X		X	X	
UART3	X			X		X	X	

Table 5-1 : UART interface mapping

Other configurations are available as factory build option on a per channel base.

RS422 channels provide on board 120Ω termination resistors. Do not apply additional external termination resistors here.

6 Programming Hints

6.1 UART Baud Rate Programming

Each of the 4 UART channels of the TPMC463 provides a programmable Baud Rate Generator. The clock of the XR17D154 UART can be divided by any divisor from 1 to 2^{16} – 1. The divisor can be programmed by the UART channel DLM (Divisor MSB) and DLL (Divisor LSB) registers. After a reset bit 7 of the UART channels MCR register defaults to '0' and the divisor value is 0xFFFF.

The basic formula of baud rate programming is:

$$\text{Baud Rate} = \frac{44.2368MHz}{16 \cdot Divisor \cdot (1 + 3 \cdot MCR[7])}$$

Examples for standard baud rates are given in following chart:

Baud Rate MCR[7] = 0	Baud Rate MCR[7] = 1	Divisor	DLM Value	DLL Value
400	100	0x1B00	0x1B	0x00
600	150	0x1200	0x12	0x00
1200	300	0x0900	0x09	0x00
2400	600	0x0480	0x04	0x80
4800	1200	0x0240	0x02	0x40
9600	2400	0x0120	0x01	0x20
19.2k	4800	0x0090	0x00	0x90
38.4k	9600	0x0048	0x00	0x48
57.6k	14.4k	0x0030	0x00	0x30
115.2k	28.8k	0x0018	0x00	0x18
230.4k	57.6k	0x000C	0x00	0x0C
460.8k	115.2k	0x0006	0x00	0x06
921.6k	230.4k	0x0003	0x00	0x03
1382.4k	345.6k	0x0002	0x00	0x02
2764.8k	691.2k	0x0001	0x00	0x01

Table 6-1 : UART Baud Rate Programming

To calculate a divisor value for a given baud rate, use following formula:

$$\text{Divisor} = \frac{44.2368MHz}{16 \cdot Baud\ Rate \cdot (1 + 3 \cdot MCR[7])}$$

The sampling rate for a UART channel can be set to 8x (normal operation is 16x) in the 8XMODE register. Transmit and receive data rates will double by selecting 8x sample rate.

The maximum achievable baud rate is 5.5296 Mbps (Divisor = 0x0001 & 8x sampling rate).

These steps should be used to modify the DLM, DLL registers of an UART channel:

1. Write 0x80 to the LCR register of the UART channel (enable access to the DLM, DLL registers).

2. Program the DLM, DLL registers of the UART channel.

3. Write normal operation byte value to the LCR register of the UART channel.

These steps should be used to modify MCR register bit 7 of an UART channel (set baud rate generator prescaler):

1. Set UART channel EFR register bit 4 to '1' (enable modification of MCR register bits 5-7).

2. Modify UART channel MCR register bit 7.

3. Set UART channel EFR register bit 4 to '0' (latch modified MCR register setting).

Note that the maximum baud rate for RS232 channel is 921.6 kps. Thus the minimum divisor value for RS232 channels is 0x0003 with MCR[7] = 0.

7 Pin Assignment – I/O Connector

Connect channel I/O either to front I/O or P14 back I/O at a time. Do not connect an I/O channel to both front I/O connector and P14 back I/O connector at the same time.

RS422 channels provide on board termination resistors. Do not apply additional external termination resistors here.

Please note that on the TPMC463, the P14 back I/O connector is always populated and connected to on board logic. Do not use these modules on carrier boards where P14/J14 is reserved for other system signals but PMC I/O. In this case ask support for special board options with front I/O only.

7.1 Front Panel I/O Connector (TPMC463-1xR)

The TPMC463 front panel I/O connector is a RJ45 modular jack connector (e.g. AMP# 406 732-1).

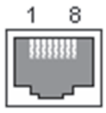

Figure 7-1 : I/O Connector Pinout

Pin	Signal RS232	Signal RS422
1	DSR/RI	-
2	CD	-
3	DTR	TxD+
4	GND	GND
5	RxD	+5V Termination Supply (unfused)
6	TxD	TxD-
7	CTS	RxD+
8	RTS	RxD-

Table 7-1 : Pin Assignment RJ45 Front Panel I/O Connector

The RS232 pinout is compliant to TIA/EIA-561 (EIA-232D).

The DSR/RI signal is connected with the DSR and RI transceiver inputs, making both DSR and RI available at the UART. This leaves the choice which signal to use in an application.

7.2 Front Panel I/O Connector (TPMC463-2xR)

The TPMC463 front panel I/O connector is a RJ45 modular jack connector (e.g. AMP# 406 732-1).

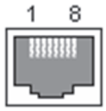

Figure 7-2 : I/O Connector Pinout

Pin	Signal RS232	Signal RS422
1	DCD	-
2	RTS	TxD+
3	GND	GND
4	TxD	TxD-
5	RxD	RxD-
6	GND	GND
7	CTS	RxD+
8	DTR	-

Table 7-2 : Pin Assignment RJ45 Front Panel I/O Connector

The RS232 pinout is compliant to TIP866-TM-20 or to the “Motorola Standard”. The RS422 pinout is compliant to TIP866-TM-20.

7.3 Serial Channel to Front Panel Port Mapping

The serial channels 0-3 are mapped onto the 4 front panel connectors labeled Port1 – Port4.

Serial Channel	Front Panel Port
Channel 0	Port 1
Channel 1	Port 2
Channel 2	Port 3
Channel 3	Port 4

Table 7-3 : Serial Channel to Front Panel Port Mapping

7.4 Back I/O PMC Connector (P14)

7.4.1 TPMC463-10R

Pin	Signal	Signal Level
1	GND	-
2	TxD0	RS232
3	RxD0	RS232
4	RTS0	RS232
5	CTS0	RS232
6	GND	-
7	CD0	RS232
8	DTR0	RS232
9	DSR/RI0	RS232
10	-	-
11	GND	-
12	TxD1	RS232
13	RxD1	RS232
14	RTS1	RS232
15	CTS1	RS232
16	GND	-
17	CD1	RS232
18	DTR1	RS232
19	DSR/RI1	RS232
20	-	-
21	GND	-
22	TxD2	RS232
23	RxD2	RS232
24	RTS2	RS232
25	CTS2	RS232
26	GND	-
27	CD2	RS232
28	DTR2	RS232
29	DSR/RI2	RS232
30	-	-
31	GND	-
32	TxD3	RS232

Pin	Signal	Signal Level
33	RxD3	RS232
34	RTS3	RS232
35	CTS3	RS232
36	GND	-
37	CD3	RS232
38	DTR3	RS232
39	DSR/RI3	RS232
40	-	-
41	GND	-
42	+5V Termination Supply (unfused!)	
43	-	-
44	-	-
45	-	-
46	-	-
47	-	-
48	-	-
49	-	-
50	-	-
51	-	-
52	-	-
53	-	-
54	-	-
55	-	-
56	-	-
57	-	-
58	-	-
59	-	-
60	-	-
61	-	-
62	-	-
63	-	-
64	-	-

Table 7-4 : TPMC463-10R Pin Assignment Back I/O PMC Connector (P14)

The DSR/RI signals are connected with the DSR and RI transceiver inputs, making both DSR and RI available at the UART. This leaves the choice which signal to use in an application.

7.4.2 TPMC463-11R

Pin	Signal	Signal Level
1	GND	-
2	TxD0-	RS422
3	TxD0+	RS422
4	RxD0-	RS422
5	RxD0+	RS422
6	GND	-
7	RTS0-	RS422
8	RTS0+	RS422
9	CTS0+	RS422
10	CTS0-	RS422
11	GND	-
12	TxD1-	RS422
13	TxD1+	RS422
14	RxD1-	RS422
15	RxD1+	RS422
16	GND	-
17	RTS1-	RS422
18	RTS1+	RS422
19	CTS1+	RS422
20	CTS1-	RS422
21	GND	-
22	TxD2-	RS422
23	TxD2+	RS422
24	RxD2-	RS422
25	RxD2+	RS422
26	GND	-
27	RTS2-	RS422
28	RTS2+	RS422
29	CTS2+	RS422
30	CTS2-	RS422
31	GND	-
32	TxD3-	RS422

Pin	Signal	Signal Level
33	TxD3+	RS422
34	RxD3-	RS422
35	RxD3+	RS422
36	GND	-
37	RTS3-	RS422
38	RTS3+	RS422
39	CTS3+	RS422
40	CTS3-	RS422
41	GND	-
42	+5V Termination Supply (unfused!)	
43	-	-
44	-	-
45	-	-
46	-	-
47	-	-
48	-	-
49	-	-
50	-	-
51	-	-
52	-	-
53	-	-
54	-	-
55	-	-
56	-	-
57	-	-
58	-	-
59	-	-
60	-	-
61	-	-
62	-	-
63	-	-
64	-	-

Table 7-5 : TPMC463-11R Pin Assignment Back I/O PMC Connector (P14)

7.4.3 TPMC463-12R

Pin	Signal	Signal Level
1	GND	-
2	TxD0	RS232
3	RxD0	RS232
4	RTS0	RS232
5	CTS0	RS232
6	GND	-
7	CD0	RS232
8	DTR0	RS232
9	DSR/RI0	RS232
10	-	-
11	GND	-
12	TxD1	RS232
13	RxD1	RS232
14	RTS1	RS232
15	CTS1	RS232
16	GND	-
17	CD1	RS232
18	DTR1	RS232
19	DSR/RI1	RS232
20	-	-
21	GND	-
22	TxD2-	RS422
23	TxD2+	RS422
24	RxD2-	RS422
25	RxD2+	RS422
26	GND	-
27	RTS2-	RS422
28	RTS2+	RS422
29	CTS2+	RS422
30	CTS2-	RS422
31	GND	-
32	TxD3-	RS422

Pin	Signal	Signal Level
33	TxD3+	RS422
34	RxD3-	RS422
35	RxD3+	RS422
36	GND	-
37	RTS3-	RS422
38	RTS3+	RS422
39	CTS3+	RS422
40	CTS3-	RS422
41	GND	-
42	+5V Termination Supply (unfused!)	
43	-	-
44	-	-
45	-	-
46	-	-
47	-	-
48	-	-
49	-	-
50	-	-
51	-	-
52	-	-
53	-	-
54	-	-
55	-	-
56	-	-
57	-	-
58	-	-
59	-	-
60	-	-
61	-	-
62	-	-
63	-	-
64	-	-

Table 7-6 : TPMC463-12R Pin Assignment Back I/O PMC Connector (P14)

The DSR/RI signals are connected with the DSR and RI transceiver inputs, making both DSR and RI available at the UART. This leaves the choice which signal to use in an application.

7.4.4 TPMC463-20R

Pin	Signal	Signal Level
1	GND	-
2	TxD0	RS232
3	RxD0	RS232
4	RTS0	RS232
5	CTS0	RS232
6	GND	-
7	CD0	RS232
8	DTR0	RS232
9	DSR/RI0	RS232
10	-	-
11	GND	-
12	TxD1	RS232
13	RxD1	RS232
14	RTS1	RS232
15	CTS1	RS232
16	GND	-
17	CD1	RS232
18	DTR1	RS232
19	DSR/RI1	RS232
20	-	-
21	GND	-
22	TxD2	RS232
23	RxD2	RS232
24	RTS2	RS232
25	CTS2	RS232
26	GND	-
27	CD2	RS232
28	DTR2	RS232
29	DSR/RI2	RS232
30	-	-
31	GND	-
32	TxD3	RS232

Pin	Signal	Signal Level
33	RxD3	RS232
34	RTS3	RS232
35	CTS3	RS232
36	GND	-
37	CD3	RS232
38	DTR3	RS232
39	DSR/RI3	RS232
40	-	-
41	GND	-
42	+5V Termination Supply (unfused!)	
43	-	-
44	-	-
45	-	-
46	-	-
47	-	-
48	-	-
49	-	-
50	-	-
51	-	-
52	-	-
53	-	-
54	-	-
55	-	-
56	-	-
57	-	-
58	-	-
59	-	-
60	-	-
61	-	-
62	-	-
63	-	-
64	-	-

Table 7-7 : TPMC463-10R Pin Assignment Back I/O PMC Connector (P14)

The DSR/RI signals are connected with the DSR and RI transceiver inputs, making both DSR and RI available at the UART. This leaves the choice which signal to use in an application.