

*The Embedded I/O Company*



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# TCP030-TM-10

**Transition Module for 3U cPCI PMC-Carrier**

**Version 1.0**

## **User Manual**

Issue 1.3

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**TEWS TECHNOLOGIES GmbH**

Am Bahnhof 7  
25469 Halstenbek, Germany  
www.tews.com

Phone: +49-(0)4101-4058-0  
Fax: +49-(0)4101-4058-19  
e-mail: info@tews.com

**TEWS TECHNOLOGIES LLC**

9190 Double Diamond Parkway,  
Suite 127, Reno, NV 89521, USA  
www.tews.com

Phone: +1 (775) 850 5830  
Fax: +1 (775) 201 0347  
e-mail: usasales@tews.com



Ehlbeek 15a  
30938 Burgwedel  
fon 05139-9980-0  
fax 05139-9980-49

www.powerbridge.de  
info@powerbridge.de

**TCP030-TM-10**

Transition Module for 3U cPCI PMC-Carrier

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**Style Conventions**

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low’ is represented by the signal name with # following, i.e. IP\_RESET#.

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<b>Issue</b>	<b>Description</b>	<b>Date</b>
1.0	First Issue	November 2004
1.1	Correction of Pin Description for X1 Pin 65 to 68	April 2005
1.2	New address TEWS LLC	September 2006
1.3	Correction Figure "Pin Assignment"	September 2006

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# 1 Product Description

The TCP030-TM-10 is a 3U Transition Module to be used with 3U cPCI PMC carrier like TEWS' TCP270. It provides easy access to the PMC I/O lines of cPCI PMC carrier with back I/O.

It distributes all 64 PMC I/O lines from the cPCI RJ2 connector to a HD68 SCSI-3 type connector located in the front panel.

The operating temperature range is -40°C to +85°C.

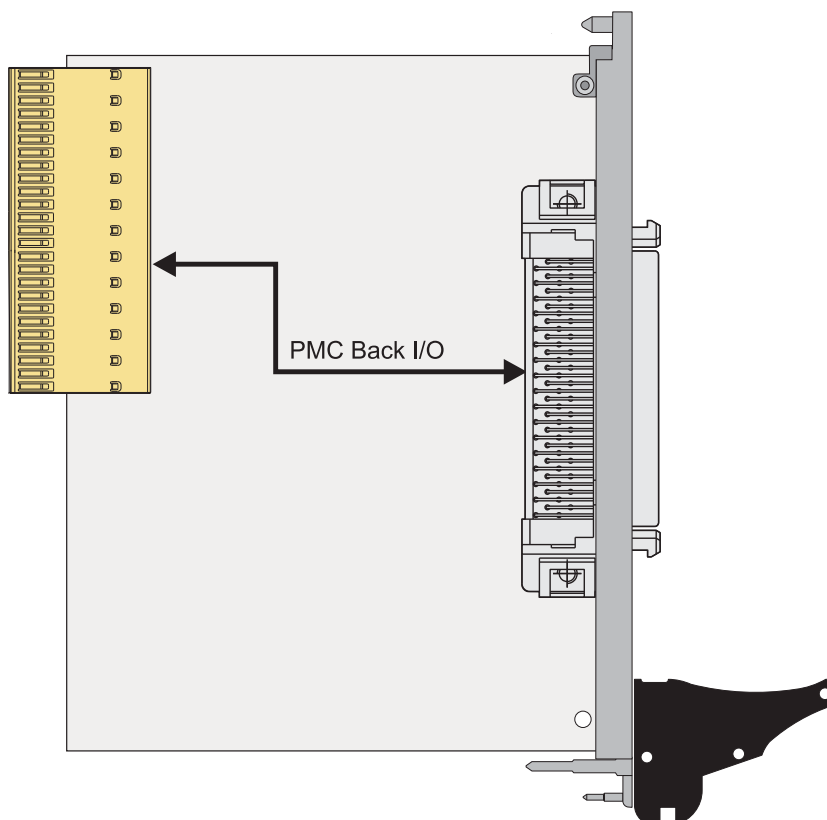


Figure 1-1: Block Diagram

## **2 Technical Specification**

<b>Form Factor</b>	cPCI Rear Transition Module for 3U cPCI PMC Carrier
<b>Board Size</b>	80 mm x 100 mm
<b>Weight</b>	100 g
<b>Front panel</b>	yes
<b>Interface to PMC I/O Lines</b>	HD68 SCSI-3 type Connector located in front panel
<b>MTBF</b>	3060000 h
<b>Temperature Range</b>	Operating: -40°C to +85°C Storage: -40°C to +125°C
<b>Humidity</b>	5-95 % non-condensing

Figure 2-1 : Technical Specification

### 3 Connector X1

X1 Pin	Signal Name	cPCI Backplane	
		Pin	Connector
1	I/O_1	E13	RJ2
2	I/O_2	D13	RJ2
3	I/O_3	C13	RJ2
4	I/O_4	B13	RJ2
5	I/O_5	A13	RJ2
6	I/O_6	E12	RJ2
7	I/O_7	D12	RJ2
8	I/O_8	C12	RJ2
9	I/O_9	B12	RJ2
10	I/O_10	A12	RJ2
11	I/O_11	E11	RJ2
12	I/O_12	D11	RJ2
13	I/O_13	C11	RJ2
14	I/O_14	B11	RJ2
15	I/O_15	A11	RJ2
16	I/O_16	E10	RJ2
17	I/O_17	D10	RJ2
18	I/O_18	C10	RJ2
19	I/O_19	B10	RJ2
20	I/O_20	A10	RJ2
21	I/O_21	E9	RJ2
22	I/O_22	D9	RJ2
23	I/O_23	C9	RJ2
24	I/O_24	B9	RJ2
25	I/O_25	A9	RJ2
26	I/O_26	E8	RJ2
27	I/O_27	D8	RJ2
28	I/O_28	C8	RJ2
29	I/O_29	B8	RJ2
30	I/O_30	A8	RJ2
31	I/O_31	E7	RJ2
32	I/O_32	D7	RJ2
33	I/O_3	C7	RJ2
34	I/O_34	B7	RJ2
35	I/O_35	A7	RJ2
36	I/O_36	E6	RJ2
37	I/O_37	D6	RJ2
38	I/O_38	C6	RJ2
39	I/O_39	B6	RJ2



X1 Pin	Signal Name	cPCI Backplane	
		Pin	Connector
40	I/O_40	A6	RJ2
41	I/O_41	E5	RJ2
42	I/O_42	D5	RJ2
43	I/O_43	C5	RJ2
44	I/O_44	B5	RJ2
45	I/O_45	A5	RJ2
46	I/O_46	E4	RJ2
47	I/O_47	D4	RJ2
48	I/O_48	C4	RJ2
49	I/O_49	B4	RJ2
50	I/O_50	A4	RJ2
51	I/O_51	E3	RJ2
52	I/O_52	D3	RJ2
53	I/O_53	C3	RJ2
54	I/O_54	B3	RJ2
55	I/O_55	A3	RJ2
56	I/O_56	E2	RJ2
57	I/O_57	D2	RJ2
58	I/O_58	C2	RJ2
59	I/O_59	B2	RJ2
60	I/O_60	A2	RJ2
61	I/O_61	E1	RJ2
62	I/O_62	D1	RJ2
63	I/O_63	C1	RJ2
64	I/O_64	B1	RJ2
65	*)	-	-
66	*)	-	-
67	*)	-	-
68	*)	-	-

Figure 3-1 : Connector X1 Pin Assignment

\*) Each of these pins can separately be connected to GND by a 0 Ohm resistor to achieve extended grounding of the I/O signals. By default these pins are left unconnected.

## 4 Compact PCI RJ2

Position	Row					
	A	B	C	D	E	F
22	nc	nc	nc	nc	nc	GND
21	nc	nc	nc	nc	nc	GND
20	nc	nc	nc	nc	nc	GND
19	nc	nc	nc	nc	nc	GND
18	nc	nc	nc	nc	nc	GND
17	nc	nc	nc	nc	nc	GND
16	nc	nc	nc	nc	nc	GND
15	nc	nc	nc	nc	nc	GND
14	nc	nc	nc	nc	nc	GND
13	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	GND
12	I/O_10	I/O_9	I/O_8	I/O_7	I/O_6	GND
11	I/O_15	I/O_14	I/O_13	I/O_12	I/O_11	GND
10	I/O_20	I/O_19	I/O_18	I/O_17	I/O_16	GND
9	I/O_25	I/O_24	I/O_23	I/O_22	I/O_21	GND
8	I/O_30	I/O_29	I/O_28	I/O_27	I/O_26	GND
7	I/O_35	I/O_34	I/O_33	I/O_32	I/O_31	GND
6	I/O_40	I/O_39	I/O_38	I/O_37	I/O_36	GND
5	I/O_45	I/O_44	I/O_43	I/O_42	I/O_41	GND
4	I/O_50	I/O_49	I/O_48	I/O_47	I/O_46	GND
3	I/O_55	I/O_54	I/O_53	I/O_52	I/O_51	GND
2	I/O_60	I/O_59	I/O_58	I/O_57	I/O_56	GND
1	nc	I/O_64	I/O_63	I/O_62	I/O_61	GND

Figure 4-1 : Compact PCI RJ2

# 5 Pin Assignment

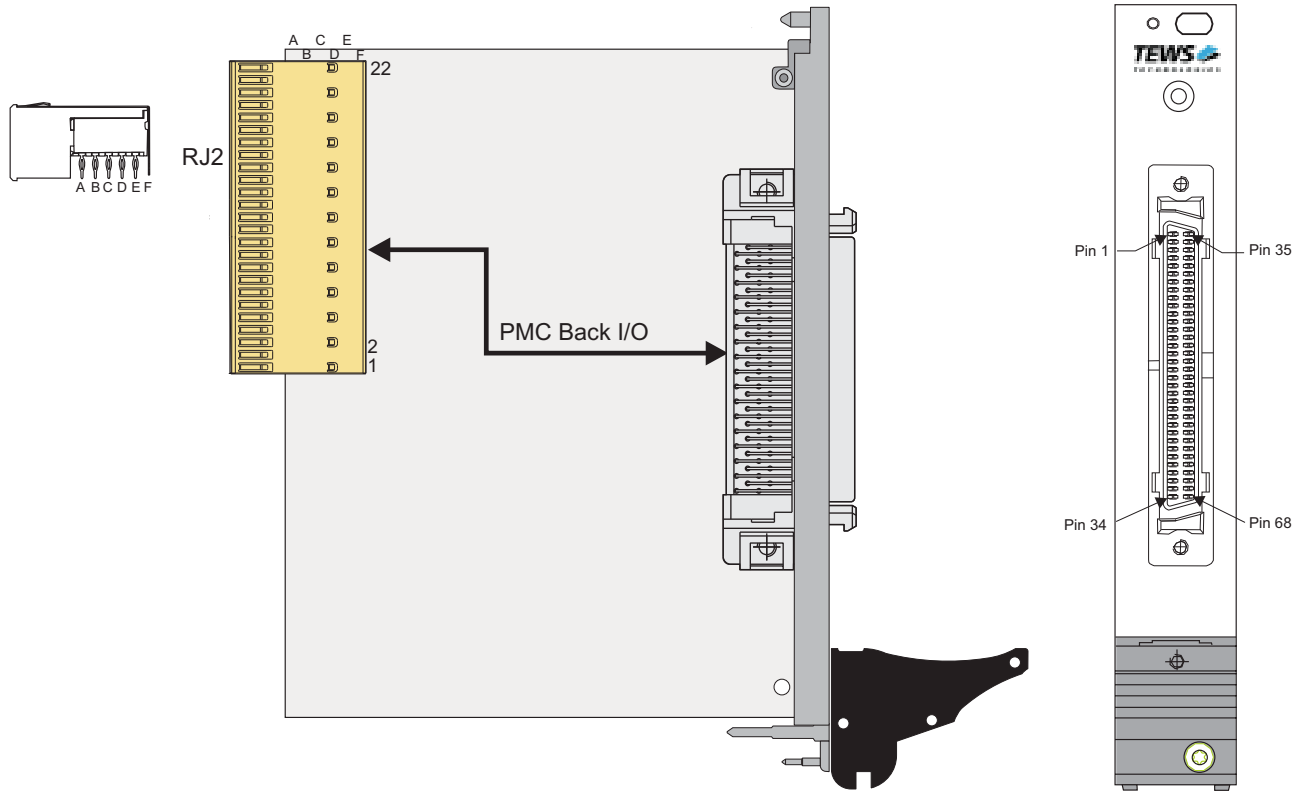


Figure 5-1 : Pin Assignment