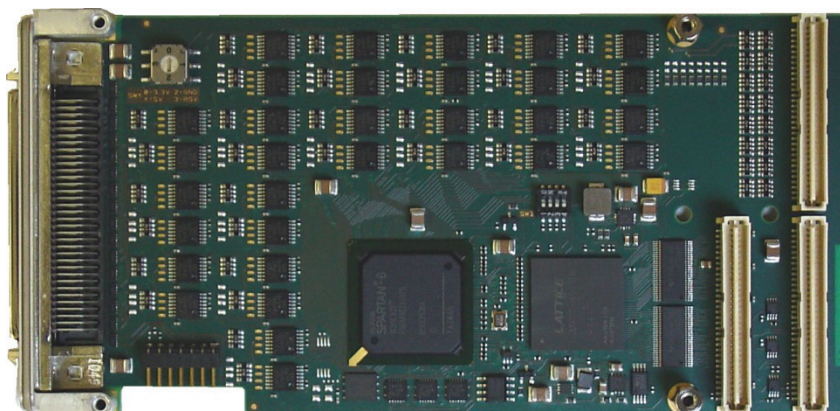


## TPMC634 Re-Configurable FPGA with 64 TTL I/O / 32 Diff. I/O



### Application Information

The TPMC634 is a standard single-width PMC module providing a user configurable Xilinx XC6SLX25 Spartan-6 FPGA.

The TPMC634-10R provides 64 ESD-protected TTL lines using TTL compatible buffers. The TPMC634-11R provides 32 differential I/O lines using ESD-protected EIA-422 / EIA-485 compatible line transceivers. The TPMC634-12R provides a mix of 16 differential EIA-422 / EIA-485 I/O lines and 32 TTL I/O lines. The TPMC634-13R provides 32 differential I/O lines using M-LVDS line transceivers. The TPMC634-14R provides a mix of 16 differential M-LVDS I/O lines and 32 TTL I/O lines.

All I/O lines are individually programmable as input or output. The receivers are always enabled. This allows reading the state of each I/O line at any time (monitoring I/O lines configured as outputs).

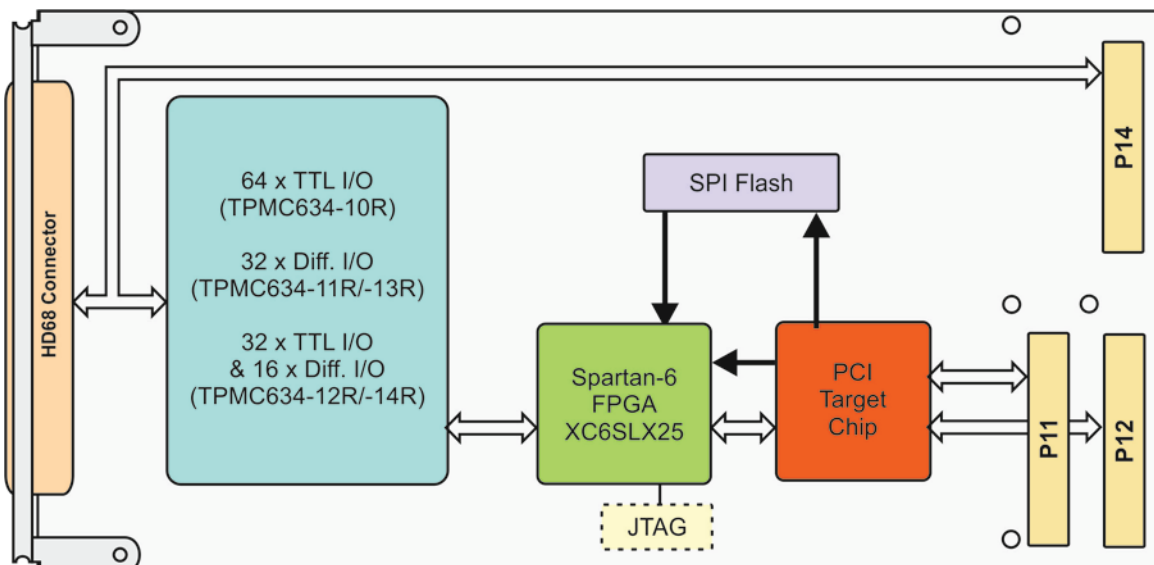
Each TTL I/O line has an on-board pull resistor to a common/shared reference. The pull resistor reference is configurable by an on-board rotary switch to 3.3V, 5V or GND. The differential I/O lines have on-board termination resistors.

The User FPGA is auto-configurable by an on-board serial SPI Flash. Both the User FPGA and the SPI flash for User FPGA configuration are in-system-programmable via the PCI bus. An on-board JTAG header provides access to the user FPGA JTAG port.

PCI configuration space parameters are configurable by an on-board serial EEPROM.

### Technical Information

- Standard single-width 32 bit 33 MHz PCI PMC Module conforming to IEEE P1386.1
- PCI 3.0 compatible Interface
- Universal PCI Signaling Voltage
- Xilinx XC6SLX25 Spartan-6 User FPGA accessible on Local Address/Data Bus
- PCI to Local Bus Interface is handled by the PCI Target Chip
- Programmable EEPROM for PCI Configuration Space Parameters
- In-System-Programmable SPI Flash for User FPGA Configuration
- User FPGA directly In-System-Programmable by Software
- Baud Rate Oscillator available at User FPGA Pin
- I/O options:
  - 64 TTL I/O (-10R)
  - 32 diff. EIA-422 / EIA-485 I/O (-11R)
  - 16 diff. EIA-422 / EIA-485 I/O and 32 TTL I/O (-12R)
  - 32 diff. M-LVDS I/O (-13R)
  - 16 diff. M-LVDS I/O and 32 TTL I/O (-14R)
- 64 I/O lines accessible on both HD68 Front Connector and P14 Rear Connector
- Operating Temperature -40°C to +85°C



### Order Information

#### RoHS Compliant

<b>TPMC634-10R</b>	Re-Configurable FPGA with 64 TTL I/O
<b>TPMC634-11R</b>	Re-Configurable FPGA with 32 Differential EIA-422 / EIA-485 I/O
<b>TPMC634-12R</b>	Re-Configurable FPGA with 16 Differential EIA-422 / EIA-485 I/O and 32 TTL I/O
<b>TPMC634-13R</b>	Re-Configurable FPGA with 32 Differential M-LVDS I/O
<b>TPMC634-14R</b>	Re-Configurable FPGA with 16 Differential M-LVDS I/O and 32 TTL I/O

For the availability of non-RoHS compliant (lead solder) products please contact TEWS.

#### Documentation

<b>TPMC634-DOC</b>	User Manual
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#### Software

<b>TDRV018-SW-25</b>	Integrity Software Support
<b>TDRV018-SW-42</b>	VxWorks Software Support (Legacy and VxBus-Enabled Software Support)
<b>TDRV018-SW-65</b>	Windows Software Support
<b>TDRV018-SW-82</b>	Linux Software Support
<b>TDRV018-SW-95</b>	QNX Software Support

#### Related Products

<b>TA304</b>	Cable Kit for Modules with HD68 SCSI-3 type connector
<b>TPIM003</b>	PIM I/O Module with HD68 SCSI-3 type connector and special pin assignment