The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC680

8 x 8 Bit Digital Inputs/Outputs

(5V TTL)

Version 1.0

User Manual

Issue 1.0.7

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powerBridge Computer

Ehlbeek 15a
30938 Burgwedel
fon 05139-9980-0
fax 05139-9980-49

www.powerbridge.de
info@powerbridge.de

TEWS TECHNOLOGIES GmbH
Am Bahnhof 7
469 Halstenbek, Germany www.tews.com
Phone: +49-(0)4101-4058-0
Fax: +49-(0)4101-4058-19
e-mail: info@tews.com

TPMC680-10R

8 x 8 Bit Digital Inputs/Outputs

(5V TTL)

HD68 front panel connector

P14 Back I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	November 2002
1.1	Changed Byte Order of Port Data Registers	November 2002
1.2	Values of interrupt timing added	October 2003
1.3	Changed description of “Port Data Direction Register”	March 2004
1.4	Description of Back I/O options added, Technical Specification updated	May 2005
1.5	New address TEWS LLC	September 2006
1.0.6	New notation for HW Engineering Documentation Releases	May 2009
1.0.7	General Revision	August 2014

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1 Product Description

The TPMC680 is a standard single-width 32 bit PMC module offering 64 bit of TTL I/O arranged in 8 x 8 bit ports. Direction of the I/O lines is software programmable for each of the 8 bit ports. Each 8 bit port is built up using a TTL bus transceiver. Each line is protected against ESD and overvoltage.

The PLX PCI9030 PCI target chip is used for the PCI interface.

Each input can generate an interrupt on INTA. Signal edge handling is programmable to interrupt on rising and/or falling edge of the input signal. Interrupts can be enabled and disabled for each bit. For interrupt source detection the status of each bit can be read from the Interrupt Status Register.

The TPMC680 supports three basic modes of operation: standard byte I/O with interrupts, 2 x 16 bit port with handshake and 1 x 32 bit port with handshake. The two handshake modes offer double buffered inputs or outputs and interlocked or pulsed handshake output protocol.

In byte I/O mode it is possible to read or write synchronously all 64 lines.

The TPMC680 provides front panel I/O via a HD68 SCSI-3 type connector and rear panel I/O via P14.

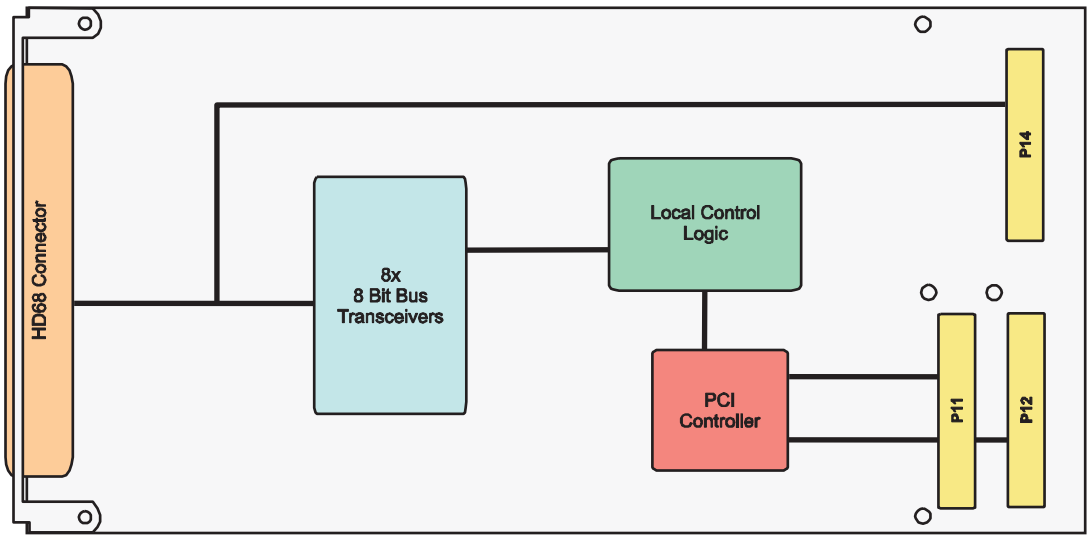

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface	
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size
Electrical Interface	PCI Rev. 2.1 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage
On Board Devices	
PCI Target Chip	PCI9030 (PLX Technology)
Local Control Logic	FPGA Spartan2 XC2S100-5 FG256 I (Xilinx)
Line Transceivers	8 x SN74LV245AT (Texas Instruments)
I/O Interface	
Number of I/O Lines	64 lines arranged in 8 x 8 bit ports (Port 0-7), all lines of one port have the same direction Max. output current per line: -16mA (High level) 16mA (Low level)
I/O Connector	PMC P14 I/O (64 pin Mezzanine Connector): Port 0-6 (ground lines can be changed to signals of Port 7) Front panel HD68 SCSI-3 type Connector: Port 0-7
Physical Data	
Power Requirements	80mA typical @ +3.3V DC 90mA typical (no load) @ +5V DC
Temperature Range	Operating -40 °C to +85 °C Storage -40°C to +125°C
MTBF	392000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.
Humidity	5 – 95 % non-condensing
Weight	76 g

Table 2-1 : Technical Specification

3 Operating Modes

3.1 Byte Wise I/O Mode

In “Byte Wise I/O Mode” there are eight independent 8 bit ports available. All lines of one port have the same direction, which is configured by the corresponding bit in Port Data Direction Register PDDR (see chapter “General Register Space”). Inputs are unbuffered (transparent) and outputs are single buffered. Accesses to the Port Data Registers PDR 0-7 can be 8, 16 or 32 bit wide (see chapter “FPGA Register Space”).

All input lines can trigger an interrupt on the rising and/or falling edge of a signal. To enable interrupts, the interrupt enable bit for rising and/or falling edge of the particular line needs to be set in Positive Edge Interrupt Enable Register PIER0/1 or Negative Interrupt Enable Register NIER0/1 and as well the global interrupt enable bit 0 of Interrupt Status and Control Register ISCR. The Interrupt Status Registers ISR0/1 signal the lines on which an interrupt event occurred. To detect a short pulse as an interrupt event, the pulse should be at least 20ns long. The delay between an edge at the inputs and the falling edge on INTA# is about 40 ns.

If bit 0 of Byte Wise Mode Control Register BWCR is set, the “64 bit Simultaneous Mode” is enabled (see chapter “Byte Wise Mode Register Space”). In this mode Ports 7-4 are buffered for reads and writes, all 64 data lines are updated with a read or write access on Ports 3-0.

The direction of all 64 lines is given by bit 0 of the Port Data Direction Register PDDR (see chapter “General Register Space”).

Accesses to the addresses of Port Data Register PDR 0 or 4 must be 32 bit wide. Figures below “64 bit Simultaneous Input Mode” and “64 bit Simultaneous Output Mode” give examples of a read and write access:

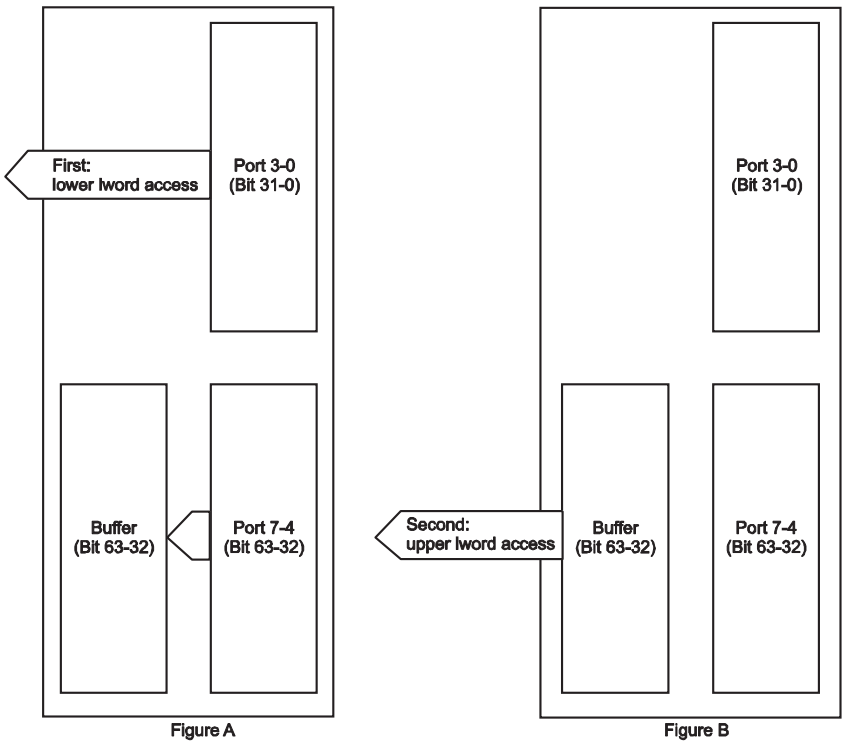

Figure 3-1 : 64 bit Simultaneous Input Mode (Read Access)

- Figure A: The buffer is simultaneously updated from Port 7-4 with a read access to Port 3-0 and
- Figure B: the lword Port 7-4 is read from the buffer.

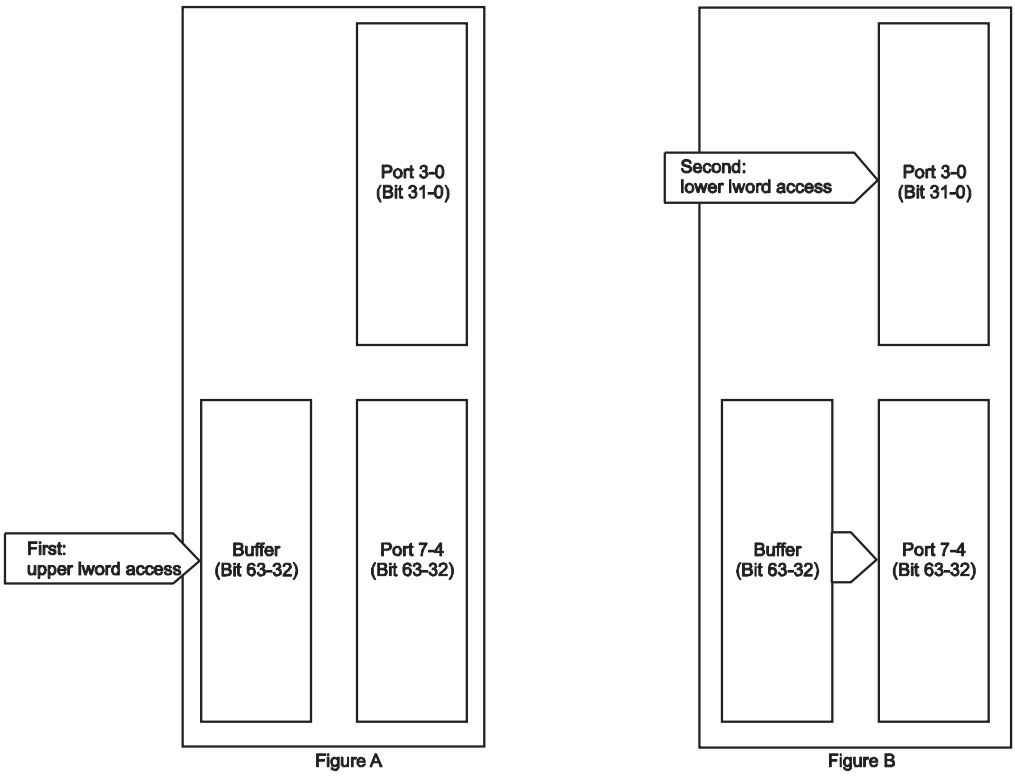

Figure 3-2 : 64 bit Simultaneous Output Mode (Write Access)

- Figure A: Lword for Port 7-4 is written to a buffer and
- Figure B: Port 7-4 is simultaneously updated from the buffer with a write access to Port 3-0.

3.2 Handshake Modes

In a handshake mode transfers are double-buffered. In the primary direction, double buffering allows orderly transfers by using the handshake pins in any of several programmable protocols.

Use of double buffering is most beneficial in situations where a peripheral device and the computer system are capable of transferring data at roughly the same speed. Double buffering allows the fetch operation of the data transmitter to be overlapped with the store operation of the data receiver. Thus, throughput may be greatly enhanced. If there is a large mismatch in transfer capability between the computer and the peripheral, little or no benefit is obtained. In these cases there is no penalty in using double buffering.

Handshake mode 1:

There are two 16 bit double-buffered ports available (port 0/1 and port 2/3). They can alternatively be configured by bit 0 of the Handshake Status and Control Registers HSCR0/1 to behave as byte I/O ports (see chapter “Byte Wise I/O Mode”), if one handshake port is enough.

Bit 0 and 1 of port 4 are used as handshake input signals H1/H3. Thus, if at least one 16 bit port is configured for handshaking, port 4 is set as an input port for H1/H3. The action of the handshake output signals H2/H4 is programmable. For these signals bit 0 and 1 of port 5 are used. Thus, if a handshake output protocol is configured, port 5 is set as an output port.

The H1S/H3S flag, which is bit 7 of the Handshake Status and Control Registers HSCR0/1, gives information about the status of the FIFO. Its behavior depends on the transfer direction and for output direction also the configuration by bit 2 of HSCR0/1 (see below “Output Transfers”). An interrupt is triggered if H1S/H3S flag is set and it is enabled by bit 1 of Handshake Status and Control Register HSCR0/1.

H1 and H2 belong to the 16 bit port on port 0 and H3/H4 belong to port 2.

Handshake mode 2:

The difference to handshake mode 1 is that it provides one 32 bit Handshake Register (on port 0 to 3). Alternative byte I/O is not possible. Therefore port 4 is always an input because of H1 on bit 0. Only Handshake Status and Control Register 0 HSCR0 is evaluated for configuration.

	Handshake Mode 1	**Handshake Mode 2**
Handshake Input	H1: Port 4 Line 0 H3: Port 4 Line 1	H1: Port 4 Line 0
Handshake Output	H2: Port 5 Line 0 H4: Port 5 Line 1	H2: Port 5 Line 0

Input Transfers:

If input direction is set for a handshake port, H1(H3) input signal is used for acquisition of data. Data is buffered on a falling edge of H1(H3). H1S(H3S) is set when any input data has not been read from the FIFO. If the handshake output signals H2(H4) are used, they indicate whether there is room for more data in the FIFO or not.

If H2(H4) output is used, it may be in the interlocked or pulsed input handshake protocol. The protocol is set by bit 5 and 6 of the Handshake Status and Control Registers HSCR0/1.

In the interlocked input handshake protocol signal H2(H4) is cleared when the port input buffers are ready to accept new data. It is set following the falling edge of the H1(H3) input. When ready for new data, H2(H4) is again cleared. When both buffers are full H2(H4) remains high until data is removed

by a read of port data register. Thus, anytime H2(H4) output is low, new input data may be entered by a falling edge on H1(H3). At other times transitions of H1(H3) are ignored.

In the pulsed input handshake protocol signal H2(H4) is cleared in the same way as in the interlocked input protocol, but never remains low longer than four clock cycles. Typically a four-clock cycle pulse is generated. But in the case that a subsequent H1(H3) falling edge occurs before termination of the pulse, H2(H4) is set immediately high. Thus, anytime after a falling edge of the H2(H4) pulse, new data may be entered in the buffers. In the figure below “Input Transfer Timing Diagram” a sample timing diagram is given. The H2(H4) interlocked and pulse input handshake protocols are shown.

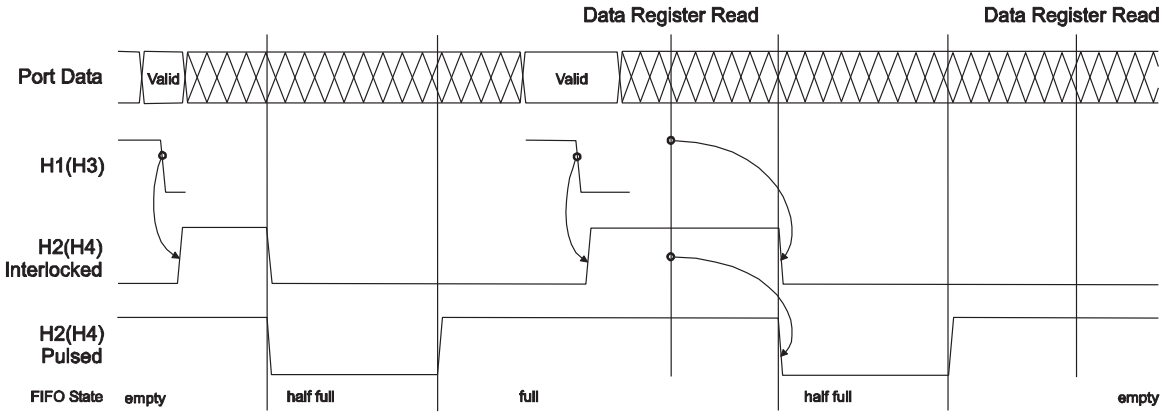

Figure 3-3 : Input Transfer Timing Diagram

Output Transfers:

In case of an output port the peripheral accepts the data by a falling edge on H1/H3, which causes the next data to be moved to the corresponding output. H2(H4) indicates that new data has been moved to the output.

If H2(H4) output is used, it may be in the interlocked or pulsed output handshake protocol. The protocol is set by bit 5 and 6 of the Handshake Status and Control Registers HSCR0/1.

In the interlocked output handshake protocol signal H2(H4) is cleared two clock cycles after data is transferred to the output. The data remains stable and H2(H4) remains low until the next falling edge of the H1(H3) input. At that time H2(H4) goes high. As soon as the next data is available, it is transferred to the output and H2(H4) is cleared. When H2(H4) is high, transitions on H1(H3) have no effect.

When H2(H4) is an output pin in the pulsed output handshake protocol, it is cleared exactly as in the interlocked output protocol, but never remains low longer than four clock cycles. Typically a four-clock cycle pulse is generated. But in the case that a subsequent H1(H3) falling edge occurs before termination of the pulse, H2(H4) is set immediately high, thus shortening the pulse.

The H1S/H3S status bit (Handshake Status and Control Register HSCR0/1, bit 7) may be programmed for two interpretations (by bit 2 of Handshake Status and Control Register HSCR0/1).

- First: The status bit is high when there is at least one buffer in the FIFO that can accept new data. After writing one word/lword of data to the ports, an interrupt service routine could check this bit to determine if it could store another word/lword, thus filling both buffers.
- Second: It is often useful to be able to check whether all of the data has been transferred to the peripheral. The H1S(H3S) status bit is set when both output buffers are empty.

The maximum delay time between a falling edge on H1 and the new valid output data can be up to 150ns, including the propagation delay of the bus transceivers. This delay is calculated under worst-case conditions over the whole temperature range with C_L=150pF. A typical delay in practice would be about 100ns.

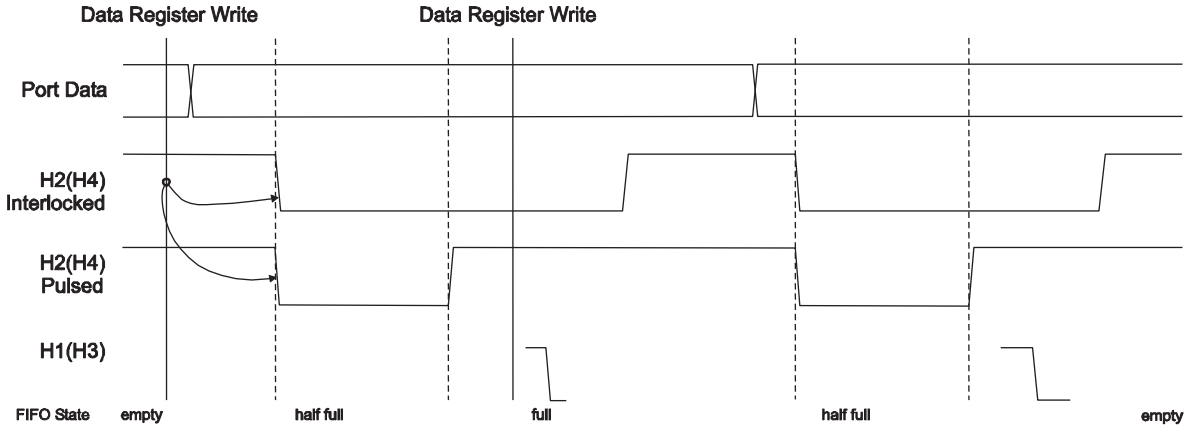

Figure 3-4 : Output Transfer Timing Diagram

4 Local Space Addressing

4.1 PCI9030 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9030 local spaces.

PCI9030 Local Space	PCI9030 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	2 (0x18)	MEM	256	32	BIG	FPGA Register Address Space
1	3 (0x1C)	-	-	-	-	Not Used
2	4 (0x20)	-	-	-	-	Not Used
3	5 (0x24)	-	-	-	-	Not Used

Table 4-1 : PCI9030 Local Space Configuration

4.2 FPGA Register Space

PCI Base Address: **PCI9030 PCI Base Address 2 (Offset 0x18 in PCI Configuration Space).**

Offset to PCI Base Address 2	Register Name	Size (Bit)
GENERAL REGISTER SPACE		
0x00	MODE REGISTER (MR)	32
0x04	PORT DATA DIRECTION REGISTER (PDDR)	32
0x08	INTERRUPT STATUS AND CONTROL REGISTER (ISCR)	32
0x0C	Reserved	32
BYTE WISE MODE REGISTER SPACE		
0x10	BYTE WISE CONTROL REGISTER (BWCR)	32
0x14	POSITIVE EDGE INTERRUPT ENABLE REGISTER 0 (PIER0)	32
0x18	POSITIVE EDGE INTERRUPT ENABLE REGISTER 1 (PIER1)	32
0x1C	NEGATIVE EDGE INTERRUPT ENABLE REGISTER 0 (NIER0)	32
0x20	NEGATIVE EDGE INTERRUPT ENABLE REGISTER 1 (NIER1)	32
0x24	INTERRUPT STATUS REGISTER 0 (ISR0)	32
0x28	INTERRUPT STATUS REGISTER 1 (ISR1)	32
0x2C	Reserved	32
HANDSHAKE MODE REGISTER SPACE		
0x30	HANDSHAKE STATUS AND CONTROL REGISTER 0 (HSCR0)	32
0x34	HANDSHAKE STATUS AND CONTROL REGISTER 1 (HSCR1)	32
0x38	Reserved	32
0x3C	Reserved	32
PORT REGISTER SPACE		
0x40 … 0x47	Mode dependent (see following tables)	
0x48 … 0xFF	Reserved	-

Table 4-2 : FPGA Register Space

Possible access widths of port register accesses for each mode:

Port Register Space for Byte Wise Mode		
Offset to PCI Base Address 2	**Register Name**	**Size (Bit)**
0x40	PORT DATA REGISTER 7 (PDR7)	8, 16 or 32
0x41	PORT DATA REGISTER 6 (PDR6)	
0x42	PORT DATA REGISTER 5 (PDR5)	
0x43	PORT DATA REGISTER 4 (PDR4)	
0x44	PORT DATA REGISTER 3 (PDR3)	8, 16 or 32
0x45	PORT DATA REGISTER 2 (PDR2)	
0x46	PORT DATA REGISTER 1 (PDR1)	
0x47	PORT DATA REGISTER 0 (PDR0)	

Table 4-3 : Port Register Space for Byte Wise Mode

Port Register Space for 64 bit Simultaneous Mode		
Offset to PCI Base Address 2	**Register Name**	**Size (Bit)**
0x40	PORT DATA REGISTER 7-4 (PDR7-4)	32
0x44	PORT DATA REGISTER 3-0 (PDR3-0)	32

Table 4-4 : Port Register Space for 64 bit Simultaneous Mode

Port Register Space for 16 bit Handshake Mode 1 (both ports in Byte Wise Mode, HSCR0/1 bit 0 clear)		
Offset to PCI Base Address 2	**Register Name**	**Size (Bit)**
0x40	PORT DATA REGISTER 7 (PDR7)	8, 16 or 32
0x41	PORT DATA REGISTER 6 (PDR6)	
0x42	PORT DATA REGISTER 5 (PDR5)	
0x43	PORT DATA REGISTER 4 (PDR4)	
0x44	PORT DATA REGISTER 3 (PDR3)	8, 16 or 32
0x45	PORT DATA REGISTER 2 (PDR2)	
0x46	PORT DATA REGISTER 1 (PDR1)	
0x47	PORT DATA REGISTER 0 (PDR0)	

Table 4-5 : Port Register Space for 16 bit Handshake Mode 1 (both ports Byte Wise Mode)

Port Register Space for 16 bit Handshake Mode 1 (Port 0/1 in Handshake Mode, HSCR0 bit 0 set; Port 2 and 3 in Byte Wise Mode, HSCR1 bit 0 clear)

Offset to PCI Base Address 2	Register Name	Size (Bit)
0x40	PORT DATA REGISTER 7 (PDR7)	8, 16 or 32
0x41	PORT DATA REGISTER 6 (PDR6)	
0x42	PORT DATA REGISTER 5 (PDR5), output if H2 used	
0x43	PORT DATA REGISTER 4 (PDR4), always input	
0x44	PORT DATA REGISTER 3 (PDR3)	8, 16
0x45	PORT DATA REGISTER 2 (PDR2)	
0x47	PORT DATA REGISTER 0-1 (PDR0-1)	16

Table 4-6 : Port Register Space for 16 bit Handshake Mode 1
(Port 0/1 Handshake Mode Port 2/3 Byte Wise Mode)

Port Register Space for 16 bit Handshake Mode 1 (Port 0 and 1 in Byte Wise Mode, HSCR0 bit 0 clear; Port 2/3 in Handshake Mode, HSCR1 bit 0 set)		
Offset to PCI Base Address 2	**Register Name**	**Size (Bit)**
0x40	PORT DATA REGISTER 7 (PDR7)	8, 16 or 32
0x41	PORT DATA REGISTER 6 (PDR6)	
0x42	PORT DATA REGISTER 5 (PDR5), output if H4 used	
0x43	PORT DATA REGISTER 4 (PDR4), always input	
0x44	PORT DATA REGISTER 2-3 (PDR2-3)	16
0x46	PORT DATA REGISTER 1 (PDR1)	8, 16
0x47	PORT DATA REGISTER 0 (PDR0)	

Table 4-7 : Port Register Space for 16 bit Handshake Mode 1
(Port 0/1 Byte Wise Mode, Port 2/3 Handshake Mode)

Port Register Space for 16 bit Handshake Mode 1 (both ports in Handshake Mode)		
Offset to PCI Base Address 2	**Register Name**	**Size (Bit)**
0x40	PORT DATA REGISTER 7 (PDR7)	8, 16 or 32
0x41	PORT DATA REGISTER 6 (PDR6)	
0x42	PORT DATA REGISTER 5 (PDR5), output if H2/H4 used	
0x43	PORT DATA REGISTER 4 (PDR4), always input	
0x44	PORT DATA REGISTER 2-3 (PDR2-3)	16
0x46	PORT DATA REGISTER 0-1 (PDR0-1)	16

Table 4-8 : Port Register Space for 16 bit Handshake Mode 1 (both ports Handshake Mode)

Port Register Space for 32 bit Handshake Mode 2		
Offset to PCI Base Address 2	**Register Name**	**Size**

		(Bit)
0x40	PORT DATA REGISTER 7 (PDR7)	8, 16 or 32
0x41	PORT DATA REGISTER 6 (PDR6)	
0x42	PORT DATA REGISTER 5 (PDR5), output if H2 used	
0x43	PORT DATA REGISTER 4 (PDR4), always input	
0x44	PORT DATA REGISTER 0-3 (PDR0-3)	32

Table 4-9 : Port Register Space for 32 bit Handshake Mode 2

4.2.1 General Register Space

4.2.1.1 Mode Register (MR; 0x00)

Bit	Symbol	Description	Access	Reset Value
31:3	-	Reserved (0 for reads)	-	0
2:0	MODE	000 : Byte Wise I/O Mode 001 : Handshake Mode 1 (two 16 bit registers) 010 : Handshake Mode 2 (one 32 bit register)	R/W	0

Table 4-10: Mode Register (MR)

4.2.1.2 Port Data Direction Register (PDDR; 0x04)

All 8 lines of one port have the same direction.

Bit	Symbol	Description	Access	Reset Value
31: 8	-	Reserved (0 for reads)	-	0
7	PORT7_DIR	Port 0-7 Data Direction 0 : Port is Input 1 : Port is Output	R/W	0
6	PORT6_DIR			
5	PORT5_DIR			
4	PORT4_DIR			
3	PORT3_DIR			
2	PORT2_DIR			
1	PORT1_DIR			
0	PORT0_DIR			

Table 4-11: Port Data Direction Register (PDDR)

In a Handshake Mode the direction of port 4 is always input because of H1(H3). The direction of port 5 is output only when H2(H4) is used.

In Handshake Mode 1, port 1 has the same direction as port 0, port 3 has the same direction as port 2 (no byte wise I/O). In Handshake Mode 2 port 1-3 have the same direction as port 0.

When changing from a Handshake Mode to Byte Wise Mode, no changes are made in PDDR.

In 64 bit Simultaneous Mode all ports have the direction of port 0.

When changing from 64 bit Simultaneous Mode to Byte Wise Mode, no changes are made in PDDR.

4.2.1.3 Interrupt Status and Control Register (ISCR; 0x08)

Bit	Symbol	Description	Access	Reset Value
31..8	-	Reserved (0 for reads)	-	0
7	GLOBAL_INT	Global Interrupt Request Status 0 : no active Interrupt Request 1 : active Interrupt Request	R	0
6	-	Reserved (0 for reads)	-	0
5				
4				
3				
2				
1				
0	GLOB_INT_EN	Global Interrupt Enable 0 : Interrupts disabled 1 : Interrupts enabled	R/W	0

Table 4-12: Interrupt Status and Control Register (ISCR)

4.2.2 Byte Wise Mode Register Space

4.2.2.1 Byte Wise Mode Control Register (BWCR; 0x10)

Bit	Symbol	Description	Access	Reset Value
31..1	-	Reserved (0 for reads)	-	0
0	64BIT_MODE_EN	64 bit Simultaneous Mode Enable 0 : 64 bit Mode disabled 1 : 64 bit Mode enabled	R/W	0

Table 4-13: Byte Wise Mode Control Register (BWCR)

In “64 bit Simultaneous Input Mode” the lower 32 bits are buffered while reading the upper 32 bits. When the lower 32 bits are read, the values are taken from the buffer.

In “64 bit Simultaneous Output Mode” a long word write to port 7 writes to the buffer. When writing to the upper 32 bits, data from the buffer is written to the lower 32 port bits.

4.2.2.2 Positive Edge Interrupt Enable Register 0 (PIER0; 0x14)

Bit	Symbol	Description	Access	Reset Value
31	PORT7_INTP_7	Port 7 Line 0-7 Rising Edge Interrupt Enable: 0 = disabled 1 = enabled	R/W	0
30	PORT7_INTP_6			
29	PORT7_INTP_5			
28	PORT7_INTP_4			
27	PORT7_INTP_3			
26	PORT7_INTP_2			
25	PORT7_INTP_1			
24	PORT7_INTP_0			
23	PORT6_INTP_7	Port 6 Line 0-7 Rising Edge Interrupt Enable: 0 = disabled 1 = enabled	R/W	0
22	PORT6_INTP_6			
21	PORT6_INTP_5			
20	PORT6_INTP_4			
19	PORT6_INTP_3			
18	PORT6_INTP_2			
17	PORT6_INTP_1			
16	PORT6_INTP_0			
15	PORT5_INTP_7	Port 5 Line 0-7 Rising Edge Interrupt Enable: 0 = disabled 1 = enabled	R/W	0
14	PORT5_INTP_6			
13	PORT5_INTP_5			
12	PORT5_INTP_4			
11	PORT5_INTP_3			
10	PORT5_INTP_2			
9	PORT5_INTP_1			
8	PORT5_INTP_0			
7	PORT4_INTP_7	Port 4 Line 0-7 Rising Edge Interrupt Enable: 0 = disabled 1 = enabled	R/W	0
6	PORT4_INTP_6			
5	PORT4_INTP_5			
4	PORT4_INTP_4			
3	PORT4_INTP_3			
2	PORT4_INTP_2			
1	PORT4_INTP_1			
0	PORT4_INTP_0			

Table 4-14: Positive Edge Interrupt Enable Register 0 (PIER0)

4.2.2.3 Positive Edge Interrupt Enable Register 1 (PIER1; 0x18)

Bit	Symbol	Description	Access	Reset Value
31	PORT3_INTP_7	Port 3 Line 0-7 Rising Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
30	PORT3_INTP_6			
29	PORT3_INTP_5			
28	PORT3_INTP_4			
27	PORT3_INTP_3			
26	PORT3_INTP_2			
25	PORT3_INTP_1			
24	PORT3_INTP_0			
23	PORT2_INTP_7	Port 2 Line 0-7 Rising Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
22	PORT2_INTP_6			
21	PORT2_INTP_5			
20	PORT2_INTP_4			
19	PORT2_INTP_3			
18	PORT2_INTP_2			
17	PORT2_INTP_1			
16	PORT2_INTP_0			
15	PORT1_INTP_7	Port 1 Line 0-7 Rising Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
14	PORT1_INTP_6			
13	PORT1_INTP_5			
12	PORT1_INTP_4			
11	PORT1_INTP_3			
10	PORT1_INTP_2			
9	PORT1_INTP_1			
8	PORT1_INTP_0			
7	PORT0_INTP_7	Port 0 Line 0-7 Rising Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
6	PORT0_INTP_6			
5	PORT0_INTP_5			
4	PORT0_INTP_4			
3	PORT0_INTP_3			
2	PORT0_INTP_2			
1	PORT0_INTP_1			
0	PORT0_INTP_0			

Table 4-15: Positive Edge Interrupt Enable Register 1 (PIER1)

4.2.2.4 Negative Edge Interrupt Enable Register 0 (NIER0; 0x1C)

Bit	Symbol	Description	Access	Reset Value
31	PORT7_INTN_7	Port 7 Line 0-7 Falling Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
30	PORT7_INTN_6			
29	PORT7_INTN_5			
28	PORT7_INTN_4			
27	PORT7_INTN_3			
26	PORT7_INTN_2			
25	PORT7_INTN_1			
24	PORT7_INTN_0			
23	PORT6_INTN_7	Port 6 Line 0-7 Falling Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
22	PORT6_INTN_6			
21	PORT6_INTN_5			
20	PORT6_INTN_4			
19	PORT6_INTN_3			
18	PORT6_INTN_2			
17	PORT6_INTN_1			
16	PORT6_INTN_0			
15	PORT5_INTN_7	Port 5 Line 0-7 Falling Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
14	PORT5_INTN_6			
13	PORT5_INTN_5			
12	PORT5_INTN_4			
11	PORT5_INTN_3			
10	PORT5_INTN_2			
9	PORT5_INTN_1			
8	PORT5_INTN_0			
7	PORT4_INTN_7	Port 4 Line 0-7 Falling Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
6	PORT4_INTN_6			
5	PORT4_INTN_5			
4	PORT4_INTN_4			
3	PORT4_INTN_3			
2	PORT4_INTN_2			
1	PORT4_INTN_1			
0	PORT4_INTN_0			

Table 4-16: Negative Edge Interrupt Enable Register 0 (NIER0)

4.2.2.5 Negative Edge Interrupt Enable Register 1 (NIER1; 0x20)

Bit	Symbol	Description	Access	Reset Value
31	PORT3_INTN_7	Port 3 Line 0-7 Falling Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
30	PORT3_INTN_6			
29	PORT3_INTN_5			
28	PORT3_INTN_4			
27	PORT3_INTN_3			
26	PORT3_INTN_2			
25	PORT3_INTN_1			
24	PORT3_INTN_0			
23	PORT2_INTN_7	Port 2 Line 0-7 Falling Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
22	PORT2_INTN_6			
21	PORT2_INTN_5			
20	PORT2_INTN_4			
19	PORT2_INTN_3			
18	PORT2_INTN_2			
17	PORT2_INTN_1			
16	PORT2_INTN_0			
15	PORT1_INTN_7	Port 1 Line 0-7 Falling Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
14	PORT1_INTN_6			
13	PORT1_INTN_5			
12	PORT1_INTN_4			
11	PORT1_INTN_3			
10	PORT1_INTN_2			
9	PORT1_INTN_1			
8	PORT1_INTN_0			
7	PORT0_INTN_7	Port 0 Line 0-7 Falling Edge Interrupt Enable 0 = disabled 1 = enabled	R/W	0
6	PORT0_INTN_6			
5	PORT0_INTN_5			
4	PORT0_INTN_4			
3	PORT0_INTN_3			
2	PORT0_INTN_2			
1	PORT0_INTN_1			
0	PORT0_INTN_0			

Table 4-17: Negative Edge Interrupt Enable Register 1 (NIER1)

4.2.2.6 Interrupt Status Register 0 (ISR0; 0x24)

The Interrupt Status Register 0 signals the lines on which an interrupt event occurred.

Bit	Symbol	Description	Access	Reset Value
31	PORT7_INT_7	Port 7 Line 0-7 Interrupt Request Status 0 = no active interrupt request 1 = active interrupt request	R/W	0
30	PORT7_INT_6			
29	PORT7_INT_5			
28	PORT7_INT_4			
27	PORT7_INT_3			
26	PORT7_INT_2			
25	PORT7_INT_1			
24	PORT7_INT_0			
23	PORT6_INT_7	Port 6 Line 0-7 Interrupt Request Status 0 = no active interrupt request 1 = active interrupt request	R/W	0
22	PORT6_INT_6			
21	PORT6_INT_5			
20	PORT6_INT_4			
19	PORT6_INT_3			
18	PORT6_INT_2			
17	PORT6_INT_1			
16	PORT6_INT_0			
15	PORT5_INT_7	Port 5 Line 0-7 Interrupt Request Status 0 = no active interrupt request 1 = active interrupt request	R/W	0
14	PORT5_INT_6			
13	PORT5_INT_5			
12	PORT5_INT_4			
11	PORT5_INT_3			
10	PORT5_INT_2			
9	PORT5_INT_1			
8	PORT5_INT_0			
7	PORT4_INT_7	Port 4 Line 0-7 Interrupt Request Status 0 = no active interrupt request 1 = active interrupt request	R/W	0
6	PORT4_INT_6			
5	PORT4_INT_5			
4	PORT4_INT_4			
3	PORT4_INT_3			
2	PORT4_INT_2			
1	PORT4_INT_1			
0	PORT4_INT_0			

Table 4-18: Interrupt Status Register 0 (ISR0)

All interrupt sources are mapped to the PCI9030 LINT1# local interrupt input. The PCI9030 LINT1# local interrupt input is used in active low-level sensitive mode. The PCI9030 LINT2# local interrupt input is not used.

Interrupt request flags are acknowledged by writing '1' to the corresponding bit in ISR0.

4.2.2.7 Interrupt Status Register 1 (ISR1; 0x28)

The Interrupt Status Register 1 signals the lines on which an interrupt event occurred.

Bit	Symbol	Description	Access	Reset Value
31	PORT3_INT_7	Port 3 Line 0-7 Interrupt Request Status 0 = no active interrupt request 1 = active interrupt request	R/W	0
30	PORT3_INT_6			
29	PORT3_INT_5			
28	PORT3_INT_4			
27	PORT3_INT_3			
26	PORT3_INT_2			
25	PORT3_INT_1			
24	PORT3_INT_0			
23	PORT2_INT_7	Port 2 Line 0-7 Interrupt Request Status 0 = no active interrupt request 1 = active interrupt request	R/W	0
22	PORT2_INT_6			
21	PORT2_INT_5			
20	PORT2_INT_4			
19	PORT2_INT_3			
18	PORT2_INT_2			
17	PORT2_INT_1			
16	PORT2_INT_0			
15	PORT1_INT_7	Port 1 Line 0-7 Interrupt Request Status 0 = no active interrupt request 1 = active interrupt request	R/W	0
14	PORT1_INT_6			
13	PORT1_INT_5			
12	PORT1_INT_4			
11	PORT1_INT_3			
10	PORT1_INT_2			
9	PORT1_INT_1			
8	PORT1_INT_0			
7	PORT0_INT_7	Port 0 Line 0-7 Interrupt Request Status 0 = No active interrupt request 1 = Active interrupt request	R/W	0
6	PORT0_INT_6			
5	PORT0_INT_5			
4	PORT0_INT_4			
3	PORT0_INT_3			
2	PORT0_INT_2			
1	PORT0_INT_1			
0	PORT0_INT_0			

Table 4-19: Interrupt Status Register 1(ISR1)

All interrupt sources are mapped to the PCI9030 LINT1# local interrupt input. The PCI9030 LINT1# local interrupt input is used in active low-level sensitive mode. The PCI9030 LINT2# local interrupt input is not used.

Interrupt request flags are acknowledged by writing '1' to the corresponding bit in ISR1.

4.2.3 Handshake Mode Register Space

See chapter “Handshake Modes” for a detailed description of the modes and the configuration bits in the Handshake Status and Control Registers.

4.2.3.1 Handshake Status and Control Register 0 (HSCR0; 0x30)

Bit	Symbol	Description	Access	Reset Value
31..8	-	Reserved (‘0’ for reads)	-	0
7	H1S	H1S Flag 0 : no H1S Event 1 : active H1S Event	R	0
6..5	PORT0_HS	H2 Handshake Protocol 00 : None 10 : Interlocked Handshake Protocol 11 : Pulsed Handshake Protocol	R/W	0
4	-	Reserved (‘0’ for reads)	-	0
3	-	Reserved (‘0’ for reads)	-	0
2	H1S_MODE	H1S Mode (Port 0 Output) 0 : H1S set if FIFO Not Full 1 : H1S set if FIFO Empty	R/W	0
1	H1S_INT_EN	H1S Interrupt Enable 0 : Interrupt disabled 1 : Interrupt enabled	R/W	0
0	PORT0_MODE	Port 0 Sub mode 0 : Byte I/O Mode 1 : Handshake Mode	R/W	0

Table 4-20: Handshake Status and Control Register 0 (HSCR0)

The Handshake Status and Control Register 0 controls 16 bit Handshake Port on Ports 0/1 and 32 bit Handshake Port on Ports 0-3.

Port 0 Sub mode (bit 0) is only valid in ‘Handshake 1’ mode.

4.2.3.2 Handshake Status and Control Register 1 (HSCR1; 0x34)

Bit	Symbol	Description	Access	Reset Value
31..8	-	Reserved ('0' for reads)	-	0
7	H3S	H3S Flag 0 : no H3S Event 1 : active H3S Event	R	0
6..5	PORT1_HS	H4 Handshake Protocol 00 : none 10 : Interlocked Handshake Protocol 11 : Pulsed Handshake Protocol	R/W	0
4	-	Reserved ('0' for reads)	-	0
3	-	Reserved ('0' for reads)	-	0
2	H3S_MODE	H3S Mode (Handshake Port 1 Output) 0 : H3S set if FIFO Not Full 1 : H3S set if FIFO Empty	R/W	0
1	H3S_INT_EN	H3S Interrupt Enable 0 : Interrupt disabled 1 : Interrupt enabled	R/W	0
0	PORT2_MODE	Handshake Port 1 Sub mode 0 : Byte I/O Mode 1 : Handshake Mode	R/W	0

Table 4-21: Handshake Status and Control Register 1(HSCR1)

The Handshake Status and Control Register 1 controls 16 bit Handshake Port on Ports 2/3. HSCR1 is not valid in 'Handshake Mode 2', because only one Handshake Register is used.

4.2.4 Port Data Register Space

See figures in chapter „Port Register Space“ for allowed addresses and access width of port registers for each mode.

In “64 bit Simultaneous Input Mode” the lower 32 bits are buffered while reading the upper 32 bits. When the lower 32 bits are read, the values are taken from the buffer.

In “64 bit Simultaneous Output Mode” a long word write to port 7 writes to the buffer. When writing to the upper 32 bits, data from the buffer is written to the lower 32 port bits.

4.2.4.1 Port Data Register 7 (PDR7; 0x40)

Bit	Symbol	Description	Access	Reset Value
7	PORT7_BIT_7	Port 7 bit 0-7 Data	R/W	0
6	PORT7_BIT_6			
5	PORT7_BIT_5			
4	PORT7_BIT_4			
3	PORT7_BIT_3			
2	PORT7_BIT_2			
1	PORT7_BIT_1			
0	PORT7_BIT_0			

Table 4-22: Port Data Register 7 (PDR7)

4.2.4.2 Port Data Register 6 (PDR6; 0x41)

Bit	Symbol	Description	Access	Reset Value
7	PORT6_BIT_7	Port 6 bit 0-7 Data	R/W	0
6	PORT6_BIT_6			
5	PORT6_BIT_5			
4	PORT6_BIT_4			
3	PORT6_BIT_3			
2	PORT6_BIT_2			
1	PORT6_BIT_1			
0	PORT6_BIT_0			

Table 4-23: Port Data Register 6 (PDR6)

4.2.4.3 Port Data Register 5 (PDR5; 0x42)

Bit	Symbol	Description	Access	Reset Value
7	PORT5_BIT_7	Port 5 bit 0-7 Data	R/W	0
6	PORT5_BIT_6			
5	PORT5_BIT_5			
4	PORT5_BIT_4			
3	PORT5_BIT_3			
2	PORT5_BIT_2			
1	PORT5_BIT_1			
0	PORT5_BIT_0			

Table 4-24: Port Data Register 5 (PDR5)

4.2.4.4 Port Data Register 4 (PDR4; 0x43)

Bit	Symbol	Description	Access	Reset Value
7	PORT4_BIT_7	Port 4 bit 0-7 Data	R/W	0
6	PORT4_BIT_6			
5	PORT4_BIT_5			
4	PORT4_BIT_4			
3	PORT4_BIT_3			
2	PORT4_BIT_2			
1	PORT4_BIT_1			
0	PORT4_BIT_0			

Table 4-25: Port Data Register 4 (PDR4)

4.2.4.5 Port Data Register 3 (PDR3; 0x44)

Bit	Symbol	Description	Access	Reset Value
7	PORT3_BIT_7	Port 3 bit 0-7 Data	R/W	0
6	PORT3_BIT_6			
5	PORT3_BIT_5			
4	PORT3_BIT_4			
3	PORT3_BIT_3			
2	PORT3_BIT_2			
1	PORT3_BIT_1			
0	PORT3_BIT_0			

Table 4-26: Port Data Register 3 (PDR3)

4.2.4.6 Port Data Register 2 (PDR2; 0x45)

Bit	Symbol	Description	Access	Reset Value
7	PORT2_BIT_7	Port 2 bit 0-7 Data	R/W	0
6	PORT2_BIT_6			
5	PORT2_BIT_5			
4	PORT2_BIT_4			
3	PORT2_BIT_3			
2	PORT2_BIT_2			
1	PORT2_BIT_1			
0	PORT2_BIT_0			

Table 4-27: Port Data Register 2 (PDR2)

4.2.4.7 Port Data Register 1 (PDR1; 0x46)

Bit	Symbol	Description	Access	Reset Value
7	PORT1_BIT_7	Port 1 bit 0-7 Data	R/W	0
6	PORT1_BIT_6			
5	PORT1_BIT_5			
4	PORT1_BIT_4			
3	PORT1_BIT_3			
2	PORT1_BIT_2			
1	PORT1_BIT_1			
0	PORT1_BIT_0			

Table 4-28: Port Data Register 1 (PDR1)

4.2.4.8 Port Data Register 0 (PDR0; 0x47)

Bit	Symbol	Description	Access	Reset Value
7	PORT0_BIT_7	Port 0 bit 0-7 Data	R/W	0
6	PORT0_BIT_6			
5	PORT0_BIT_5			
4	PORT0_BIT_4			
3	PORT0_BIT_3			
2	PORT0_BIT_2			
1	PORT0_BIT_1			
0	PORT0_BIT_0			

Table 4-29: Port Data Register 0 (PDR0)

5 PCI9030 Target Chip

5.1 PCI Configuration Registers (PCR)

5.1.1 PCI9030 Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	02A8 1498
0x04	Status		Command		Y	0280 0000
0x08	Class Code			Revision ID	N	118000 00
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers				Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers				Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0				Y	FFFFFF00
0x1C	PCI Base Address 3 for Local Address Space 1				Y	00000000
0x20	PCI Base Address 4 for Local Address Space 2				Y	00000000
0x24	PCI Base Address 5 for Local Address Space 3				Y	00000000
0x28	PCI Cardbus Information Structure Pointer				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	000A 1498
0x30	PCI Base Address for Local Expansion ROM				Y	00000000
0x34	Reserved			New Cap. Ptr.	N	000000 40
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00
0x40	PM Cap.		PM Nxt Cap.	PM Cap. ID	N	4801 00 01
0x44	PM Data	PM CSR EXT	PM CSR		Y	00 00 0000
0x48	Reserved	HS CSR	HS Nxt Cap.	HS Cap. ID	Y[23:16]	00 00 00 06
0x4C	VPD Address		VPD Nxt Cap.	VPD Cap. ID	Y[31:16]	0000 00 03
0x50	VPD Data				Y	00000000

Table 5-1 : PCI9030 Header

5.1.2 PCI Base Address Initialization

PCI Base Address Initialization is scope of the PCI host software.

PCI9030 PCI Base Address Initialization:

1. Write 0xFFFF_FFFF to the PCI9030 PCI Base Address Register.
2. Read back the PCI9030 PCI Base Address Register.
3. For PCI Base Address Registers 0:5, check bit 0 for PCI Address Space:

   Bit 0 = '0' requires PCI Memory Space mapping

   Bit 0 = '1' requires PCI I/O Space mapping

   For the PCI Expansion ROM Base Address Register, check bit 0 for usage:

   Bit 0 = '0': Expansion ROM not used

   Bit 0 = '1': Expansion ROM used
4. For PCI I/O Space mapping, starting at bit location 2, the first bit set determines the size of the required PCI I/O Space size.

   For PCI Memory Space mapping, starting at bit location 4, the first bit set to '1' determines the size of the required PCI Memory Space size.

   For PCI Expansion ROM mapping, starting at bit location 11, the first bit set to '1' determines the required PCI Expansion ROM size.

   For example, if bit 5 of a PCI Base Address Register is detected as the first bit set to '1', the PCI9030 is requesting a 32-byte space (address bits 4:0 are not part of base address decoding).
5. Determine the base address and write the base address to the PCI9030 PCI Base Address Register. For PCI Memory Space mapping the mapped address region must comply with the definition of bits 3:1 of the PCI9030 PCI Base Address Register.

After programming the PCI9030 PCI Base Address Registers, the software must enable the PCI9030 for PCI I/O and/or PCI Memory Space access in the PCI9030 PCI Command Register (Offset 0x04). To enable PCI I/O Space access to the PCI9030, set bit 0 to '1'. To enable PCI Memory Space access to the PCI9030, set bit 1 to '1'.

Offset in Config.	Description	Usage
0x10	PCI9030 LCR's MEM	Used
0x14	PCI9030 LCR's I/O	Used
0x18	PCI9030 Local Space 0	Used
0x1C	PCI9030 Local Space 1	Not used
0x30	Expansion ROM	Not used

Table 5-2 : PCI9030 PCI Base Address Usage

5.2 Local Configuration Register (LCR)

After reset, the PCI9030 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

The PCI base address for the PCI9030 Local Configuration Registers is PCI9030 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9030 PCI Configuration Register Space) or PCI9030 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9030 PCI Configuration Register Space).

Do not change hardware dependent bit settings in the PCI9030 Local Configuration Registers.

Offset from PCI Base Address	Register	Value	Description
0x00	Local Address Space 0 Range	0x0FFF_FF00	FPGA Address Space
0x04	Local Address Space 1 Range	0x0000_0000	
0x08	Local Address Space 2 Range	0x0000_0000	
0x0C	Local Address Space 3 Range	0x0000_0000	
0x10	Local Exp. ROM Range	0x0000_0000	
0x14	Local Re-map Register Space 0	0x0000_0001	
0x18	Local Re-map Register Space 1	0x0000_0000	
0x1C	Local Re-map Register Space 2	0x0000_0000	
0x20	Local Re-map Register Space 3	0x0000_0000	
0x24	Local Re-map Register ROM	0x0000_0000	
0x28	Local Address Space 0 Descriptor	0x1581_20A0	
0x2C	Local Address Space 1 Descriptor	0x0000_0000	
0x30	Local Address Space 2 Descriptor	0x0000_0000	
0x34	Local Address Space 3 Descriptor	0x0000_0000	
0x38	Local Exp. ROM Descriptor	0x0000_0000	
0x3C	Chip Select 0 Base Address	0x0000_0081	
0x40	Chip Select 1 Base Address	0x0000_0002	
0x44	Chip Select 2 Base Address	0x0000_0002	
0x48	Chip Select 3 Base Address	0x0000_0002	
0x4C	Interrupt Control/Status	0x0041	
0x4E	EEPROM Write Protect Boundary	0x0030	
0x50	Miscellaneous Control Register	0x0078_0000	
0x54	General Purpose I/O Control	0x0024_B6C0	
0x70	Hidden1 Power Management data select	0x0000_0000	
0x74	Hidden 2 Power Management data scale	0x0000_0000	

Table 5-3 : PCI9030 Local Configuration Register

5.3 Configuration EEPROM

After power-on or PCI reset the PCI9030 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x27 : PCI9030 PCI Configuration Register Values
- Address 0x28 to 0x87 : PCI9030 Local Configuration Register Values
- Address 0x88 to 0xFF : Reserved

See the PCI9030 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x02A8	0x1498	0x0280	0x0000	0x1180	0x0000	0x000A	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x0001	0x0000	0x0000
0x20	0x0000	0x0006	0x0000	0x0003	0x0FFF	0xFF00	0x0000	0x0000
0x30	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x50	0x1581	0x20A0	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0081	0x0000	0x0002	0x0000	0x0002
0x70	0x0000	0x0002	0x0030	0x0041	0x0078	0x0000	0x0024	0xB6C0
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 5-4 : Configuration EEPROM

5.4 Local Software Reset

The PCI9030 Local Reset Output LRESETo# is used to reset the on board local logic.

The PCI9030 local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the PCI9030 local configuration register CNTRL (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of 1 resets the PCI9030 and issues a reset to the Local Bus (LRESETo# asserted). The PCI9030 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI9030 PCI and Local Configuration Registers are not reset. The PCI9030 PCI Interface is not reset.

6 Configuration Hints

6.1 Big / Little Endian

- PCI – Bus (Little Endian)

Byte 0	AD[7..0]
Byte 1	AD[15..8]
Byte 2	AD[23..16]
Byte 3	AD[31..24]

- Every Local Address Space (0...3) and the Expansion ROM Space can be programmed to operate in Big or Little Endian Mode.

Big Endian		**Little Endian**	
32 Bit		**32 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
Byte 2	D[15..8]	Byte 2	D[23..16]
Byte 3	D[7..0]	Byte 3	D[31..24]
16 Bit upper lane		**16 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
16 Bit lower lane			
Byte 0	D[15..8]		
Byte 1	D[7..0]		
8 Bit upper lane		**8 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
8 Bit lower lane			
Byte 0	D[7..0]		

Table 6-1 : Local Bus Little/Big Endian

Standard use of the TPMC680 design:

Local Address Space 0	32 bit bus in Big Endian Mode
Local Address Space 1	not used
Local Address Space 2	not used
Local Address Space 3	not used
Expansion ROM Space	not used

To change the Endian Mode use the Local Configuration Registers for the corresponding Space. Bit 24 of the according register sets the mode. A value of 1 indicates Big Endian and a value of 0 indicates Little Endian.

Use the PCI Base Address 0 + Offset or PCI Base Address 1 + Offset:

Short cut	Offset	Name
LAS0BRD	0x28	Local Address Space 0 Bus Region Description Register
LAS1BRD	0x2C	Local Address Space 0 Bus Region Description Register
LAS2BRD	0x30	Local Address Space 0 Bus Region Description Register
LAS3BRD	0x34	Local Address Space 0 Bus Region Description Register
EROMBRD	0x38	Expansion ROM Bus Region Description Register

You could also use the PCI - Base Address 1 I/O Mapped Configuration Registers.

7 Installation

7.1 I/O Circuit

The 64 I/O lines are realized with 8 x 74LV245AT 8 bit bus transceivers, a serial resistor and an array for ESD and overvoltage protection (see figure below “I/O Circuitry”). The maximum output current per line is +/- 16mA. There are no pull-up resistors, therefore unused inputs should be tied to Low or High.

Please note that the length of flat cables connected to the module should be kept very short to prevent large cross talk.

In the figure below only one I/O line is shown. There is one direction signal for each 8 bit port.

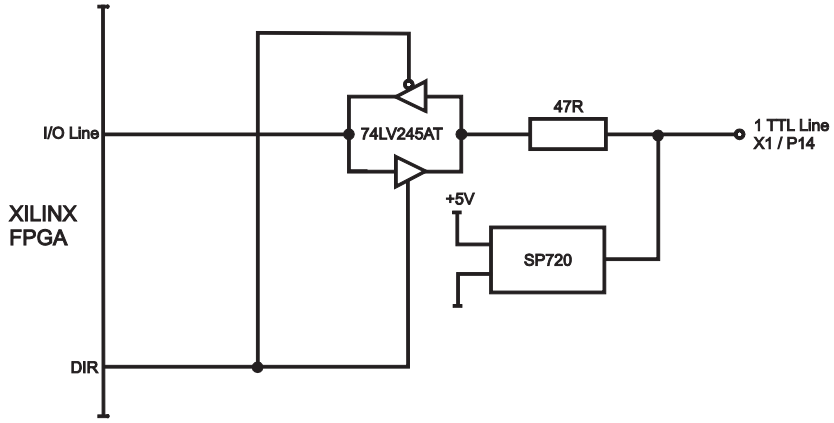

Figure 7-1 : I/O Circuitry

7.2 Back I/O Configuration

The configuration of P14 64 pin Mezzanine “Back I/O” connector lines [57..64] can be changed between ground or port 7 signals by zero ohm resistors.

For removing zero ohm resistors, work on a grounded, static free work surface.

The pads of the zero ohm resistors allow making a direct solder connection between the pads after removing the zero ohm resistors.

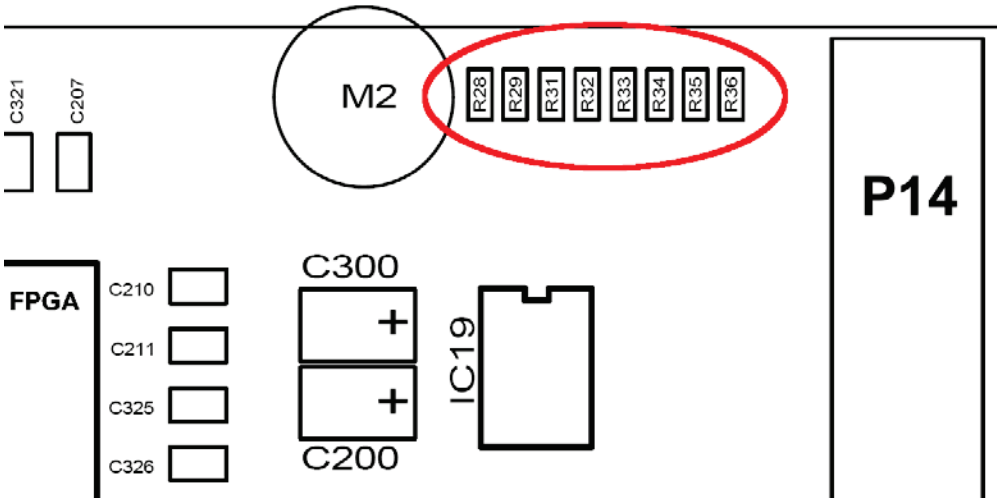

Figure 7-2 : Jumper positions for ground option

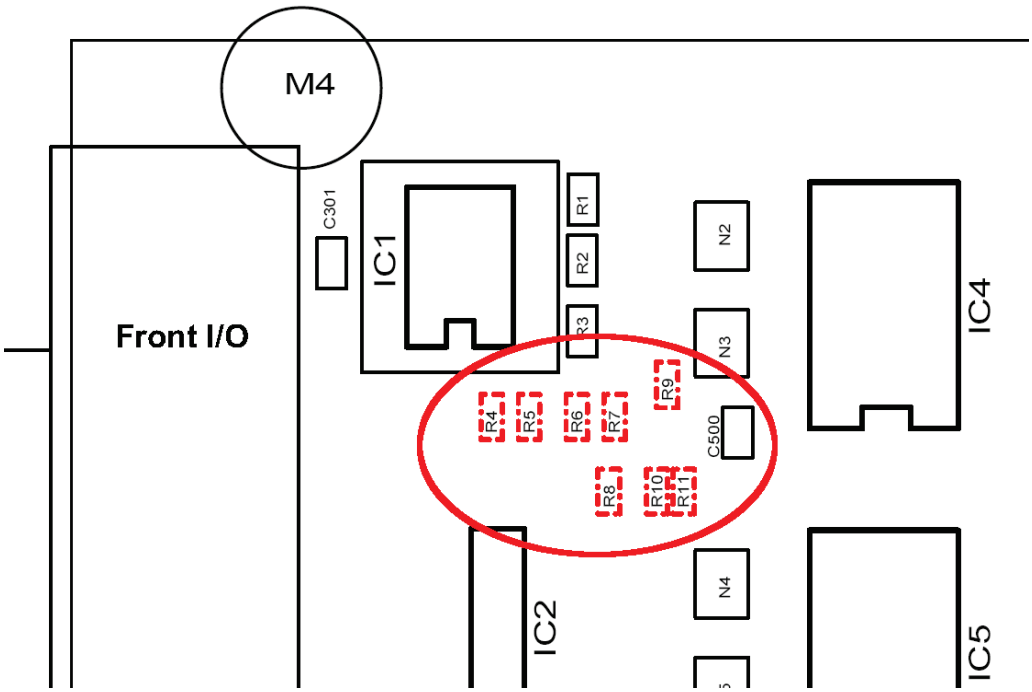

Figure 7-3 : Jumper positions for Port 7 signal option

Back I/O Line	Signal	Jumper Position
57	ground (default)	R33
	Port 7 I/O Line 0	R8
58	ground (default)	R28
	Port 7 I/O Line 1	R9
59	ground (default)	R34
	Port 7 I/O Line 2	R10
60	ground (default)	R29
	Port 7 I/O Line 3	R11
61	ground (default)	R35
	Port 7 I/O Line 4	R7
62	ground (default)	R31
	Port 7 I/O Line 5	R6
63	ground (default)	R36
	Port 7 I/O Line 6	R5
64	ground (default)	R32
	Port 7 I/O Line 7	R4

Table 7-1 : Jumper positions for Back I/O options

Caution: Never make simultaneous connections on both jumper positions of one I/O line. Serious damage of the module is possible.

8 Pin Assignment – I/O Connector

8.1 Back I/O P14

See chapter "Back I/O Configuration".

Pin	Signal	Pin	Signal
1	Port 0, I/O Line 0	33	Port 4 I/O Line 0 (H1)
2	Port 0, I/O Line 1	34	Port 4 I/O Line 1 (H3)
3	Port 0, I/O Line 2	35	Port 4 I/O Line 2
4	Port 0, I/O Line 3	36	Port 4 I/O Line 3
5	Port 0, I/O Line 4	37	Port 4 I/O Line 4
6	Port 0, I/O Line 5	38	Port 4 I/O Line 5
7	Port 0, I/O Line 6	39	Port 4 I/O Line 6
8	Port 0, I/O Line 7	40	Port 4 I/O Line 7
9	Port 1, I/O Line 0	41	Port 5 I/O Line 0 (H2)
10	Port 1, I/O Line 1	42	Port 5 I/O Line 1 (H4)
11	Port 1, I/O Line 2	43	Port 5 I/O Line 2
12	Port 1, I/O Line 3	44	Port 5 I/O Line 3
13	Port 1, I/O Line 4	45	Port 5 I/O Line 4
14	Port 1, I/O Line 5	46	Port 5 I/O Line 5
15	Port 1, I/O Line 6	47	Port 5 I/O Line 6
16	Port 1, I/O Line 7	48	Port 5 I/O Line 7
17	Port 2, I/O Line 0	49	Port 6 I/O Line 0
18	Port 2, I/O Line 1	50	Port 6 I/O Line 1
19	Port 2, I/O Line 2	51	Port 6 I/O Line 2
20	Port 2, I/O Line 3	52	Port 6 I/O Line 3
21	Port 2, I/O Line 4	53	Port 6 I/O Line 4
22	Port 2, I/O Line 5	54	Port 6 I/O Line 5
23	Port 2, I/O Line 6	55	Port 6 I/O Line 6
24	Port 2, I/O Line 7	56	Port 6 I/O Line 7
25	Port 3, I/O Line 0	57	GND / Port 7 I/O Line 0
26	Port 3, I/O Line 1	58	GND / Port 7 I/O Line 1
27	Port 3, I/O Line 2	59	GND / Port 7 I/O Line 2
28	Port 3, I/O Line 3	60	GND / Port 7 I/O Line 3
29	Port 3, I/O Line 4	61	GND / Port 7 I/O Line 4
30	Port 3, I/O Line 5	62	GND / Port 7 I/O Line 5
31	Port 3, I/O Line 6	63	GND / Port 7 I/O Line 6
32	Port 3, I/O Line 7	64	GND / Port 7 I/O Line 7

Table 8-1 : P14 I/O Pin Assignment

Be sure that the P14 connector I/O signals are available and not otherwise used on the J14 connector of the PMC carrier board.

8.2 Front Panel I/O

All I/O ports 0:7 are available on the HD68 front panel connector.

Pin	Signal	Pin	Signal
1	Port 0, I/O Line 0	35	Port 4 I/O Line 2
2	Port 0, I/O Line 1	36	Port 4 I/O Line 3
3	Port 0, I/O Line 2	37	Port 4 I/O Line 4
4	Port 0, I/O Line 3	38	Port 4 I/O Line 5
5	Port 0, I/O Line 4	39	Port 4 I/O Line 6
6	Port 0, I/O Line 5	40	Port 4 I/O Line 7
7	Port 0, I/O Line 6	41	Port 5 I/O Line 0 (H2)
8	Port 0, I/O Line 7	42	Port 5 I/O Line 1 (H4)
9	Port 1, I/O Line 0	43	Port 5 I/O Line 2
10	Port 1, I/O Line 1	44	Port 5 I/O Line 3
11	Port 1, I/O Line 2	45	Port 5 I/O Line 4
12	Port 1, I/O Line 3	46	Port 5 I/O Line 5
13	Port 1, I/O Line 4	47	Port 5 I/O Line 6
14	Port 1, I/O Line 5	48	Port 5 I/O Line 7
15	Port 1, I/O Line 6	49	Port 6 I/O Line 0
16	Port 1, I/O Line 7	50	Port 6 I/O Line 1
17	Port 2, I/O Line 0	51	Port 6 I/O Line 2
18	Port 2, I/O Line 1	52	Port 6 I/O Line 3
19	Port 2, I/O Line 2	53	Port 6 I/O Line 4
20	Port 2, I/O Line 3	54	Port 6 I/O Line 5
21	Port 2, I/O Line 4	55	Port 6 I/O Line 6
22	Port 2, I/O Line 5	56	Port 6 I/O Line 7
23	Port 2, I/O Line 6	57	Port 7 I/O Line 0
24	Port 2, I/O Line 7	58	Port 7 I/O Line 1
25	Port 3, I/O Line 0	59	Port 7 I/O Line 2
26	Port 3, I/O Line 1	60	Port 7 I/O Line 3
27	Port 3, I/O Line 2	61	Port 7 I/O Line 4
28	Port 3, I/O Line 3	62	Port 7 I/O Line 5
29	Port 3, I/O Line 4	63	Port 7 I/O Line 6
30	Port 3, I/O Line 5	64	Port 7 I/O Line 7
31	Port 3, I/O Line 6	65	GND
32	Port 3, I/O Line 7	66	GND
33	Port 4 I/O Line 0 (H1)	67	GND
34	Port 4 I/O Line 1 (H3)	68	GND

Table 8-2 : Front I/O Pin Assignment