The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC685

16 x 8 Bit Digital Inputs/Outputs (5V TTL)

Version 1.0

User Manual

Issue 1.0.1

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TPMC685-10

16 x 8 Bit Digital Inputs/Outputs (5V TTL)

TPMC685-11

15 x 8 Bit Digital Inputs/Outputs (5V TTL) plus 8 Ground

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial Issue	September 2012
1.0.1	○ Input and output voltage levels added in chapter “Technical Specification” ○ Added Chapter 5.3 “On-board LEDs” ○ Added information about the filter time accuracy to chapter 4.4 “Input filter Registers” and chapter 6.8 “Input Filter”. ○ Added notes about the fact that Port [15] is not available on the TPMC685-11 throughout the document. ○ Added notes about the usage of the PCI-Clock as time base for all internal timers in chapter 6 “Functional Description” ○ Added notes about input filter delay in chapter 6.9 “Port Data Register” ○ Clearing mechanism for the “Simultaneous I/O Register” corrected to self-clearing. ○ Clarification about timer reactivation added to chapters 4.2.1 and chapter 6.6 ○ Description of TIMEBASE = 0x00 and 0x11 added in chapter 4.2 and chapter 4.3 ○ Added Notes throughout the document about status register read while “Ack on Read” is used ○ PCI Class Code corrected	April 2018

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1 Product Description

The TPMC685 is a standard single-width 32 bit PMC module offering up to 128 bit of TTL I/O arranged in 16 x 8 bit ports. Direction of the I/O lines is software programmable for each of the ports. Each port is built up using a TTL bus transceiver. Each line is protected against ESD and overvoltage.

Software selectable Pullup / Pulldown Resistors are available on all I/O lines.

Each input can generate an interrupt. Signal edge handling is programmable to interrupt on rising and/or falling edge of the input signal. Interrupts can be enabled and disabled for each bit. For interrupt source detection the status of each bit can be read from the interrupt status register.

To eliminate spikes and glitches, keeping interrupts to a minimum, each port has its own user configurable input filter.

All outputs drive 5V TTL levels with up to 24mA.

It is possible to read or write synchronously all 128 lines.

The first 64 bits of TTL I/O are accessible via the front panel HD68 SCSI-3 type connector and the second 64 bits of TTL I/O via rear panel P14.

To deal with system faults, the TPMC685 provides a user configurable Watchdog timer. It can set all outputs in a user defined (save) state when the watchdog expires.

Two Timers are included in the TPMC685 for easy implementation of equidistant input sampling or output setting.

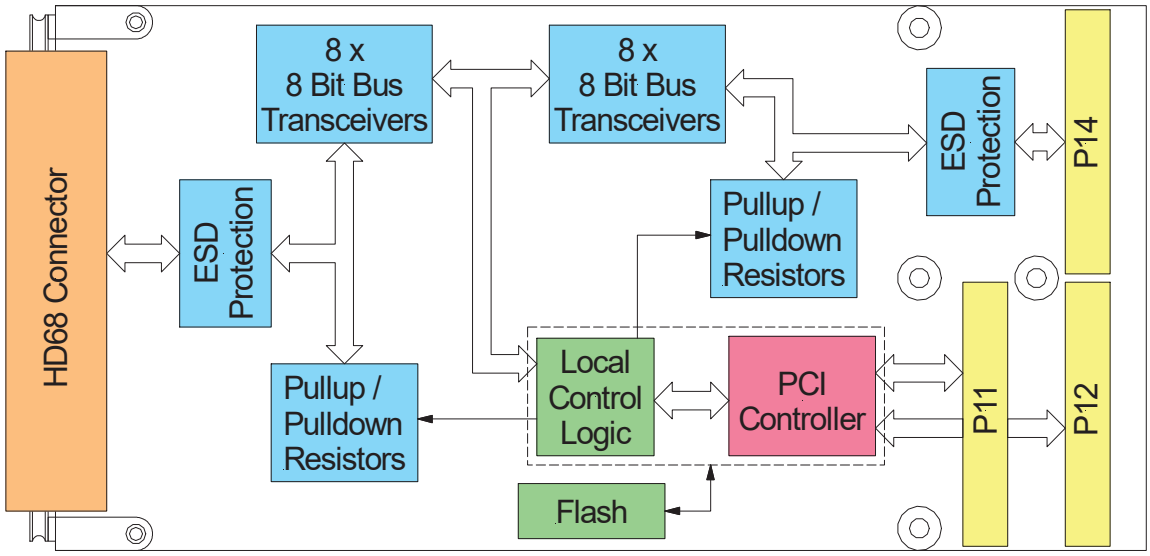

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface confirming to IEEE P1386/P1386.1 Single Size	
Electrical Interface	PCI Rev. 3.0 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage tolerant	
On Board Devices		
PCI Target Chip	Xilinx Spartan-6 with PCI Core	
I/O Interface		
Number of I/Os	TPMC685-10: 128 (64 Front, 64 Rear) TPMC685-11: 120 (64 Front, 56 Rear) + 8 Rear-GND	
I/O Voltage	TTL signaling: Min. high input voltage: 2.0V Max. low input voltage: 0.8V Min. high output voltage @ 24mA: 3.76V Max. low output voltage @ 24mA: 0.44V	
Output Current	maximum current: +/-24mA per I/O	
Input Debounce time	120ns to 65536ms	
Input Interrupts	Rising, falling or both edges for each I/O	
I/O Protection	ESD and Over-Voltage Protection	
I/O Connector	Front I/O HD68 / SCSI-3 (AMP 5-787082-7 or compatible) PMC P14 I/O (64 pin Mezzanine Connector)	
Physical Data		
Power Requirements	230mA typical @ +5V DC (all IOs input, outputs need additional power depending on number and load)	
Temperature Range	Operating Storage	-40 °C to +85 °C -40 °C to +85 °C
MTBF	617000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	75 g	

Table 2-1 : Technical Specification

3 Address Map

3.1 PCI Configuration Space

PCI CFG Register Address	Write '0' to all unused (Reserved) bits								Initial Values (Hex Values)
	31	24	23	16	15	8	7	0	
0x00	Device ID 0x02AD (TPMC685)				Vendor ID 0x1498 (TEWS Technologies)				02AD 1498
0x04	Status				Command				0280 0000
0x08	Class Code						Revision ID		000000 00
0x0C	not supported		Header Type		PCI Latency Timer		not supported		00 00 00 00
0x10	Base Address Register 0 (BAR0)								FFFFFF00
0x14	not supported								00000000
0x18	not supported								00000000
0x1C	not supported								00000000
0x20	not supported								00000000
0x24	not supported								00000000
0x28	PCI CardBus Information Structure Pointer								00000000
0x2C	Subsystem ID **s.b.**				Subsystem Vendor ID 0x1498 (TEWS Technologies)				**s.b.** 1498
0x30	not supported								00000000
0x34	Reserved						New Cap. Ptr.		000000 00
0x38	Reserved								00000000
0x3C	Max_Lat		Min_Gnt		Interrupt Pin		Interrupt Line		00 00 01 00
0x40-0xFF	Reserved								00000000

Table 3-1 : PCI Configuration Space Header

Subsystem-ID: TPMC685-10 = 0x000A

TPMC685-11 = 0x000B

3.1.1 Base Address Register Configuration

Base Address Register (BAR)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	MEM	256	32	Little	Register Space

Table 3-2 : Base Address Register Configuration

3.2 Register Space

The Register Space is accessible via the PCI Base Address Register 0 (BAR0). All local Registers of the TPMC685 are located in this space.

Offset (BAR 0)	Description	Size (Bit)
General Registers		
0x00	Global Control Register (GCR)	32
0x04	Global Interrupt Status Register (GISR)	32
0x08	Port Data Direction Register (PDDR)	32
0x0C	Pullup / Pulldown Register (PPR)	32
0x10	Simultaneous I/O Register (SIOR)	32
0x14 ... 0x1F	Reserved	-
Timer Registers		
0x20	Timer Control Register 0	32
0x24	Timer Control Register 1	32
0x28	Timer Status Register 0	32
0x2C	Timer Status Register 1	32
Watchdog Registers		
0x30	Watchdog Control Register (WDCR)	32
0x34	Watchdog Status Register (WDSR)	32
0x38	Watchdog Port Data Register 0 (WDPDR0)	8
...	...	...
0x47	Watchdog Port Data Register 15 (WDPDR15)	8
0x48 ... 0x4F	Reserved	-
Input Filter Registers		
0x50	Input Filter Register 0 (IFR0)	32
...	...	...
0x8C	Input Filter Register 15 (IFR15)	32
Interrupt Enable Registers		
0x90	Rising Edge Interrupt Enable Register 0 (RIER0)	8
...	...	...
0x9F	Rising Edge Interrupt Enable Register 15 (RIER15)	8
0xA0	Falling Edge Interrupt Enable Register 0 (FIER0)	8
...	...	...
0xAF	Falling Edge Interrupt Enable Register 15 (FIER15)	8

Interrupt Status Registers		
0xB0	Rising Edge Interrupt Status Register 0 (RISR0)	8
...	...	...
0xBF	Rising Edge Interrupt Status Register 15 (RISR15)	8
0xC0	Falling Edge Interrupt Status Register 0 (FISR0)	8
...	...	...
0xCF	Falling Edge Interrupt Status Register 15 (FISR15)	8
Port Data Registers		
0xD0	Port Data Register 0 (PDR0)	8
...	...	...
0xDF	Port Data Register 15 (PDR15)	8
Reserved		
0xE0 … 0xFF	Reserved	-

Table 3-3 : Register Space Address Map

4 Register Description

4.1 General Registers

4.1.1 Global Control Register

Bit	Symbol	Description	Access	Reset Value
31:16	CODE_VER	FPGA-Code Version	R	*)
15:10	-	Reserved (0 for reads)	R	0
9	IACK_MODE	0 : Interrupts are acknowledged by writing a “1” to the corresponding bit of the Interrupt Status Register 1 : Interrupts are acknowledged by reading the corresponding Interrupt Status Register.	R/W	0
8	GLOB_INT_EN	Global Interrupt Enable 0 : Interrupts disabled 1 : Interrupts enabled	R/W	0
7:6	-	Reserved (0 for reads)	R	0
5	64BIT_OUT_EN_1	64 bit Simultaneous Output Mode Enable for Port[15:8] 0 : disabled 1 : enabled	R/W	0
4	64BIT_OUT_EN_0	64 bit Simultaneous Output Mode Enable for Port[7:0] 0 : disabled 1 : enabled	R/W	0
3:2	-	Reserved (0 for reads)	R	0
1	64BIT_IN_EN_1	64 bit Simultaneous Input Mode Enable for Port[15:8] 0 : disabled 1 : enabled	R/W	0
0	64BIT_IN_EN_0	64 bit Simultaneous Input Mode Enable for Port[7:0] 0 : disabled 1 : enabled	R/W	0

Table 4-1 : Global Control Register

*) depends on FPGA-Code Version

When Interrupt acknowledge mode “Ack on Read” is used, any Interrupt Status Register should not be read outside the ISR (Interrupt Service Routine) context as such a read access could clear a previously asserted interrupt before the ISR has finished the interrupt handling. This could lead to a spurious interrupt because the ISR could not find the source for the interrupt, or the interrupt is removed before the ISR is started by the system.

4.1.2 Global Interrupt Status Register

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved	R	0
10	INT_TIMER_1	Timer 1 Interrupt Status 0 : no active Interrupt Request 1 : active Interrupt Request	R	0
9	INT_TIMER_0	Timer 0 Interrupt Status 0 : no active Interrupt Request 1 : active Interrupt Request	R	0
8	INT_WATCHDOG	Watchdog Interrupt Status 0 : no active Interrupt Request 1 : active Interrupt Request	R	0
7	INT_RISR[15:12]	Rising Edge Interrupt Status 0 : no active Interrupt Request 1 : active Interrupt Request in the corresponding interrupt status registers	R	0
6	INT_RISR[11:8]			
5	INT_RISR[7:4]			
4	INT_RISR[3:0]			
3	INT_FISR[15:12]	Falling Edge Interrupt Status 0 : no active Interrupt Request 1 : active Interrupt Request in the corresponding interrupt status registers	R	0
2	INT_FISR[11:8]			
1	INT_FISR[7:4]			
0	INT_FISR[3:0]			

Table 4-2 : Global Interrupt Status Register

4.1.3 Port Data Direction Register

All 8 lines of one port have the same direction. This register sets the port direction as input or output.

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved (0 for reads)	-	0
15	DIR_PORT15 *)	Port 0-15 Data Direction 0 : Port is Input 1 : Port is Output	R/W	0
14	DIR_PORT14			
13	DIR_PORT13			
12	DIR_PORT12			
11	DIR_PORT11			
10	DIR_PORT10			
9	DIR_PORT9			
8	DIR_PORT8			
7	DIR_PORT7			
6	DIR_PORT6			
5	DIR_PORT5			
4	DIR_PORT4			
3	DIR_PORT3			
2	DIR_PORT2			
1	DIR_PORT1			
0	DIR_PORT0			

Table 4-3 : Port Data Direction Register

*) On TPMC685-11, this bit will be don't care since this port is physically not connected to a connector. The pins of this port are instead used as P14 ground pins on the TPMC685-11.

4.1.4 Pullup / Pulldown Register

Bit	Symbol	Description	Access	Reset Value
31:30	PULL_PORT15 *)	Port [15:0] Pullup / Pulldown selection 00 : Pulldown 01 : Pullup to 5V 10 : Pullup to 3.3V 11 : No Pullup or Pulldown	R/W	0
29:28	PULL_PORT14			
27:26	PULL_PORT13			
25:24	PULL_PORT12			
23:22	PULL_PORT11			
21:20	PULL_PORT10			
19:18	PULL_PORT9			
17:16	PULL_PORT8			
15:14	PULL_PORT7			
13:12	PULL_PORT6			
11:10	PULL_PORT5			
9:8	PULL_PORT4			
7:6	PULL_PORT3			
5:4	PULL_PORT2			
3:2	PULL_PORT1			
1:0	PULL_PORT0			

Table 4-4 : Pullup / Pulldown Register

*) On TPMC685-11, this bit will be don't care since this port is physically not connected to a connector. The pins of this port are instead used as P14 ground pins on the TPMC685-11.

4.1.5 Simultaneous I/O Register

Bit	Symbol	Description	Access	Reset Value
31:10	-	Reserved (0 for reads)	R	0
9	64BIT_DRIVE_1	Drive Output values on Port [15:8] Writing a '1' updates all Output Ports simultaneously. This bit is self-clearing.	R/W	0
8	64BIT_DRIVE_0	Drive Output values on Port [7:0] Writing a '1' updates all Output Ports simultaneously. This bit is self-clearing.	R/W	0
7:2	-	Reserved (0 for reads)	R	0
1	64BIT_SAMPLE_1	Sample Inputs of Port [15:8] Writing a '1' samples all Input Ports. Data in the corresponding Port Data registers will not change until this bit is rewritten. This bit is self-clearing.	R/W	0
0	64BIT_SAMPLE_0	Sample Inputs of Port [7:0] Writing a '1' samples all Input Ports. Data in the corresponding Port Data registers will not change until this bit is rewritten. This bit is self-clearing.	R/W	0

Table 4-5 : Simultaneous I/O Register

As all bits in this register are self-clearing, software will always read this register as 0x00000000.

4.2 Timer Registers

4.2.1 Timer Control Register [1:0]

Bit	Symbol	Description	Access	Reset Value
31:29	-	Reserved (0 for reads)	R	0
28	TIMER_EN_x	0 = Disable Timer x 1 = Enable Timer x	R/W	0
27:26	-	Reserved (0 for reads)	R	0
25	TIMER_MODE_x	0 = single cycle mode 1 = continuous mode	R/W	0
24	TIMER_INT_EN_x	0 = Disable Interrupt when the Timer expires 1 = Enable Interrupt when the Timer expires	R/W	0
23:18	-	Reserved (0 for reads)	R	0
17:16	TIMEBASE_x	00 = use 100ns Time base 01 = use 1µs Time base 10 = use 1ms Time base others = reserved *)	R/W	0
15:0	TIME_x	These bits set the starting value for the timer. The timer runs with the time base set by TIMEBASE.	R/W	0

Table 4-6 : Timer Control Register

*) The time base will actually be 60ns if this setting is used.

To restart the timer when using the single cycle mode, the timer must first be disabled before it can be restarted by enabling the timer again.

4.2.2 Timer Status Register [1:0]

Bit	Symbol	Description	Access	Reset Value
31:30	-	Reserved (0 for reads)	R	0
29	TIMER_EXPIRED_x	0 = Timer has not expired 1 = Timer has expired	R/C *	0
28	TIMER_RUN_STAT_x	0 = Timer is stopped 1 = Timer is running	R	0
27:26	-	Reserved (0 for reads)	R	0
25	TIMER_MODE_STAT_x	0 = single cycle mode 1 = continuous mode	R	0
24	TIMER_INT_EN_STAT_x	Timer Interrupt Enable Status 0 = Timer interrupt is disabled 1 = Timer interrupt is enabled	R	0
23:18	-	Reserved (0 for reads)	R	0
17:16	TIMEBASE _STAT_x	00 = use 100ns Time base 01 = use 1µs Time base 10 = use 1ms Time base others = reserved *)	R	0
15:0	TIME_STAT_x	These bits show the remaining value of the timer. The timer runs with the time base shown by TIMEBASE_STAT_x.	R	0

Table 4-7 : Timer Status Register

* the way this status bit is cleared depends on the IACK_MODE selected in the GCR.

*) The time base will actually be 60ns if this setting is used.

While Interrupt acknowledge mode “Ack on Read” is used, the Timer Status Register should not be read outside the ISR (Interrupt Service Routine) context as such a read access could clear a previously asserted interrupt before the ISR has finished the interrupt handling. This could lead to a spurious interrupt because the ISR could not find the source for the interrupt, or the interrupt is removed before the ISR is started by the system.

4.3 Watchdog Registers

4.3.1 Watchdog Control Register

The “Watchdog Control Register” allows to enable / disable the Watchdog and to set the watchdog time interval.

An expired Watchdog timer can generate an interrupt.

Bit	Symbol	Description	Access	Reset Value
31:29	-	Reserved (0 for reads)	R	0
28	WD_EN	0 = Disable Watchdog 1 = Enable Watchdog	R/W	0
27:26	-	Reserved (0 for reads)	R	0
25	WD_SAVE_EN	0 = do not use Save output settings from the WDPDRs if Watchdog expires. 1 = use Save output settings from the WDPDRs if Watchdog expires.	R/W	0
24	WD_INT_EN	0 = Disable Interrupt Generation when the Watchdog expires 1 = Enable Interrupt Generation when the Watchdog expires	R/W	0
23:18	-	Reserved (0 for reads)	R	0
17:16	WD_TIMEBASE	00 = use 100ns Time base 01 = use 1µs Time base 10 = use 1ms Time base 11 = reserved *)	R/W	0
15:0	WD_TIME	These bits set the starting value for the timer. The timer runs with the time base set by WD_TIMEBASE.	R/W	0

Table 4-8 : Watchdog Control Register

*) The Watchdog time base will actually be 60ns if this setting is used.

4.3.2 Watchdog Status Register

Reading the “Watchdog Status Register” is used to detect the watchdog status (watchdog enabled / disabled / timer expired). Any access to this register retriggers the watchdog timer.

Bit	Symbol	Description	Access	Reset Value
31:29	-	Reserved (0 for reads)	R	0
28	WD_EN_STATUS	0 = Watchdog is disabled 1 = Watchdog is enabled	R	0
27:26	-	Reserved (0 for reads)	R	0
25	WD_SAVE_STATUS	0 = Save output settings from the WDPDRs are not used if Watchdog expires. 1 = Save output settings from the WDPDRs are used if Watchdog expires.	R	0
24	WD_INT_STATUS	0 = no active Watchdog interrupt 1 = active Interrupt because the Watchdog expired	R/C *	0
23:21	-	Reserved (0 for reads)	R	0
20	WD_EXP_STATUS	0 = Watchdog did not expire 1 = Watchdog has expired	R	0
19:18	-	Reserved (0 for reads)	R	0
17:16	WD_TIMEBASE _STATUS	00 = use 100ns Time base 01 = use 1µs Time base 10 = use 1ms Time base 11 = reserved *)	R	0
15:0	WD_TIME_STATUS	These bits show the remaining value of the Watchdog timer. The timer runs with the time base shown by WD_TIMEBASE_STATUS.	R	0

Table 4-9 : Watchdog Status Register

* the way this status bit is cleared depends on the IACK_MODE selected in the GCR.

*) The Watchdog time base will actually be 60ns if this setting is used.

While Interrupt acknowledge mode “Ack on Read” is used, the Watchdog Status Register should not be read outside the ISR (Interrupt Service Routine) context as such a read access could clear a previously asserted interrupt before the ISR has finished the interrupt handling. This could lead to a spurious interrupt because the ISR could not find the source for the interrupt, or the interrupt is removed before the ISR is started by the system. It is recommended to use write accesses to the Watchdog Status register for watchdog retriggering in this case.

4.3.3 Watchdog Port Data Register [15:0]

The Watchdog Port Data Registers are used to define the “secure” output settings, which will get active in the case the watchdog expires and WD_SAVE_EN in the Watchdog Control Register is set.

The “Watchdog Port Data Registers” are preloaded with 0x00 at power-up. This means all outputs will drive a logic low level when the watchdog expires and WD_SAVE_EN is set. Software can overwrite the “Watchdog Port Data Registers”.

Bit	Symbol	Description	Access	Reset Value
7	PORTx_WD_BIT7	Output data settings for Port x Data Bit 7:0 that are used if the Watchdog timer expires.	R/W	0
6	PORTx_WD_BIT6		R/W	0
5	PORTx_WD_BIT5		R/W	0
4	PORTx_WD_BIT4		R/W	0
3	PORTx_WD_BIT3		R/W	0
2	PORTx_WD_BIT2		R/W	0
1	PORTx_WD_BIT1		R/W	0
0	PORTx_WD_BIT0		R/W	0

Table 4-10 : Watchdog Port Data Registers

On TPMC685-11, the Watchdog Port Data Register [15] will be don’t care since this port is physically not connected to a connector. The pins of this port are instead used as P14 ground pins on the TPMC685-11.

4.4 Input Filter Registers

Each I/O Port has its own input filter. This filter removes glitches and spikes, which can dramatically reduce the interrupt load. To use the input filter, it must be enabled and programmed with valid values for Timebase and Filter-Timer.

4.4.1 Input Filter Register [15:0]

Bit	Symbol	Description	Access	Reset Value
31:25	-	Reserved (0 for reads)	R	0
24	FILTER_EN_x	0 = Disable Input Filter 1 = Enable Input Filter	R/W	0
23:18	-	Reserved (0 for reads)	R	0
17:16	FILTER_TIMEBASE_x	Time base used for the Input Filter 00 = use 1ns Time base* 01 = use 1µs Time base 10 = use 1ms Time base 11 = reserved	R/W	0
15:0	FILTER_TIMER_x	These bits set the Filter time together with the time base set by FILTER_TIMEBASE_x.	R/W	0

Table 4-11 : Input Filter Registers

* For FILTER_TIMEBASE_x = 0x0 (timebase 1ns), the lowest 7 bit of FILTER_TIMER_x have no effect. The effective minimum filter-time resolution is 120ns.

The actual filter time will be in the range of the selected filter time ±25%.

On TPMC685-11, the Input Filter Register [15] will be don't care since this port is physically not connected to a connector. The pins of this port are instead used as P14 ground pins on the TPMC685-11.

4.5 Interrupt Registers

4.5.1 Rising Edge Interrupt Enable Register [15:0]

Bit	Symbol	Description	Access	Reset Value
7	PORTx_RIE7	Port x Line 7:0 Rising Edge Interrupt Enable 0 = disabled 1 = enabled (Individual Interrupt Enable for each Line)	R/W	0
6	PORTx_RIE6		R/W	0
5	PORTx_RIE5		R/W	0
4	PORTx_RIE4		R/W	0
3	PORTx_RIE3		R/W	0
2	PORTx_RIE2		R/W	0
1	PORTx_RIE1		R/W	0
0	PORTx_RIE0		R/W	0

Table 4-12 : Rising Edge Interrupt Enable Registers

On TPMC685-11, the Rising Edge Interrupt Enable Register [15] will be don't care since this port is physically not connected to a connector. The pins of this port are instead used as P14 ground pins on the TPMC685-11.

4.5.2 Falling Edge Interrupt Enable Register [15:0]

Bit	Symbol	Description	Access	Reset Value
7	PORTx_FIE7	Port x Line 7:0 Falling Edge Interrupt Enable 0 = disabled 1 = enabled (Individual Interrupt Enable for each Line)	R/W	0
6	PORTx_FIE6		R/W	0
5	PORTx_FIE5		R/W	0
4	PORTx_FIE4		R/W	0
3	PORTx_FIE3		R/W	0
2	PORTx_FIE2		R/W	0
1	PORTx_FIE1		R/W	0
0	PORTx_FIE0		R/W	0

Table 4-13 : Falling edge Interrupt Enable Register

On TPMC685-11, the Falling Edge Interrupt Enable Register [15] will be don't care since this port is physically not connected to a connector. The pins of this port are instead used as P14 ground pins on the TPMC685-11.

4.5.3 Rising Edge Interrupt Status Register [15:0]

These registers signal the lines on which an falling edge interrupt event occurred.

Bit	Symbol	Description	Access	Reset Value
7	PORTx_RIS7	Port x Line 7:0 Rising Edge Interrupt Request Status 0 = no active interrupt request 1 = active interrupt request	R/C*	0
6	PORTx_RIS6		R/C*	0
5	PORTx_RIS5		R/C*	0
4	PORTx_RIS4		R/C*	0
3	PORTx_RIS3		R/C*	0
2	PORTx_RIS2		R/C*	0
1	PORTx_RIS1		R/C*	0
0	PORTx_RIS0		R/C*	0

Table 4-14 : Rising Edge Interrupt Status Register

* the way this status bit is cleared depends on the IACK_MODE selected in the GCR.

On TPMC685-11, the Rising Edge Interrupt Status Register [15] will be don't care since this port is physically not connected to a connector. The pins of this port are instead used as P14 ground pins on the TPMC685-11.

While Interrupt acknowledge mode "Ack on Read" is used, the Rising Edge Interrupt Status Registers should not be read outside the ISR (Interrupt Service Routine) context as such a read access could clear a previously asserted interrupt before the ISR has finished the interrupt handling. This could lead to a spurious interrupt because the ISR could not find the source for the interrupt, or the interrupt is removed before the ISR is started by the system.

4.5.4 Falling Edge Interrupt Status Register [15:0]

These registers signal the lines on which an falling edge interrupt event occurred.

Bit	Symbol	Description	Access	Reset Value
7	PORTx_FIS7	Port x Line 7:0 Falling Edge Interrupt Request Status 0 = no active interrupt request 1 = active interrupt request	R/C*	0
6	PORTx_FIS6		R/C*	0
5	PORTx_FIS5		R/C*	0
4	PORTx_FIS4		R/C*	0
3	PORTx_FIS3		R/C*	0
2	PORTx_FIS2		R/C*	0
1	PORTx_FIS1		R/C*	0
0	PORTx_FIS0		R/C*	0

Table 4-15 : Falling Edge Interrupt Status Register

* the way this status bit is cleared depends on the IACK_MODE selected in the GCR.

On TPMC685-11, the Falling Edge Interrupt Status Register [15] will be don't care since this port is physically not connected to a connector. The pins of this port are instead used as P14 ground pins on the TPMC685-11.

While Interrupt acknowledge mode "Ack on Read" is used, the Falling Edge Interrupt Status Registers should not be read outside the ISR (Interrupt Service Routine) context as such a read access could clear a previously asserted interrupt before the ISR has finished the interrupt handling. This could lead to a spurious interrupt because the ISR could not find the source for the interrupt, or the interrupt is removed before the ISR is started by the system.

4.6 Port Data Registers

A Read to the Port Data Registers displays the input values for ports configured as Input. If the Port is configured as Output, reading the Port Data Register returns the output values written to this register.

Simultaneous Update Modes are available for the Front I/Os, the Rear I/Os or all I/Os. It can be used for inputs and outputs independently.

To use the Simultaneous Mode, it must be enabled in the Global Control Register.

In Simultaneous Input Mode, a write to the “64BIT_SAMPLE_x” Bit in the “Simultaneous I/O Register” Register latches all corresponding inputs. Any read to the port data registers of these inputs now returns the input data sampled at the time the latch was enabled. With the next write to the “64BIT_SAMPLE_x” Bit, new input data is latched.

In Simultaneous Output Mode, any write to the port data registers of the affected outputs is buffered until the corresponding “64BIT_DRIVE_x” Bit in the “Simultaneous I/O Register” is written. With the write to this Bit, all the Outputs are updated, thus achieving up to 128 simultaneous outputs.

4.6.1 Port Data Register [15:0]

Bit	Symbol	Description	Access	Reset Value
7	PORTx_BIT7	Port x Data Bit 7:0	R/W	+)
6	PORTx_BIT6		R/W	+)
5	PORTx_BIT5		R/W	+)
4	PORTx_BIT4		R/W	+)
3	PORTx_BIT3		R/W	+)
2	PORTx_BIT2		R/W	+)
1	PORTx_BIT1		R/W	+)
0	PORTx_BIT0		R/W	+)

Table 4-16 : Port Data Register [15:0]

+) depends on Port direction

On TPMC685-11, the Port Data Register [15] will be don’t care since this port is physically not connected to a connector. The pins of this port are instead used as P14 ground pins on the TPMC685-11.

5 Configuration Hints

5.1 Jumper / Switches

The TPMC685 has no Jumpers or mechanical Switches

5.2 Big / Little Endian

As a PCI Target Device, all TPMC685 internal registers are little endian.

- PCI – Bus (Little Endian)

Byte 0	AD[7..0]
Byte 1	AD[15..8]
Byte 2	AD[23..16]
Byte 3	AD[31..24]

5.3 On-board LEDs

The TPMC685 provides the following three on-board LEDs for status indication and diagnostic:

Description	Color	PCB Text
FPGA Configuration Done	Green	DONE
Watchdog LED	Red	WD
Power Good	Green	PG

Table 5-1 : On-board LEDs

The LEDs are located near the front bezel as shown in the following figure.

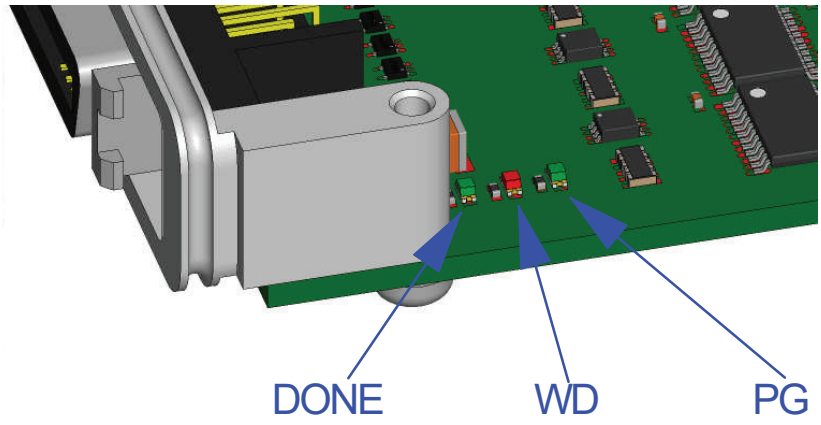

Figure 5-1 : On-board LED locations

6 Functional Description

6.1 Interrupt Acknowledge Mode

The TPMC685 supports two different Interrupt acknowledge modes: “Ack on Write” (default) and “Ack on Read”.

When “Ack on Write” is used, pending interrupts are acknowledged by writing a ‘1’ to the corresponding status register bit. In the case of multiple pending interrupts across the 128 I/Os of the TPMC685, this may need up to 18 PCI accesses to acknowledge all pending interrupts.

To reduce the amount of PCI accesses necessary to acknowledge pending interrupts, the TPMC685 can be switched to “Ack on Read” by setting the IACK_MODE bit in the Global Control Register. When “Ack on Read” is used, pending interrupts are acknowledged by reading the corresponding status register. In the case of multiple pending interrupts across all 128 I/Os of the TPMC685, this can half the PCI accesses necessary to acknowledge all pending interrupts.

When Interrupt acknowledge mode “Ack on Read” is used, any Interrupt Status Register should not be read outside the ISR (Interrupt Service Routine) context as such a read access could clear a previously asserted interrupt before the ISR has finished the interrupt handling. This could lead to a spurious interrupt because the ISR could not find the source for the interrupt, or the interrupt is removed before the ISR is started by the system.

6.2 Port Direction

Each port can be set to input or output by the Port Data Direction Register. It takes up to 300µs from the write to the Port Data Direction Register until the port direction is changed. After power-up or reset, all ports are configured as input.

6.3 Pullup / Pulldown

Each I/O Line is connected to a Pull-Resistor. All 8 Pull-Resistors of a port are connected to a common “Pull-Voltage” that can be connected to GND, 3.3V, 5V or left floating. This results in 3.3V Pullup, 5V Pullup or Pulldown resistors for each port. If the Pull-Resistors float, the user should keep in mind that the 8 I/O Lines of the port are connected via their Pull-Resistors. See also Figure below.

Pull-Resistor configuration is done by Software via the Pullup / Pulldown Register.

By default, all Ports have pulldown resistors.

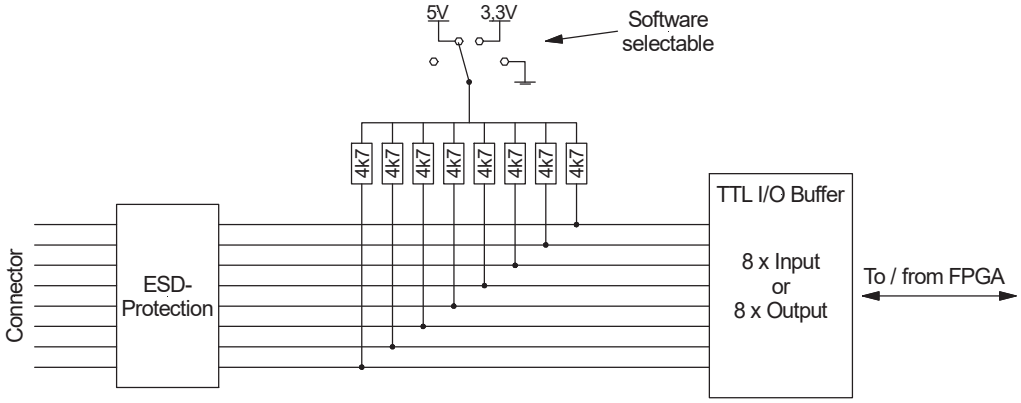

Figure 6-1 : Pullup / Pulldown Block Diagram

6.4 Simultaneous Input Sampling

Reading the Port Data Registers allows sampling up to 4 Input Ports simultaneously when using aligned 16 bit or 32 bit PCI accesses. If more input ports shall be sampled simultaneously, this can be achieved by using the simultaneous I/O feature of the TPMC685. First, the Simultaneous Input Sampling feature must be enabled by setting the corresponding 64BIT_IN_EN_x bit in the Global Control Register. Now, every time the 64BIT_SAMPLE_x bit in the Simultaneous I/O Register is set, the Input ports selected by 64BIT_IN_EN_x are latched simultaneously, and can be read using multiple PCI accesses.

If Ports in the range of an active 64BIT_IN_EN_x are set to output, readback of the output value is also delayed until the corresponding 64BIT_SAMPLE_x is set the next time.

6.5 Simultaneous Outputs

Writing the Port Data Registers allows setting up to 4 Output Ports simultaneously when using aligned 16 bit or 32 bit PCI access. If more output ports shall be set simultaneously, this can be achieved by using the simultaneous I/O feature of the TPMC685:

1) Enable the Simultaneous Drive Outputs feature by setting the corresponding 64BIT_OUT_EN_x bit in the Global Control Register.

2) All writes to the corresponding output registers are now buffered without updating the outputs.

3) Setting the 64BIT_DRIVE_x bit in the Simultaneous I/O Register updates all corresponding outputs with the previously written values.

4) Clear 64BIT_OUT_EN_x to return to normal output mode, or go to step 2) for the next simultaneous output setting.

In simultaneous Output mode, readback of values written into the output registers is not possible until 64BIT_DRIVE_x is set.

6.6 Timer

The TPMC685 has two identical timers that can be used by software for e.g. equidistant input sampling or output setting.

Each Timer has its own Timer Control Register and Timer Status Register.

The Timer Control Register is used to

- set the timer mode to “single cycle” or “continuous”
- enable / disable interrupt generation each time the timer expires
- set the runtime of the timer by TIMEBASE_x and TIME_x
    - TIMEBASE_x sets the timebase for the timer counter
    - TIME_x is the number of TIMEBASE_x units the timer will run
- Enable or disable the timer

The Timer Status register is used to readback the actual timer status.

- TIME_STAT_x displays the actual value of the timer counter
- TIMEBASE_STAT_x is the timebase the timer runs with
- TIMER_INT_EN_STAT_x displays if the timer will generate an interrupt when it expires
- TIMER_MODE_STAT_x shows if the timer is configured for single cycle or continuous mode
- TIMER_RUN_STAT_x shows if the timer is running or if it was/has stopped
- TIMER_EXPIRED_x shows if the timer has reached zero since the last reading of the Timer Status Register. If TIMER_INT_EN_x is set, TIMER_EXPIRED_x is the interrupt status bit for the timer interrupt.

To restart the timer when using the single cycle mode, the timer must first be disabled before it can be restarted by enabling the timer again.

The TPMC685 uses the PCI-Clock for the timers. In general, the PCI-Clock is 33 MHz as the TPMC685 is a 33MHz capable PMC. As the PCI specification allows the PCI-Clock to be in the range of 0 to 33 MHz, the accuracy of the timers also depends on the system’s actual PCI-Clock frequency.

While Interrupt acknowledge mode “Ack on Read” is used, the Timer Status Register should not be read outside the ISR (Interrupt Service Routine) context as such a read access could clear a previously asserted interrupt before the ISR has finished the interrupt handling. This could lead to a spurious interrupt because the ISR could not find the source for the interrupt, or the interrupt is removed before the ISR is started by the system.

6.7 Watchdog

To use the watchdog, do the following configuration steps:

1) set the watchdog time interval by WD_TIMEBASE and WD_TIME in the Watchdog Control Register
2) If the watchdog shall generate an interrupt, set WD_INT_EN in the Watchdog Control Register
3) If the TPMC685 shall freeze its outputs when the watchdog expires, then clear WD_SAVE_EN in the Watchdog Control Register. If the TPMC685 shall drive user defined output values when the watchdog expires, set WD_SAVE_EN.
4) If WD_SAVE_EN is set, write the user defined output values into the Watchdog Port Data Registers
5) Enable the watchdog
6) Read or write the Watchdog status register to retrigger the watchdog.

When the watchdog expires, any write to the Port Data Registers will not change any output until the watchdog is disabled.

The TPMC685 uses the PCI-Clock for the watchdog. In general, the PCI-Clock is 33 MHz as the TPMC685 is a 33MHz capable PMC. As the PCI specification allows the PCI-Clock to be in the range of 0 to 33 MHz, the accuracy of the watchdog timeout setting also depends on the system's actual PCI-Clock frequency.

While Interrupt acknowledge mode "Ack on Read" is used, the Watchdog Status Register should not be read outside the ISR (Interrupt Service Routine) context as such a read access could clear a previously asserted interrupt before the ISR has finished the interrupt handling. This could lead to a spurious interrupt because the ISR could not find the source for the interrupt, or the interrupt is removed before the ISR is started by the system. It is recommended to use write accesses to the Watchdog Status register for watchdog retriggering in this case.

6.8 Input Filter

Each I/O Port has its own input filter. This filter removes glitches and spikes, which can dramatically reduce the interrupt load. To use the input filter, it must be enabled and programmed with valid values for Timebase and Filter-Timer. Supported filter times range from 120ns to 65536ms. The filter time accuracy is ±25%.

If the Input filter is activated for an output-port, only the readback of the output values is delayed by the filter-time. Output values are not delayed.

The TPMC685 uses the PCI-Clock for the input filters. In general, the PCI-Clock is 33 MHz as the TPMC685 is a 33MHz capable PMC. As the PCI specification allows the PCI-Clock to be in the range of 0 to 33 MHz, the accuracy of the input filter time also depends on the system's actual PCI-Clock frequency.

6.9 Port Data Register

The TPMC685 has one Port Data Register for each I/O-Port.

Reading a Port Data Register always returns the value read from the I/O pin, filtered by the input filter if enabled.

If the input filter is enabled, it will take the selected filter time until a level change on the I/O-Line is visible in the Port Data Register. As interrupts are generated due to changes in the Port Data Register, the delay also affects the interrupt generation.

This is also true for ports configured as output. Do not enable input filter for output ports until you are sure to know what you do.

Data written to a Port Data Register is always stored inside the TPMC685. Readback of this data is only possible for ports configured as output. If a port is changed from input to output, the data previously written to the port data register is used by the output port. Use this to preload the port with correct data before changing its direction.

7 Pin Assignment – I/O Connector

7.1 Overview

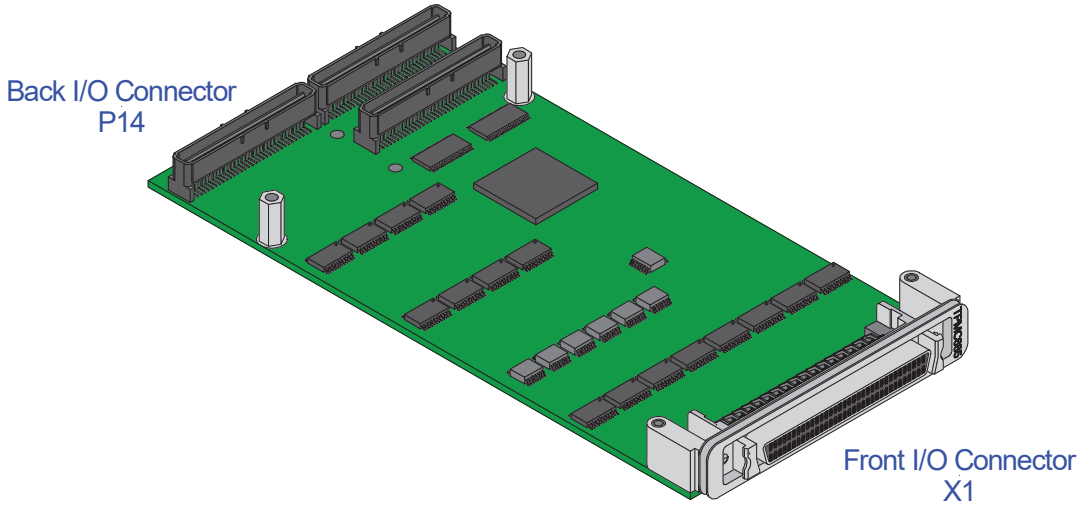

Figure 7-1 : I/O Connector Overview

7.2 Front I/O Connector X1

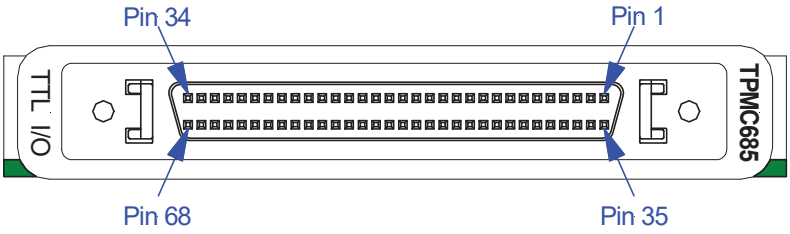

Figure 7-2 : Front Panel I/O Connector Pin Numbering

7.2.1 Connector Type

Pin-Count	68
Connector Type	HD68 SCSI-3 type female connector
Source & Order Info	AMP 787082-7 or compatible

7.2.2 Pin Assignment

Pin	Signal	Level
1	Port 0, I/O Line 0	5V TTL
2	Port 0, I/O Line 1	5V TTL
3	Port 0, I/O Line 2	5V TTL
4	Port 0, I/O Line 3	5V TTL
5	Port 0, I/O Line 4	5V TTL
6	Port 0, I/O Line 5	5V TTL
7	Port 0, I/O Line 6	5V TTL
8	Port 0, I/O Line 7	5V TTL
9	Port 1, I/O Line 0	5V TTL
10	Port 1, I/O Line 1	5V TTL
11	Port 1, I/O Line 2	5V TTL
12	Port 1, I/O Line 3	5V TTL
13	Port 1, I/O Line 4	5V TTL
14	Port 1, I/O Line 5	5V TTL
15	Port 1, I/O Line 6	5V TTL
16	Port 1, I/O Line 7	5V TTL
17	Port 2, I/O Line 0	5V TTL
18	Port 2, I/O Line 1	5V TTL
19	Port 2, I/O Line 2	5V TTL
20	Port 2, I/O Line 3	5V TTL
21	Port 2, I/O Line 4	5V TTL
22	Port 2, I/O Line 5	5V TTL
23	Port 2, I/O Line 6	5V TTL
24	Port 2, I/O Line 7	5V TTL
25	Port 3, I/O Line 0	5V TTL
26	Port 3, I/O Line 1	5V TTL
27	Port 3, I/O Line 2	5V TTL
28	Port 3, I/O Line 3	5V TTL
29	Port 3, I/O Line 4	5V TTL
30	Port 3, I/O Line 5	5V TTL
31	Port 3, I/O Line 6	5V TTL
32	Port 3, I/O Line 7	5V TTL
33	Port 4, I/O Line 0	5V TTL
34	Port 4, I/O Line 1	5V TTL

Pin	Signal	Level
35	Port 4, I/O Line 2	5V TTL
36	Port 4, I/O Line 3	5V TTL
37	Port 4, I/O Line 4	5V TTL
38	Port 4, I/O Line 5	5V TTL
39	Port 4, I/O Line 6	5V TTL
40	Port 4, I/O Line 7	5V TTL
41	Port 5, I/O Line 0	5V TTL
42	Port 5, I/O Line 1	5V TTL
43	Port 5, I/O Line 2	5V TTL
44	Port 5, I/O Line 3	5V TTL
45	Port 5, I/O Line 4	5V TTL
46	Port 5, I/O Line 5	5V TTL
47	Port 5, I/O Line 6	5V TTL
48	Port 5, I/O Line 7	5V TTL
49	Port 6, I/O Line 0	5V TTL
50	Port 6, I/O Line 1	5V TTL
51	Port 6, I/O Line 2	5V TTL
52	Port 6, I/O Line 3	5V TTL
53	Port 6, I/O Line 4	5V TTL
54	Port 6, I/O Line 5	5V TTL
55	Port 6, I/O Line 6	5V TTL
56	Port 6, I/O Line 7	5V TTL
57	Port 7, I/O Line 0	5V TTL
58	Port 7, I/O Line 1	5V TTL
59	Port 7, I/O Line 2	5V TTL
60	Port 7, I/O Line 3	5V TTL
61	Port 7, I/O Line 4	5V TTL
62	Port 7, I/O Line 5	5V TTL
63	Port 7, I/O Line 6	5V TTL
64	Port 7, I/O Line 7	5V TTL
65	GND	Ground
66	GND	Ground
67	GND	Ground
68	GND	Ground

Table 7-1 : Pin Assignment Front-I/O Connector

7.3 Back I/O Connector P14

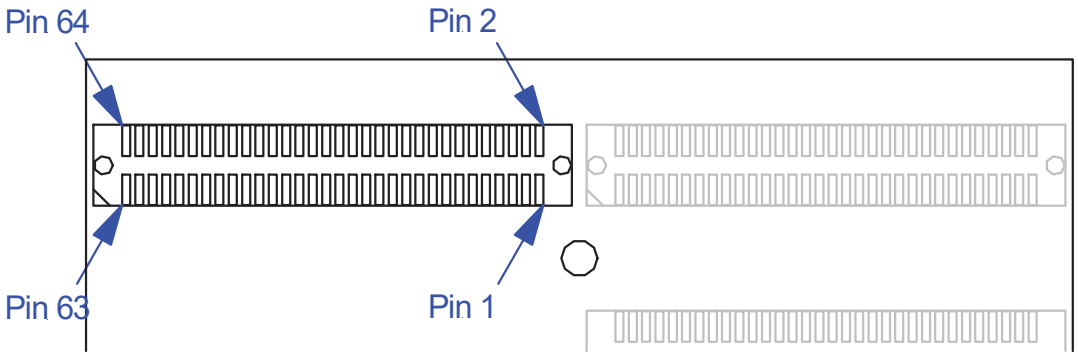

Figure 7-3 : Back I/O Connector P14 Pin Numbering

7.3.1 Connector Type

Pin-Count	64
Connector Type	64 pol. Mezzanine SMD Connector
Source & Order Info	Molex – 71436-2864 or compatible

7.3.2 Pin Assignment

Pin	Signal	Level
1	Port 8, I/O Line 0	5V TTL
2	Port 8, I/O Line 1	5V TTL
3	Port 8, I/O Line 2	5V TTL
4	Port 8, I/O Line 3	5V TTL
5	Port 8, I/O Line 4	5V TTL
6	Port 8, I/O Line 5	5V TTL
7	Port 8, I/O Line 6	5V TTL
8	Port 8, I/O Line 7	5V TTL
9	Port 9, I/O Line 0	5V TTL
10	Port 9, I/O Line 1	5V TTL
11	Port 9, I/O Line 2	5V TTL
12	Port 9, I/O Line 3	5V TTL
13	Port 9, I/O Line 4	5V TTL
14	Port 9, I/O Line 5	5V TTL
15	Port 9, I/O Line 6	5V TTL
16	Port 9, I/O Line 7	5V TTL
17	Port 10, I/O Line 0	5V TTL
18	Port 10, I/O Line 1	5V TTL
19	Port 10, I/O Line 2	5V TTL

Pin	Signal	Level
33	Port 12, I/O Line 0	5V TTL
34	Port 12, I/O Line 1	5V TTL
35	Port 12, I/O Line 2	5V TTL
36	Port 12, I/O Line 3	5V TTL
37	Port 12, I/O Line 4	5V TTL
38	Port 12, I/O Line 5	5V TTL
39	Port 12, I/O Line 6	5V TTL
40	Port 12, I/O Line 7	5V TTL
41	Port 13, I/O Line 0	5V TTL
42	Port 13, I/O Line 1	5V TTL
43	Port 13, I/O Line 2	5V TTL
44	Port 13, I/O Line 3	5V TTL
45	Port 13, I/O Line 4	5V TTL
46	Port 13, I/O Line 5	5V TTL
47	Port 13, I/O Line 6	5V TTL
48	Port 13, I/O Line 7	5V TTL
49	Port 14, I/O Line 0	5V TTL
50	Port 14, I/O Line 1	5V TTL
51	Port 14, I/O Line 2	5V TTL

Pin	Signal	Level
20	Port 10, I/O Line 3	5V TTL
21	Port 10, I/O Line 4	5V TTL
22	Port 10, I/O Line 5	5V TTL
23	Port 10, I/O Line 6	5V TTL
24	Port 10, I/O Line 7	5V TTL
25	Port 11, I/O Line 0	5V TTL
26	Port 11, I/O Line 1	5V TTL
27	Port 11, I/O Line 2	5V TTL
28	Port 11, I/O Line 3	5V TTL
29	Port 11, I/O Line 4	5V TTL
30	Port 11, I/O Line 5	5V TTL
31	Port 11, I/O Line 6	5V TTL
32	Port 11, I/O Line 7	5V TTL

Pin	Signal	Level
52	Port 14, I/O Line 3	5V TTL
53	Port 14, I/O Line 4	5V TTL
54	Port 14, I/O Line 5	5V TTL
55	Port 14, I/O Line 6	5V TTL
56	Port 14, I/O Line 7	5V TTL
57	GND / Port 15, I/O Line 0*	GND / TTL
58	GND / Port 15, I/O Line 1*	GND / TTL
59	GND / Port 15, I/O Line 2*	GND / TTL
60	GND / Port 15, I/O Line 3*	GND / TTL
61	GND / Port 15, I/O Line 4*	GND / TTL
62	GND / Port 15, I/O Line 5*	GND / TTL
63	GND / Port 15, I/O Line 6*	GND / TTL
64	GND / Port 15, I/O Line 7*	GND / TTL

Table 7-2 : Pin Assignment Back-I/O Connector

* -10 = I/O Line, -11 = GND