The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC700

32/16 Digital Outputs (24V, 0.5A)

High Side Switches

Version 1.1

User Manual

Issue 1.1.1

August 2014

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TPMC700-10R

32 digital outputs front panel I/O

TPMC700-11R

16 digital outputs front panel I/O

TPMC700-20R

32 digital outputs P14 I/O

TPMC700-21R

16 digital outputs P14 I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	September 1999
1.1	General Revision	April 2003
1.2	Description of optical isolation corrected	March 2004
1.3	Added differences of V1.1	June 2005
1.4	New address TEWS LLC	September 2006
1.1.0	New notation of HW Engineering Documentation Releases	November 2011
1.1.1	General Revision	August 2014

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1 Product Description

The TPMC700 is a PMC compatible module which provide 32 (16) digital outputs with galvanic isolation via optocouplers. All outputs resist short-circuits and are protected against thermal overload. The output drivers are capable of driving 0.5A continuous per channel as high side switch. A hardware watchdog clears all outputs in case of trigger failure.

The TPMC700-1xR provides front panel I/O with a HD50 SCSI-2 type connector, the TPMC700-2xR provides P14 I/O.

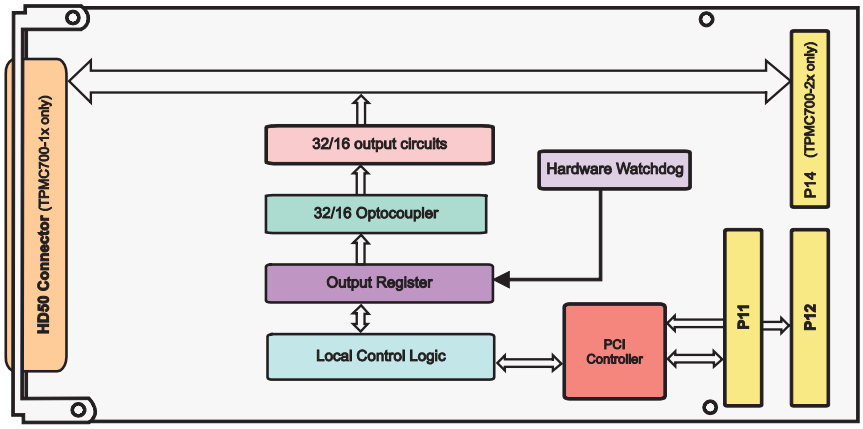

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface confirming to IEEE P1386/P1386.1 Single Size	
Electrical Interface	PCI Rev. 2.2 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip	PCI9030 (PLX Technology)	
I/O Interface		
Number of Channels		
Number of Outputs	TPMC700-10R/-20R: 32 digital outputs TPMC700-11R/-21R: 16 digital outputs	
Output Isolation	Optocouplers for galvanic isolation between system ground and output lines	
External Output Voltage	24V DC typical, 6V DC minimum, 48V DC maximum	
Output Current	0.5A typical (0.3A for voltages over 32V)	
Short Circuit Current	0.8A typical	
Output Voltage Drop	1.1V typical @0.5A	
Output Protection	Overload, short circuit, GND and Vs open wire protection, thermal shutdown	
Watchdog	Maximum trigger distance = 120ms	
I/O Connector	TPMC700-10R/-11R: HD50 SCSI-2 type connector (AMP 787395-5) TPMC700-20R/-21R: PMC P14 I/O (64 pin Mezzanine Connector)	
Physical Data		
Power Requirements	130mA typical @ +3.3V DC	
Temperature Range	Operating Storage	-25 °C to +85 °C -55°C to +125°C
MTBF	TPMC700-10R: 310 000h TPMC700-11R: 449 000h TPMC700-20R: 310 000h TPMC700-21R: 449 000h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	70 g	

Table 2-1 : Technical Specification

3 Local Space Addressing

3.1 PCI9030 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9030 local spaces.

PCI9030 Local Space	PCI9030 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	2 (0x18)	MEM	16	32	BIG	CPLD Register Space
1	3 (0x1C)	-	-	-	-	Not Used
2	4 (0x20)	-	-	-	-	Not Used
3	5 (0x24)	-	-	-	-	Not Used

Table 3-1 : PCI9030 Local Space Configuration

3.2 CPLD Register Space

PCI Base Address: PCI9030 PCI Base Address 2 (Offset 0x18 in PCI Configuration Space).

Offset to PCI Base Address 2	Register Name	Size (Bit)
0x0000	Data Output Register	32
0x0004	Control Register	32

Table 3-2 : CPLD Register Space

3.2.1 Data Output Register

The Data Output Register is a long word wide read/write register used to set or clear the outputs lines.

Bit	Symbol	Description	Access	Reset Value
31:0	OUTPUT 32 … OUTPUT 1	Set or clear the corresponding output line 1 = active 0 = inactive Bit 0 represents OUTPUT 1 …. Bit 31 represents OUTPUT 32	R/W	0

Table 3-3 : Data Output Register

After power-on or reset the Data Output Register is cleared to '0', all outputs are inactive.

3.2.2 Control Register

The Control Register is a 32 bit read/write register.

Bit	Symbol	Description	Access	Reset Value
31:4	-	Reserved (0 for reads)	-	0
3	WDOG_STAT	Watchdog Status bit 1 = indicate that the watchdog has recognized a failure and has disabled all output channels. The Output Register is locked. Writing '1' to this bit unlocks the Output Register. 0 = signals normal operation	R/W	0
2	-	Reserved (0 for reads)	-	0
1	WDOG_EN	Watchdog Enable bit for all 32 outputs 1 = enable watchdog function 0 = disable	R/W	0
0	-	Reserved (0 for reads)	-	0

Table 3-4 : Control Register

The watchdog status is only active if the watchdog is enabled.

4 PCI9030 Target Chip

4.1 PCI Configuration Registers (PCR)

4.1.1 PCI9030 Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	02BC 1498
0x04	Status		Command		Y	0280 0000
0x08	Class Code			Revision ID	N	118000 00
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers				Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers				Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0				Y	FFFFFFF0
0x1C	PCI Base Address 3 for Local Address Space 1				Y	00000000
0x20	PCI Base Address 4 for Local Address Space 2				Y	00000000
0x24	PCI Base Address 5 for Local Address Space 3				Y	00000000
0x28	PCI CardBus Information Structure Pointer				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	s.b. 1498
0x30	PCI Base Address for Local Expansion ROM				Y	00000000
0x34	Reserved			New Cap. Ptr.	N	000000 40
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00
0x40	PM Cap.		PM Nxt Cap.	PM Cap. ID	N	4801 00 01
0x44	PM Data	PM CSR EXT	PM CSR		Y	00 00 0000
0x48	Reserved	HS CSR	HS Nxt Cap.	HS Cap. ID	Y[23:16]	00 00 00 06
0x4C	VPD Address		VPD Nxt Cap.	VPD Cap. ID	Y[31:16]	0000 00 03
0x50	VPD Data				Y	00000000

Table 4-1 : PCI9030 Header

Subsystem-ID Value (Offset 0x2E): TPMC700-10R 0x000A

TPMC700-11R 0x000B

TPMC700-20R 0x0014

TPMC700-21R 0x0015

4.2 Local Configuration Register (LCR)

After reset, the PCI9030 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

The PCI base address for the PCI9030 Local Configuration Registers is PCI9030 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9030 PCI Configuration Register Space) or PCI9030 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9030 PCI Configuration Register Space).

Do not change hardware dependent bit settings in the PCI9030 Local Configuration Registers.

Offset from PCI Base Address	Register	Value
0x00	Local Address Space 0 Range	0x0FFF_FFF0
0x04	Local Address Space 1 Range	0x0000_0000
0x08	Local Address Space 2 Range	0x0000_0000
0x0C	Local Address Space 3 Range	0x0000_0000
0x10	Expansion ROM Range	0x0000_0000
0x14	Local Address Space 0 Local Base Address (Remap)	0x0000_0001
0x18	Local Address Space 1 Local Base Address (Remap)	0x0000_0000
0x1C	Local Address Space 2 Local Base Address (Remap)	0x0000_0000
0x20	Local Address Space 3 Local Base Address (Remap)	0x0000_0000
0x24	Expansion ROM Local Base Address (Remap)	0x0000_0000
0x28	Local Address Space 0 Bus Region Descriptor	0x1581_20A0
0x2C	Local Address Space 1 Bus Region Descriptor	0x0000_0000
0x30	Local Address Space 2 Bus Region Descriptor	0x0000_0000
0x34	Local Address Space 3 Bus Region Descriptor	0x0000_0000
0x38	Expansion ROM Bus Region Descriptor	0x0000_0000
0x3C	Chip Select 0 Base Address	0x0000_0009
0x40	Chip Select 1 Base Address	0x0000_0002
0x44	Chip Select 2 Base Address	0x0000_0002
0x48	Chip Select 3 Base Address	0x0000_0002
0x4C	Interrupt Control/Status	0x0000
0x4E	Serial EEPROM Write-Protected Address Boundary	0x0030
0x50	PCI Target Response, Serial EEPROM Control, and Initialization Control	0x0078_0000
0x54	General Purpose I/O Control	0x0020_06D2
0x70	Hidden1 Register for Power Management Data Select	0x0000_0000
0x74	Hidden 2 Register for Power Management Data Scale	0x0000_0000

Table 4-2 : PCI9030 Local Configuration Registers

4.3 Configuration EEPROM

After power-on or PCI reset, the PCI9030 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x27 : PCI9030 PCI Configuration Register Values
- Address 0x28 to 0x87 : PCI9030 Local Configuration Register Values
- Address 0x88 to 0xFF : Reserved

See the PCI9030 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x0326	0x1498	0x0280	0x0000	0x0780	0x0000	s.b.	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x4801	0x0000	0x0000
0x20	0x0000	0x4C06	0x0000	0x0003	0x0FFF	0xFFF0	0x0FFF	0xFFC0
0x30	0x0FFF	0xFE00	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0000	0x1001	0x0000	0x2001	0x0000	0x0000	0x0000	0x0000
0x50	0x1500	0xC0A0	0x1580	0xC062	0x1502	0x4120	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0009	0x0000	0x1021	0x0000	0x2081
0x70	0x0000	0x2181	0x0030	0x0041	0x0078	0x0000	0x026D	0xB6D2
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 4-3 : Configuration EEPROM

Subsystem-ID Value (Offset 0x0C): TPMC700-10R 0x000A

TPMC700-11R 0x000B

TPMC700-20R 0x0014

TPMC700-21R 0x0015

4.4 Local Software Reset

The PCI9030 Local Reset Output LRESETo# is used to reset the on board local logic.

The PCI9030 local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the PCI9030 local configuration register CNTRL (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of '1' resets the PCI9030 and issues a reset to the Local Bus (LRESETo# asserted). The PCI9030 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI9030 PCI and Local Configuration Registers are not reset. The PCI9030 PCI Interface is not reset.

5 Configuration Hints

5.1 Big / Little Endian

- PCI – Bus (Little Endian)

Byte 0	AD[7..0]
Byte 1	AD[15..8]
Byte 2	AD[23..16]
Byte 3	AD[31..24]

- Every Local Address Space (0...3) and the Expansion ROM Space can be programmed to operate in Big or Little Endian Mode.

Big Endian		**Little Endian**	
32 Bit		**32 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
Byte 2	D[15..8]	Byte 2	D[23..16]
Byte 3	D[7..0]	Byte 3	D[31..24]
16 Bit upper lane		**16 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
16 Bit lower lane			
Byte 0	D[15..8]		
Byte 1	D[7..0]		
8 Bit upper lane		**8 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
8 Bit lower lane			
Byte 0	D[7..0]		

Table 5-1 : Local Bus Little/Big Endian

Standard use of the TPMC700:

Local Address Space 0	32 bus in Big Endian Mode
Local Address Space 1	not used
Local Address Space 2	not used
Local Address Space 3	not used
Expansion ROM Space	not used

To change the Endian Mode use the Local Configuration Registers for the corresponding Space. Bit 24 of the according register sets the mode. A value of 1 indicates Big Endian and a value of 0 indicates Little Endian.

Use the PCI Base Address 0 + Offset or PCI Base Address 1 + Offset:

Short cut Offset	Name	
LAS0BRD	0x28	Local Address Space 0 Bus Region Description Register
LAS1BRD	0x2C	Local Address Space 0 Bus Region Description Register
LAS2BRD	0x30	Local Address Space 0 Bus Region Description Register
LAS3BRD	0x34	Local Address Space 0 Bus Region Description Register
EROMBRD	0x38	Expansion ROM Bus Region Description Register

You could also use the PCI - Base Address 1 I/O Mapped Configuration Registers.

6 Functional Description of Digital Outputs

6.1 Optical Isolation

The TPMC700 has 32 (TPMC700-10R/-20R) or 16 (TPMC700-11R/-21R) digital outputs. The standard signal level for these outputs is 24V DC. All outputs are isolated by optocouplers from the system and in two groups (output OUT1-16 against output OUT17-32) against each other.

Within these two groups there are four subgroups for the VS power supply which allow different supply voltages in groups of four, but referenced to the same GND.

Group	VS/standard 24V DC	Ground	Input
O 1	VS_O1	GND_OA	OUT 1 OUT 2 OUT 3 OUT 4
O 2	VS_ O2		OUT 5 OUT 6 OUT 7 OUT 8
O 3	VS_ O3		OUT 9 OUT 10 OUT 11 OUT 12
O 4	VS_ O4		OUT 13 OUT 14 OUT 15 OUT 16
O 5	VS_ O5	GND_OB	OUT 17 OUT 18 OUT 19 OUT 20
O 6	VS_ O6		OUT 21 OUT 22 OUT 23 OUT 24
O 7	VS_ O7		OUT 25 OUT 26 OUT 27 OUT 28
O 8	VS_ O8		OUT 29 OUT 30 OUT 31 OUT 32

Table 6-1 : Isolated Digital Outputs

6.2 Output Polarity

Each output can be individually switched to the according power supply VS_Ox (high side switch).

6.3 Overload Protection

The output drivers used on the TPMC700 are ‘smart drivers’ TDE1707. The maximum continuous output current is 0.5A. The output circuits are protected against overload, short circuit and over temperature. In case of such failure the corresponding output is switched off until the error condition is removed. The output returns automatically to normal operation, i.e. the state programmed in the Data Output Register.

6.4 Output Watchdog

Writing ‘1’ into bit 1 of the Global Control Register the hardware watchdog function is enabled. The status of the watchdog is indicated at bit 3 of the Global Control Register.

Any software accesses (read or write) to the Data Output Register will retrigger the watchdog. The maximum time between two accesses is set to 120ms. If the time expires without a software access all outputs go into “OFF” state. At the same time the watchdog status will change from ‘0’ to ‘1’ and locks the Data Output Register. This prevents a write access to the Data Output Register.

Writing ‘1’ to the watchdog status (bit 3 Control Register) clears this bit and also unlocks the Output Register. After unlocking the Data Output Register the output stays in the “OFF” state till the next write access to this register.

The watchdog is disabled after power-on or reset.

7 Programming Hints

7.1 Local Read/Write

The local CPLD register design is developed for a long word (32 bit) read/write access. A byte or word access will fail.

Use only long word read/write accesses to the TPMC700.

8 Installation

8.1 Output Wiring

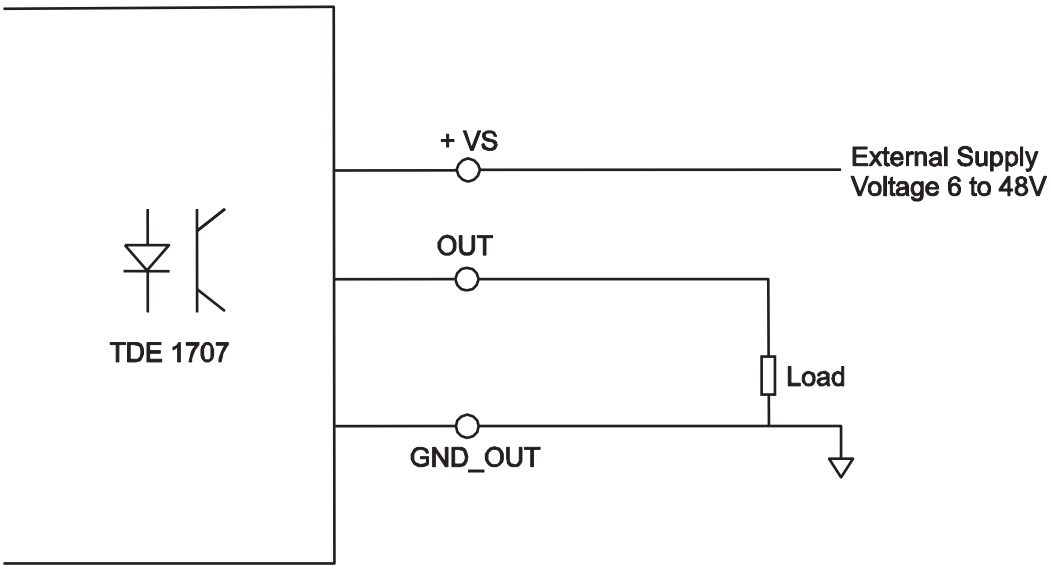

Figure 8-1 : Output Wiring as High Side Switch

9 Pin Assignment – I/O Connector

9.1 Front panel I/O

9.1.1 Connector

AMP 787395-5 or compatible

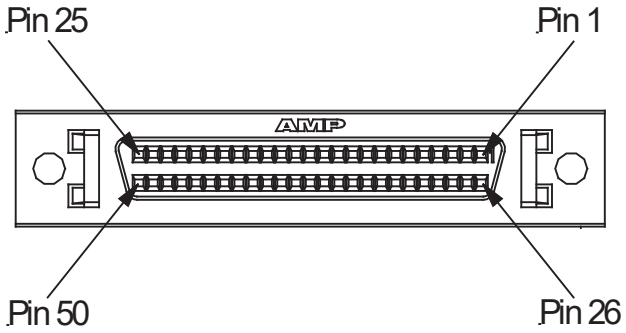

Figure 9-1 : Front Panel I/O Connector Numbering

9.1.2 Front panel I/O Assignment TPMC700-1xR

The subsequent figure shows the complete assembled pin front panel I/O connector. Bear in mind that variant -11R does not provide the channels 16 up to 32. Consequently, these are unconnected.

Pin	Signal	Pin	Signal
1	VS_O1	26	OUT 10
2	VS_O1	27	OUT 11
3	VS_O2	28	OUT 12
4	VS_O2	29	OUT 13
5	VS_O3	30	OUT 14
6	VS_O3	31	OUT 15
7	VS_O4	32	OUT 16
8	VS_O4	33	OUT 17
9	VS_O5	34	OUT 18
10	VS_O5	35	OUT 19
11	VS_O6	36	OUT 20
12	VS_O6	37	OUT 21
13	VS_O7	38	OUT 22
14	VS_O7	39	OUT 23
15	VS_O8	40	OUT 24
16	VS_O8	41	OUT 25
17	OUT 1	42	OUT 26
18	OUT 2	43	OUT 27
19	OUT 3	44	OUT 28
20	OUT 4	45	OUT 29
21	OUT 5	46	OUT 30
22	OUT 6	47	OUT 31
23	OUT 7	48	OUT 32
24	OUT 8	49	GND_OA
25	OUT 9	50	GND_OB

Table 9-1 : Pin Assignment Front I/O Connector TPMC700-1xR

Please check the maximum current of the used connection cable. Some standard cables (AWG28 50 pol.) are limited to 0.75 A per lead.

9.2 Back panel I/O

9.2.1 Mezzanine Card Connector P14

MOLEX 71436-216 or compatible

9.2.2 Back panel I/O Assignment TPMC700-2xR

The subsequent figure shows the complete assembled pin back panel I/O connector. Bear in mind that variant -21R does not provide the channels 16 up to 32. Consequently, these are unconnected.

Pin	Signal	Pin	Signal
1	VS_O1	27	OUT 11
2	VS_O1	28	OUT 12
3	VS_O2	29	OUT 13
4	VS_O2	30	OUT 14
5	VS_O3	31	OUT 15
6	VS_O3	32	OUT 16
7	VS_O4	33	OUT 17
8	VS_O4	34	OUT 18
9	VS_O5	35	OUT 19
10	VS_O5	36	OUT 20
11	VS_O6	37	OUT 21
12	VS_O6	38	OUT 22
13	VS_O7	39	OUT 23
14	VS_O7	40	OUT 24
15	VS_O8	41	OUT 25
16	VS_O8	42	OUT 26
17	OUT 1	43	OUT 27
18	OUT 2	44	OUT 28
19	OUT 3	45	OUT 29
20	OUT 4	46	OUT 30
21	OUT 5	47	OUT 31
22	OUT 6	48	OUT 32
23	OUT 7	49	GND_OA
24	OUT 8	50	GND_OB
25	OUT 9	51	NC
26	OUT 10	52 … 64	NC

Table 9-2 : Pin Assignment Back I/O Connector TPMC700-2xR