The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC861

4 Channel Isolated Serial Interface

RS422/RS485

Version 2.0

User Manual

Issue 2.0.0

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powerBridge Computer

Ehlbeek 15a
30938 Burgwedel
fon 05139-9980-0
fax 05139-9980-49

www.powerbridge.de
info@powerbridge.de

TEWS TECHNOLOGIES GmbH

Am Bahnhof 7 25469 Halstenbek, Germany
+49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
mail: info@tews.com www.tews.com

TPMC861-10R

4 channel isolated serial interface RS422/RS485

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	July 2001
1.1	Correction Figure “PCI Header”	April 2003
1.2	New address TEWS LLC	September 2006
1.0.3	New User Manual Issue Notation “Interrupt Status Register” at PCI Base-Address 2 + 0x24 renamed to “Interrupt Pending Register”	July 2009
1.0.4	Correction Figure “Serial Channel Interface Overview”	November 2010
1.0.5	Table 8-1 and Table 8-2: UART channel numbering changed from A-D to 0-3 Chapter 7.2: Mapping between Switch number and UART channel clarified	August 2017
2.0.0	User Manual update for TPMC861 V2.0	February 2021

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1 Product Description

The TPMC861 is a standard single-width 32 bit PMC module with four channels of high performance RS422/485-HD/FD serial interface. Each of the four channels is isolated from the system and against each other by optocoupler and on board DC/DC converter per channel.

The serial channels are accessible through a DB25 connector mounted in the front panel and via P14 I/O.

Each channel has a 128 byte transmit FIFO and a 128 byte receive FIFO to significantly reduce the overhead required to provide data to and get data from the transmitter and receivers. The FIFO trigger levels are programmable.

For RS422 and RS485-FD a four wire interface (RX+, RX-, TX+, TX-) plus isolated ground (GND) per channel is supported. For RS485-HD a two wire interface (DX+, DX-) plus isolated ground (GND) per channel is supported. The baud rate is individually programmable up to 460.8 Kbaud for each channel.

Interrupts are supported. All channels generate interrupts on PCI interrupt INTA. For fast interrupt source detection the TPMC861 provides a combined interrupt pending register.

Each receiver input and transmitter output of all channels is protected against electrostatic discharge (ESD) up to +/- 15kV according to IEC 1000-4-2.

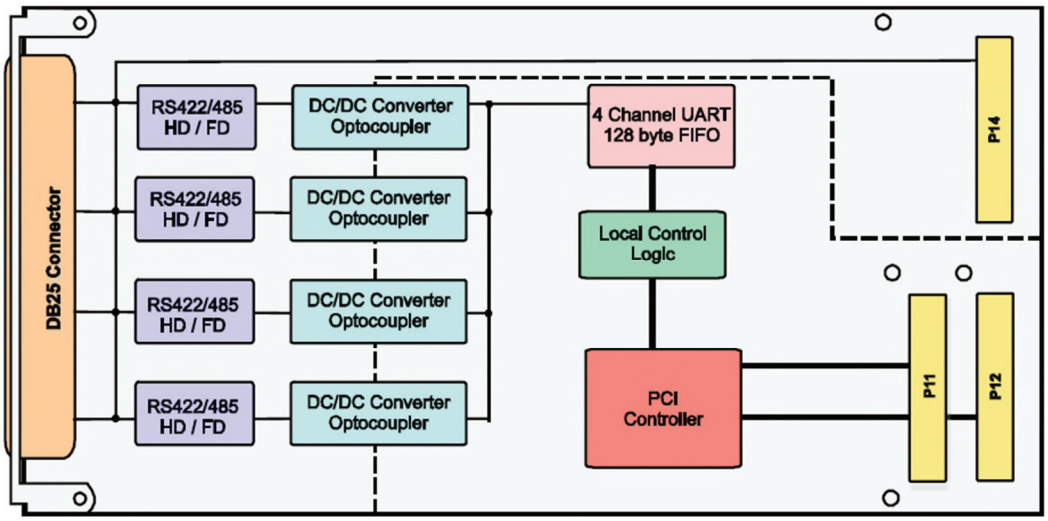


Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size	
Electrical Interface	PCI Rev. 3.0 compatible 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip	TEWS PCI Interface FPGA	
UART Controller	XR16C864 (4 channel UART, RS422/RS485)	
I/O Interface		
Number of UART Channels	4	
FIFO	128byte transmit FIFO, 128byte receive FIFO per channel	
Interrupts	PCI INTA for all channels, on board Interrupt Pending Register	
I/O Signals / Channel	TX+/-, RX+/-, isolated GND	
Maximum Transfer Rate	Each channel programmable up to 460.8 kbaud	
ESD Protection	+/- 15kV Human Body Model, +/- 6kV IEC1000-4-2 Model	
I/O Connector	DB25 female connector PMC P14 I/O (64 pin Mezzanine connector)	
Physical Data		
Power Requirements	3.3V: Not used 5V: RS422: 310mA (No Load); 470mA (Full Load 4 Channels Simultaneous Transmit and Receive @460.8 kbaud) RS485-FD-M: 440mA (No Load); 545mA (Full Load 4 Channels Simultaneous Transmit and Receive @460.8 kbaud) RS485-HD: 340mA (No Load); 545mA/425mA (Full Load 4 Channels Transmit/Receive @460.8 kbaud)	
Temperature Range	Operating Storage	-40°C to +85 °C -55°C to +125°C
MTBF	423797h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	78 g	

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

This PMC module is sensitive to static electricity.
Packing, unpacking and all other module handling has to be done with appropriate care.

3.2 Ground for Isolated I/O

I/O Connector's isolated ground signals must be connected to external ground.

4 Addressing

4.1 PCI Configuration Space

PCI CFG Register Address	Write '0' to all unused (Reserved) bits								PCI writeable	Initial Values (Hex Values)
	31	24	23	16	15	8	7	0		
0x00	Device ID				Vendor ID				N	035D 1498
0x04	Status				Command				Y	0480 0000
0x08	Class Code						Revision ID		N	070200 0A
0x0C	not supported		Header Type		not supported		not supported		Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers								Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers								Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0								Y	FFFFFFC0
0x1C	not supported								Y	00000000
0x20	not supported								Y	00000000
0x24	not supported								Y	00000000
0x28	not supported								N	00000000
0x2C	Subsystem ID				Subsystem Vendor ID				N	000A 1498
0x30	not supported								Y	00000000
0x34	Reserved						Cap. Ptr.		N	000000 00
0x38	Reserved								N	00000000
0X3C	MAX_LAT		MIN_GNT		Interrupt Pin		Interrupt Line		Y[7:0]	00 00 01 00
0X40-0XFF	Reserved									00000000

Table 4-1 : PCI Controller Header

4.1.1 PCI Address Space Overview

PCI BAR	PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	0x10	MEM	128	32	Little	PCI Controller Register Space
1	0x14	I/O	128	32	Little	
2	0x18	MEM	64	8	Little	Local Register Space

Table 4-2 : PCI Address Space Overview

4.1.2 Serial EEPROM Memory

The serial EEPROM memory contains by default the TEWS PCI Interface FPGA configuration data for compatibility reasons. However, the entire configuration data are stored within and loaded from the internal flash of the PCI target chip.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x035D	0x1498	0x0480	0x0000	0x0702	0x000A	0x000A	0x1498
0x10	0x0000	0x0000	0x0000	0x0101	0x4801	0x4801	0x0000	0x0000
0x20	0x0000	0x4C06	0x0000	0x0003	0xFFFF	0xFFC0	0x0000	0x0000
0x30	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x50	0x5420	0x80C0	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0011	0x0000	0x0027	0x0000	0x0023
0x70	0x0000	0x0000	0x0030	0x0041	0x0078	0x4000	0x0249	0x26D2
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 4-3 : Configuration EEPROM

4.2 PCI Controller Register Space

4.2.1 PCI Controller Configuration Register Map

The PCI base address for the PCI Controller Configuration Registers is PCI Base Address 0 (PCI Memory Space, Offset 0x10 in the PCI Configuration Space) or PCI Base Address 1 (PCI I/O Space, Offset 0x14 in the PCI Configuration Space).

Do not change hardware dependent bit settings in the PCI Controller Configuration Registers.

Offset from PCI Base Address	Register	Value	Description
0x00	Local Address Space 0 Range	0x0FFF_FFC0	Used memory space
0x04	Local Address Space 1 Range	0x0000_0000	Not used
0x08	Local Address Space 2 Range	0x0000_0000	Not used
0x0C	Local Address Space 3 Range	0x0000_0000	Not used
0x10	Local Exp. ROM Range	0x0000_0000	Not used
0x14	Local Re-map Register Space 0	0x0000_0001	Address Offset for Memory
0x18	Local Re-map Register Space 1	0x0000_0000	Not used
0x1C	Local Re-map Register Space 2	0x0000_0000	Not used
0x20	Local Re-map Register Space 3	0x0000_0000	Not used
0x24	Local Re-map Register ROM	0x0000_0000	Not used
0x28	Local Address Space 0 Descriptor	0x5420_80C0	Local Timing Address Space 0
0x2C	Local Address Space 1 Descriptor	0x0000_0000	Not used
0x30	Local Address Space 2 Descriptor	0x0000_0000	Not used
0x34	Local Address Space 3 Descriptor	0x0000_0000	Not used
0x38	Local Exp. ROM Descriptor	0x0000_0000	Not used
0x3C	Chip Select 0 Base Address	0x0000_0011	UART-Register
0x40	Chip Select 1 Base Address	0x0000_0027	Special Register
0x44	Chip Select 2 Base Address	0x0000_0023	Not used
0x48	Chip Select 3 Base Address	0x0000_0000	Not used
0x4C	Interrupt Control/Status	0x0041	Interrupt Configuration
0x4E	EEPROM Write Protect Boundary	0x0030	No write protection
0x50	Miscellaneous Control Register	0x0078_4000	Retry Delay not used due to PCI r2.2 Features enabled
0x54	General Purpose I/O Control	0x26D2_0249	All GP I/Os are outputs
0x70	Hidden1 Power Management data select	0x0000_0000	Not used
0x74	Hidden 2 Power Management data scale	0x0000_0000	Not used

Table 4-4 : PCI Controller Configuration Register Map

4.3 Local Register Space

4.3.1 Local Register Map

All local registers of the TPMC861 are accessible in the memory space of the PMC module.

The PCI base address for the Local Registers is PCI Base Address 2 (PCI Memory Space, Offset 0x18 in the PCI Configuration Space).

Offset from PCI Base Address 2	Description	Access Size (Bits)
0x00 to 0x07	UART Controller Channel 0 Register Sets	8
0x08 to 0x0F	UART Controller Channel 1 Register Sets	8
0x10 to 0x17	UART Controller Channel 2 Register Sets	8
0x18 to 0x1F	UART Controller Channel 3 Register Sets	8
0x20	FIFO Ready Register Channel 0-3	8
0x24	Interrupt Pending Register	8

Table 4-5 : Local Register Map Overview

4.3.2 UART Channel Register Set

Each of the four isolated serial channels of the TPMC861 is accessed in the PCI Memory Space by two sets of registers. Both register sets have a common register, the Line Control Register (LCR). Bit 7 of the Line Control Register is used to switch between the two register sets of a channel.

Register Set 1 is only accessible if bit 7 of the Line Control Register (LCR Address: PCI Base Address 2 + Channel Offset + 0x03) is set to '0'. After reset Register Set 1 is accessible.

PCI Base Address + Channel Offset +	Read Mode	Write Mode	Size
0x00	Receive Holding Register	Transmit Holding Register	Byte
0x01	Interrupt Enable Register	Interrupt Enable Register	Byte
0x02	Interrupt Status Register	FIFO Control Register	Byte
0x03	Line Control Register	Line Control Register	Byte
0x04	Modem Control Register	Modem Control Register	Byte
0x05	Line Status Register (LCR)	-	Byte
0x06	Modem Status Register	-	Byte
0x07	Scratchpad Register	Scratchpad Register	Byte

Table 4-6 : UART Channel Register Set 1

When LCR bit 7 is set to '0' and FCTR bit 6 is set to '1', the EMS Register is accessible:

PCI Base Address + Channel Offset +	Write-only	Size	Comment
0x07	Enhanced Mode Select Register (EMSR)	Byte	LCR[7] = 0, FCTR[6] = 1

To get to the first two registers of Register Set 2, bit 7 of the Line Control Register must be set to '1'.

PCI Base Address + Channel Offset +	Read/Write	Size	Comment
0x00	LSB of Divisor Latch	Byte	LCR[7] = 1, LCR ≠ 0xBF
0x01	MSB of Divisor Latch	Byte	LCR[7] = 1, LCR ≠ 0xBF

The Enhanced Registers in Register Set 2 are only accessible if the LCR is set to '0xBF'.

PCI Base Address + Channel Offset +	Read/Write	Size	Comment
0x00	Trigger Level Register (TRG)	Byte	LCR set to '0xBF'
0x01	Feature Control Register (FCTR)	Byte	LCR set to '0xBF'
0x02	Enhanced Feature Register (EFR)	Byte	LCR set to '0xBF'
0x03	Line Control Register (LCR)	Byte	Always accessible
0x04	Xon-1 Word	Byte	LCR set to '0xBF'
0x05	Xon-2 Word	Byte	LCR set to '0xBF'
0x06	Xoff-1 Word	Byte	LCR set to '0xBF'
0x07	Xoff-2 Word	Byte	LCR set to '0xBF'

Table 4-7 : UART Channel Register Set 2

4.3.3 Special Registers

The TPMC861 provides two special registers. For fast status detection there is a FIFO Ready Register covering all four channels and an Interrupt Pending Register covering all four channels.

Offset to PCI Base Address 2	Register Name	Size (Bit)
0x20	FIFO Ready Register Channel 0-3	8
0x24	Interrupt Pending Register Channel 0-3	8

Table 4-8 : Special Register

4.3.3.1 FIFO Ready Register

The FIFO Ready Register is a byte wide read only register. The FIFO Ready Register provides the status of the transmit and receive FIFOs of channel 0 to channel 3. Each TX and RX channel (0-3) has a dedicated 128 byte FIFO. When any of the RX/TX FIFOs becomes empty/full, the corresponding status bit is set in the FIFO Ready Register.

Bit	Symbol	Description	Access	Reset Value
7	RXRDY Channel 3	RX Ready Bit for channel 0-3 (active low) 0 = the corresponding receive FIFO level is above the programmed trigger level or a time-out has occurred 1 = the corresponding receive FIFO level is below the programmed trigger level	R	
6	RXRDY Channel 2			
5	RXRDY Channel 1			
4	RXRDY Channel 0			
3	TXRDY Channel 3	TX Ready Bit for channel 0-3 (active high) 0 = the corresponding transmit FIFO is full. The channel will not accept any more transmit data 1 = one or more empty locations exist in the corresponding FIFO	R	
2	TXRDY Channel 2			
1	TXRDY Channel 1			
0	TXRDY Channel 0			

Table 4-9 : FIFO Ready Register (Offset 0x20)

4.3.3.2 Interrupt Pending Register

The Interrupt Pending Register is a byte wide read only register located in the PCI Memory Space (PCI Base Address2 + 0x24) and reflects the interrupt status of the four UART channels. It is useful for fast interrupt source detection.

Bit	Symbol	Description	Access	Reset Value
7:4		Not used	-	-
3	Interrupt Channel 3	Interrupt Status of Channel 0-3 1 = interrupt is pending on corresponding channel 0 = no interrupt on corresponding channel	R	0x0
2	Interrupt Channel 2			
1	Interrupt Channel 1			
0	Interrupt Channel 0			

Table 4-10 : Interrupt Pending Register (Offset 0x24)

Interrupts from the four serial channels can be individual enabled in the ST16C654 serial controller. After reset all UART interrupts are disabled. Each of the four serial channels generates interrupts on the local interrupt 1 of the PCI target chip, which is mapped to PCI interrupt INTA. If the “PCI Interrupt Enable” bit in the PCI Controller’s Interrupt Control/Status Register is disabled (INTCSR bit 6 is set to ‘0’), the Interrupt Pending Register can be used as a polling register for interrupts of the four serial channels.

5 Configuration Hints

5.1 Local Software Reset

A Local Software Reset signal may be used to reset the on board local logic.

The local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the Miscellaneous Control Register CNTRL (offset 0x50) in the PCI Controller Register Space.

CNTRL[30] PCI Adapter Software Reset:

Value of 1 issues a reset to the local logic. The local logic remains in this reset condition until the PCI Host clears the bit. The contents of the PCI Controller Configuration Registers are not reset.

5.2 PCI Interrupt Control / Status

The UART channels generate interrupts on pin INTA# of the PCI bus. The combined interrupt status can be read at the Interrupt Control/Status Register INTCSR in the PCI Controller Register Space.

Bit	Symbol	Description	Access	Reset Value
31:8	-	Not used	R	0
7	SINT	Software Interrupt	R/W	0
6	PINT Enable	PCI Interrupt Enable	R/W	1
5	LINT2 Status	Local Interrupt 2 Status (not in use)	R	0
4	LINT2 Polarity	Local Interrupt 2 Polarity	R	0
3	LINT2 Enable	Local Interrupt 2 Enable	R	0
2	LINT1 Status	Local Interrupt 1 Status (UART channel interrupt)	R	0
1	LINT1 Polarity	Local Interrupt 1 Polarity	R/W	0
0	LINT1 Enable	Local Interrupt 1 Enable	R/W	1

Table 5-1 : Interrupt Control/Status Register (INTCSR, PCI Base Address 0 + 0x4C)

This register will be initialized after power-on with the initial values shown above.

The local interrupt 1 reflects the four UART channel interrupts. Bit 2 will be set if bit 0 is set and an interrupt is generated on one or more UART channels. For more information see chapter “Interrupt Pending Register”.

6 Programming Hints

6.1 Baud Rate Programming Formula

Each of the four serial isolated channels of the TPMC861 contains a dedicated programmable baud rate generator with a prescaler. The prescaler is controlled by MCR register bit 7 to divide the input clock by either 1 or 4. The clock output of the prescaler goes to the baud rate generator. The baud rate generator further divides this clock by a programmable divisor to obtain a 16x sampling rate clock of the serial data rate. The baud rate generator divisor can be programmed by the LSB and the MSB of the Divisor Latch Register (DLL and DLM). After reset, the MCR bit 7 of each channel is default '0' and the value of DLL and DLM is 0xFFFF.

The basic formula of baud rate programming is:

$$\frac{7.3728MHz}{16 * DIVISOR * (1 + 3 * MCR\_BIT7)}$$

Baud Rate MCR bit 7=0	Baud Rate MCR bit 7=1	Divisor
200	50	0x0900
300	75	0x0600
600	150	0x0300
1200	300	0x0180
2400	600	0x00C0
4800	1200	0x0060
9600	2400	0x0030
19.2K	4800	0x0018
28.8K	7200	0x0010
38.4K	9600	0x000C
76.8K	19.2K	0x0006
153.6K	38.4K	0x0003
230.4K	57.6K	0x0002
460.8K	115.2K	0x0001

Table 6-1 : Baud Rate Programming Table

7 Installation

7.1 Serial Channel Interface Overview

The Figure below shows the hardware scheme of a TPMC861 serial channel interface.

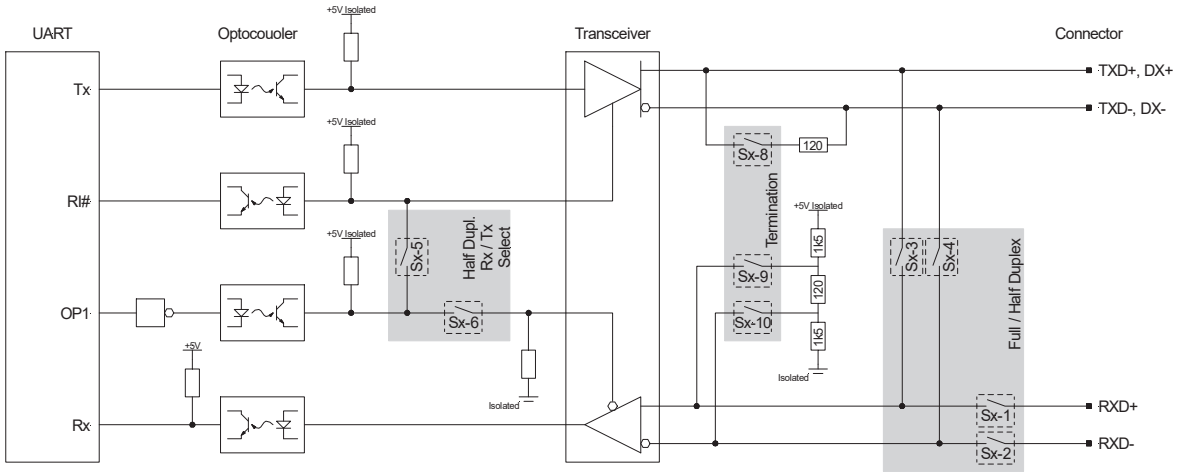


Figure 7-1 : Serial Channel Interface Overview

7.2 Serial Channel Interface Configuration

The isolated serial channel interface is configurable by DIP switch for each channel individually. There is a 10 position DIP switch for each of the 4 isolated serial channels.

S**x-y** with **x** =1 to 4 for the serial channel 0 to 3 DIP switch, and **y** = 1 to 10 for the switch position number y on the serial channel DIP switch.

DIP-SWITCH FUNCTION		
SUB-SWITCH ID	**Function Group**	**Function**
Sx-1, Sx-2	Duplex Mode Configuration 1	ON: RS422 and RS485 FD Modes OFF: RS485 HD Mode
Sx-3, Sx-4	Duplex Mode Configuration 2	ON: RS485 HD Mode OFF: RS422 and RS485 FD Modes
Sx-5	Transmitter Enable Control	ON: Controlled by 16C864 OFF: Transmitter Enabled
Sx-6	Receiver Enable Control	ON: Controlled by 16C864 OFF: Receiver Enabled
Sx-7	Reserved	
Sx-8	Transmit Line Termination	ON: 120R Transmit Line Termination OFF: No Transmit Line Termination
Sx-9, Sx-10	Receive Line Termination	ON: 120R Receive Line Termination OFF: No Receive Line Termination

FD: Full Duplex, HD: Half Duplex

Table 7-1 : DIP Switch Function

	Sx-1	Sx-2	Sx-3	Sx-4	Sx-5	Sx-6	Sx-7	Sx-8	Sx-9	Sx-10
RS422							X			
RS485 FD-M							X			
RS485 FD-S							X			
RS485 HD							X			

Switch Closed (ON)

Switch Open (OFF)

Switch setting depends on bus configuration

FD-M : Full Duplex Master
FD-S : Full Duplex Slave
HD : Half Duplex
X = Reserved

Table 7-2 : DIP Switch Configuration

7.3 DIP Switch Locations

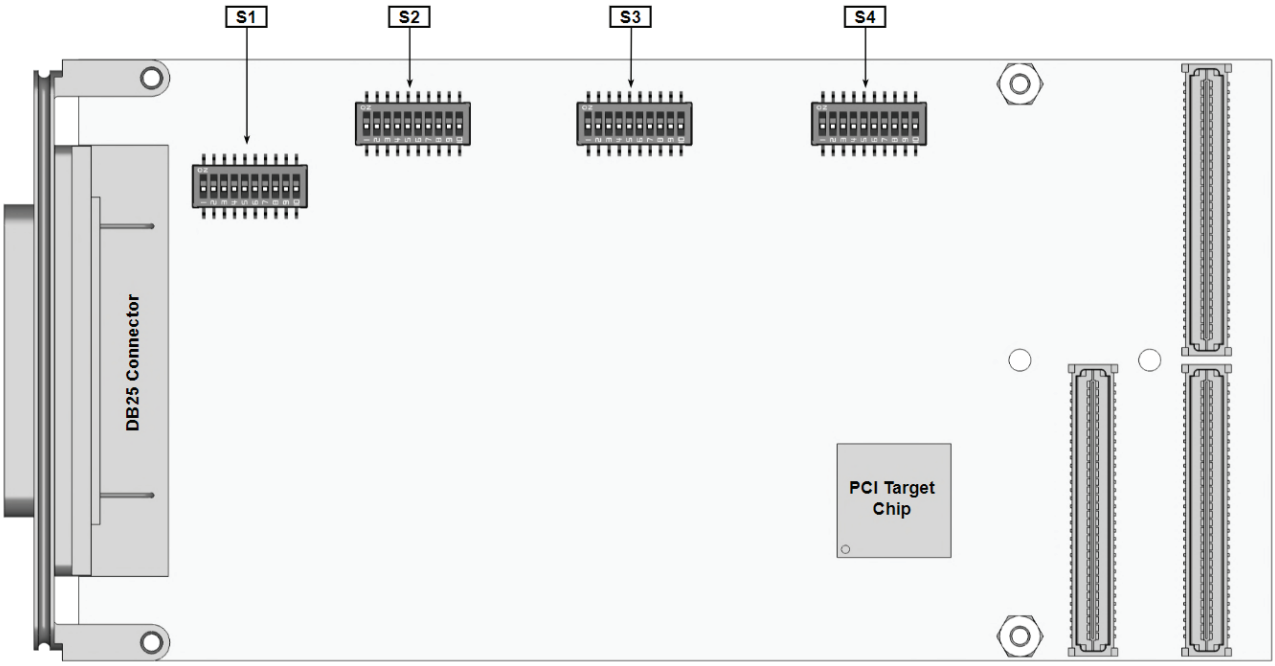


Figure 7-2 : DIP Switch Locations

7.4 Default Configuration

All 4 channels are configured to RS422 mode by factory default.

8 Pin Assignment – I/O Connector

8.1 Front panel DB25 Connector

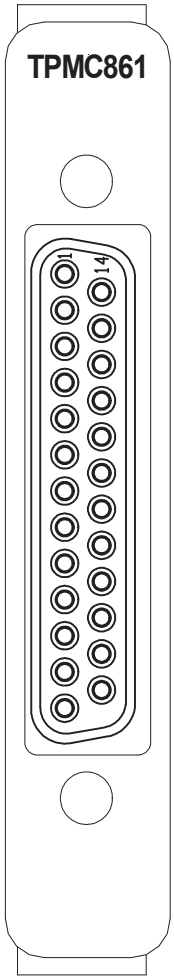
Pin	TPMC861 RS485-HD	TPMC861 RS422 RS485-FD		Comment
1	DX0-	TXD0-		Serial Channel 0
2	DX0+	TXD0+		Serial Channel 0
3	GND_0	GND_0		Isolated Ground Channel 0
4	DX1-	TXD1-		Serial Channel 1
5	DX1+	TXD1+		Serial Channel 1
6	GND_1	GND_1		Isolated Ground Channel 1
7	DX2-	TXD2-		Serial Channel 2
8	DX2+	TXD2+		Serial Channel 2
9	GND_2	GND_2		Isolated Ground Channel 2
10	DX3-	TXD3-		Serial Channel 3
11	DX3+	TXD3+		Serial Channel 3
12	GND_3	GND_3		Isolated Ground Channel 3
13	NC	NC		Not connected
14		RXD0-		Serial Channel 0
15		RXD0+		Serial Channel 0
16	GND_0	GND_0		Isolated Ground Channel 0
17		RXD1-		Serial Channel 1
18		RXD1+		Serial Channel 1
19	GND_1	GND_1		Isolated Ground Channel 1
20		RXD2-		Serial Channel 2
21		RXD2+		Serial Channel 2
22	GND_2	GND_2		Isolated Ground Channel 2
23		RXD3-		Serial Channel 3
24		RXD3+		Serial Channel 3
25	GND_3	GND_3		Isolated Ground Channel 3

Table 8-1 : Front panel DB25 female connector

8.2 Mezzanine Card I/O Connector P14

Pin	TPMC861 RS485-HD	TPMC861 RS422 RS485-FD	Comment
1	GND_0	GND_0	Isolated Ground Channel 0
2	DX0-	TXD0-	Serial Channel 0
3	DX0+	TXD0+	Serial Channel 0
4		RXD0-	Serial Channel 0
5		RXD0+	Serial Channel 0
6	GND_1	GND_1	Isolated Ground Channel 1
7	DX1-	TXD1-	Serial Channel 1
8	DX1+	TXD1+	Serial Channel 1
9		RXD1-	Serial Channel 1
10		RXD1+	Serial Channel 1
11	GND_2	GND_2	Isolated Ground Channel 2
12	DX2-	TXD2-	Serial Channel 2
13	DX2+	TXD2+	Serial Channel 2
14		RXD2-	Serial Channel 2
15		RXD2+	Serial Channel 2
16	GND_3	GND_3	Isolated Ground Channel 3
17	DX3-	TXD3-	Serial Channel 3
18	DX3+	TXD3+	Serial Channel 3
19		RXD3-	Serial Channel 3
20		RXD3+	Serial Channel 3
21..64	NC	NC	Not connected

Table 8-2 : Mezzanine Card I/O Connector P14