XMC-CAN/402-4-FD

XMC Board with 4 CAN FD Interfaces, optional IRIG-B

XMC Board with Altera® FPGA for 4x CAN FD via DSUB25

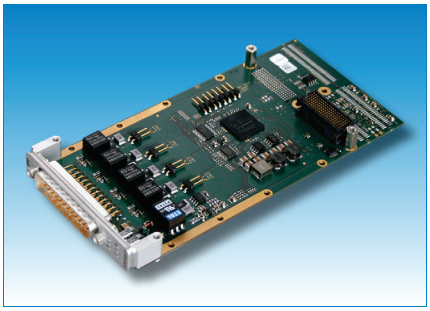
- *High-Speed CAN FD interfaces according to ISO 11898-2, up to 5 Mbit/s*
- *Bus mastering and local data management by FPGA (esdACC)*
- *PCI bus according to PCI Local Bus Specification 3.0*
- *Selectable CAN termination on board*
- *Supports MSI (Message Signaled Interrupts)*
- *All I/O signals via 25-pin DSUB in the front panel*
- *Optional IRIG-B input*

Wide Range of OS Support and Advanced CAN Diagnostic

- *Software drivers for Windows®and Linux® included free of charge*
- *Optional CAN layer 2 software drivers for real-time operating systems*
- *CANopen®, J1939 and ARINC 825 protocol libraries available*
- *ISO 16845:2004 certified esd Advanced CAN Core (esdACC) technology*
- *High resolution hardware timestamps*

Customization on Request

- *Extended temperature range: -40° C … +75° C*
- *Error simulation support*
- *All signals via Rear I/O*



CAN FD

The XMC-CAN/402-4-FD comes with four independent CAN FD interfaces according to ISO 11898-1:2015, which are driven by the ISO 16845:2004 certified esdACC (esd advanced CAN Core) implemented in the Altera FPGA. ***The XMC-CAN/402-4-FD is fully backwards compatible with CAN and can also be used in Classical CAN applications.***

CAN Data Management

The FPGA supports bus mastering (first-party DMA) to transfer data to the host memory. This results in a reduction of overall latency on servicing I/O transactions in particular at higher data rates and a reduced host CPU load.
Due to the usage of MSI (Message Signaled Interrupts) the XMC-CAN/402-4-FD can be operated for example in Hypervisor environments.
The XMC-CAN/402-4-FD provides high resolution 64-bit hardware timestamps for CAN messages.

The XMC-CAN/402-4-FD-IRIG-B offers an additional IRIG-B interface via DSUB25 for analog or RS-422 IRIG-B coded signals. Both inputs are electrically isolated. IRIG-B evaluation is controlled by an 8051 microcontroller integrated in the FPGA.

Software Support

Windows and Linux (NTCAN-API)
The CAN layer 2 drivers for Windows and Linux are included in the scope of delivery.

Realtime OS (NTCAN-API)
CAN layer 2 drivers for QNX®, RTX(64), VxWorks® and OnTime RTOS-32 can be ordered separately.

Higher Layer Protocols
(Classical CAN application only)
Higher Layer Protocols are available for many operating systems (see order info):

- *CANopen Master- and Slave-Stack*
- *J1939*
- *ARINC 825*

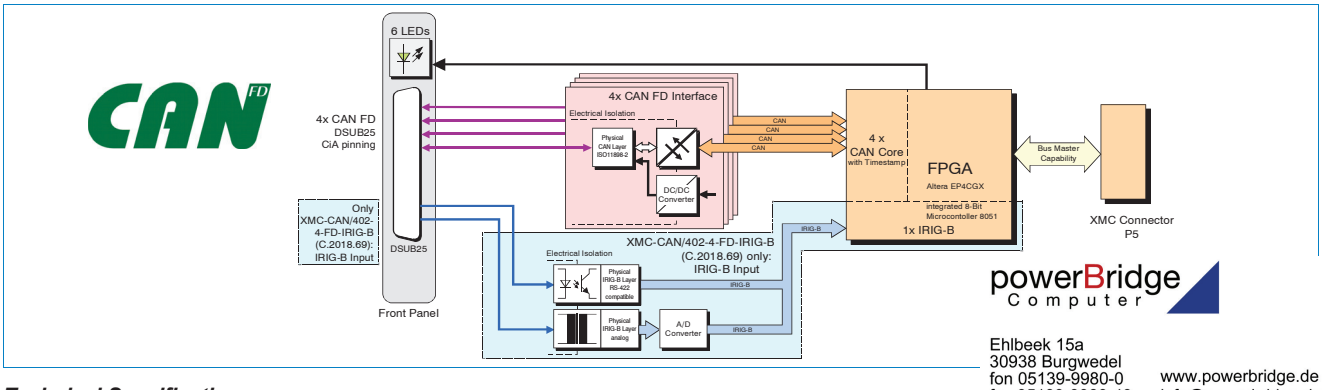
Additional free-of-charge esd CAN tools for Windows are downloadable from our website. The tools offer efficient setup and analysis of CAN applications and networks.

Customization on Request

Customized options are available for customized series production in reasonable quantities. Please contact our sales team for detailed information.

Related Products

The PMC-CAN/402-4-FD comes with a PMC interface instead of the XMC interface.



powerBridge Computer

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Technical Specifications:

PCI Express® Interface:	
PCIe® port	*PCI Express Spec. R1.0a, Link width 1x, PCI bus master capability*
CAN:	
Interface	*4x interface according to ISO11898-2, electrical isolation, Bit rates from 10 kbit/s up to 5 Mbit/s*
CAN controller	*esdACC in EP4CGX Altera FPGA, according to ISO 11898-1:2015*
General:	
Ambient temp.	*0 °C ... +75 °C*
Rel. humidity	*Max. 90 % (non-condensing)*
Power supply	*3.3 V / I_{MAX}: 1 A, I_{TYP}: 750 mA*
Dimensions	*149 mm x 74 mm x 10 mm*
Connector	*XMC: P5 (according to IEEE 1386) CAN: DSUB25 (4x CAN FD)*

Order Information:		
Hardware		*Order No.*
XMC-CAN/402-4-FD	*XMC Board, 4x CAN FD via DSUB25*	*C.2018.68*
XMC-CAN/402-4-FD -IRIG-B as C.2018.68, with additional IRIG-B		*C.2018.69*

Order Information (Continued):		
Accessories		*Order No.*
CAN/400-4-1C4 1xDSUB25-to-4xDSUB9	*Adapter cable to C.2018.68, DSUB25 female to 4x DSUB9 male, length: 0.5 m*	*C.2047.19*
CAN/400-4-1C5 1xDSUB25-to-5xDSUB9	*Adapter to C.2018.69, DSUB25 female to 4x DSUB9 male + 1x DSUB9 female*	*C.2047.18*
Software Support[1]		
CAN layer 2 drivers for Windows/Linux are included in delivery free of charge.		
Additional CAN layer 2 object licences including CD-ROM:		
CAN-DRV-LCD QNX	*Object licence for QNX6, QNX7*	*C.1101.32*
CAN-DRV-LCD VxWorks	*Object licence for WxWorks*	*C.1101.55*
CAN-DRV-LCD RTX	*Object licence for RTX64*	*C.1101.35*
CAN-DRV-LCD On Time RTOS-32	*Object licence*	*C.1101.45*
Higher CAN layer protocols including CD-ROM for Classical CAN Application:		
CANopen-LCD Windows/Linux, RTX, QNX or VxWorks		*C.1101.xx*
J1939 stack for Windows or Linux		*C.1130.xx*
ARINC 825-LCD for Windows/Linux, RTX, QNX or VxWorks		*C.1140.xx*
Related Products:		
PMC-CAN/402-4-FD	*PMC Board, 4x CAN FD via DSUB9*	*C.2028.68*

[1] *For detailed information about driver availability for your operating system please contact our sales team.*

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XMC-CAN/402-4-FD

Driven by esdACC-FD (Advanced CAN Core)

Basic Product Features:

- CAN ISO 11898-1:2015 protocol compatibility
- Tested and certified acc. to ISO CAN Conformance Tests "ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan"
- 11-bit and 29-bit CAN IDs
- Supported bit rates from 10 kbit/s up to 5 Mbit/s
- Receive buffer (64 CAN messages)
- Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (hardware supported bit rate detection)
- Acceptance filter (4-byte code, 4-byte mask)
- Self reception mode (reception of 'own' messages)
- Busload measurement

Superior esdACC Features [1]:

- Operating system independently programmable via esd's NTCAN-API
- 32-bit register interface optimized for CAN needs
  - Easy to program
  - Transmission and reception of CAN frames with a minimum of register accesses
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 12.5 ns)
  - Timestamping complies with the CiA® 603 specification
  - On hardware with IRIG-B interfaces IRIG-B time is used for timestamping
- TX FIFO (16 CAN frames deep)
  - Providing the means to generate 100% busload even with non-realtime operating systems
  - Providing the means for real back-to-back transmission
- Timestamped Tx FIFO (16 CAN frames deep)
  - High priority
  - 64 bit timestamp
  - Bit time accuracy for CAN transmission
- Frame accurate abortion of transmissions with minimum delay
  - e.g. for driver timeouts
  - ISO 11898-1:2015 conform
  - Aborted frames in FIFO won't be blocked by low priority TX

Superior esdACC Features (continued) [1]:

- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
- Optional integration with 32-bit microcontroller to further relieve host CPU
- Optional different sources for timestamps (e.g. IRIG-B)
- Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
- The esdACC IP core has been verified on Xilinx® Spartan® and Altera® Cyclone® FPGAs.

[1] Availability of the Superior esdACC Features depends on the operating system. Please contact our sales team for further information.

For further information on the esdACC IP Core please contact our sales team.

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