CAN-PCIe/402-FD

PCI Express® Board with up to 4 CAN-FD Interfaces

Single Lane PCIe Board with Intel® FPGA for up to 4x CAN FD

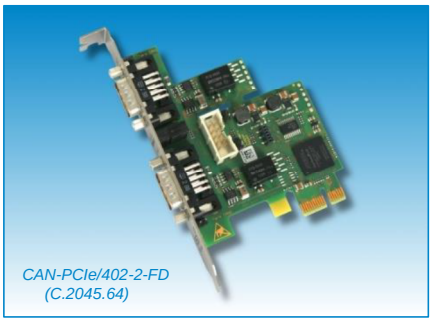
- *1x,2x or 4x CAN FD interfaces according to ISO 11898-2, up to 8 Mbit/s*
- *Bus mastering and local data management by FPGA (esdACC)*
- *PCIe® interface according to PCI Express Specification R1.0a*
- *Selectable CAN termination on board*
- *Supports MSI (Message Signaled Interrupts)*

Wide Range of Operating System Support and Advanced CAN Diagnostic

- *Software drivers for Windows® and Linux® included free of charge*
- *Optional CAN layer 2 software drivers for real-time operating systems*
- *CANopen®, J1939 and ARINC 825 protocol libraries*
- *ISO 16845:2004 certified esd Advanced CAN Core (esdACC) technology*

Variety of Product Designs

- *4x CAN FD via 1x DSUB37*
- *Low profile version for 1x or 2x CAN FD*



CAN-PCIe/402-2-FD (C.2045.64)

Wide Choice of Hardware Designs

The CAN-PCIe/402-FD is a PC board designed for the PCIe bus that features one (CAN-PCIe/402-1-FD) or two (CAN-PCIe/402-2-FD) electrically isolated CAN FD interfaces according to ISO 11898-2 via DSUB9 connectors.
Equipped with up to two CAN FD interfaces the board is available as low-profile versions (CAN-PCIe/402-1-LP-FD and -LP2-FD).
Four CAN FD interfaces can be connected via one 37-pin DSUB connector in the version CAN-PCIe/402-B4-FD/1Slot.

CAN FD

The CAN FD interfaces are designed according to ISO 11898-1:2015. They are driven by the ISO 16845:2004 certified esdACC (esd advanced CAN Core) implemented in the Intel FPGA.
All CAN FD versions are fully back-wards compatible with CAN and can also be used in Classical CAN applications.

CAN Data Management

The FPGA supports bus mastering (first-party DMA) to transfer data to the host memory. This results in a reduction of overall latency on servicing I/O transactions in particular at higher data rates and a reduced host CPU load.
Due to the usage of MSI (Message Signaled Interrupts) the CAN-PCIe/402-FD can be operated for example in Hypervisor environments.
The CAN-PCIe/402-FD provides high resolution hardware timestamps.

Software Support

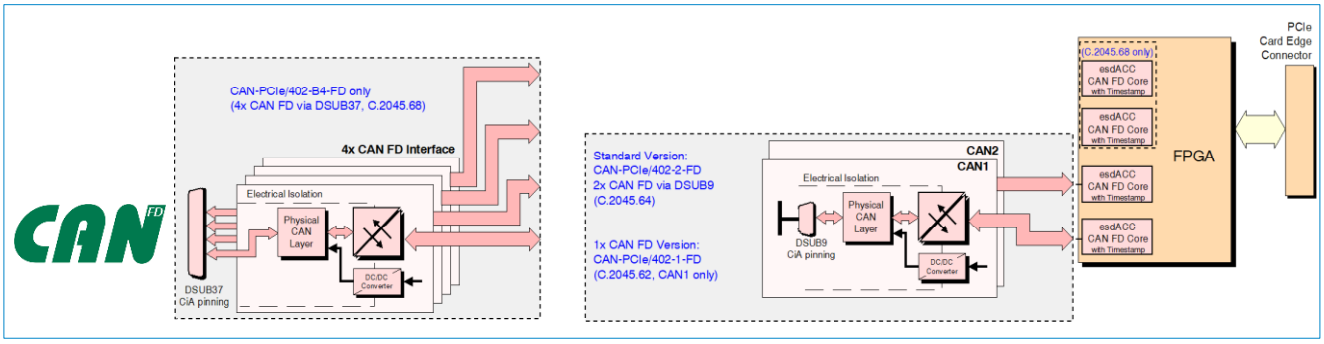
Windows and Linux (NTCAN-API)
The CAN layer 2 drivers for Windows and Linux are included in the scope of delivery.

Real-time OS (NTCAN-API)
CAN layer 2 drivers for QNX® RTX® and RTX64® can be ordered separately.

Higher Layer Protocols
(Classical CAN application only)
Higher Layer Protocols are available for many operating systems (see order info):
• CANopen Master- and Slave-Stack
• J1939
• ARINC825

Customization on Request

Customized options are available for customized series production in reasonable quantities. Please contact our sales team for detailed information.



Technical Specifications:

PCI Express Interface:	
PCIe port	*PCI Express Spec. R1.0a, Link width 1x*
CAN:	
Interface	*1x, 2x or 4x CAN FD interfaces according to ISO 11898-2, bit rates from 10 kbit/s up to 8 Mbit/s (with the same CAN transceiver), with or without electrical isolation*
CAN controller	*esdACC in EP4CGX Intel FPGA, acc. to ISO 11898-1:2015*
General:	
Power supply	*3.3 V: 2x CAN I_{MAX} = 280 mA, 4x CAN I_{MAX} = 290 mA* *12 V: 2x CAN I_{MAX} = 180 mA, 4x CAN I_{MAX} = 230 mA*
Ambient temp.	*0 °C ... +75 °C*
Rel. humidity	*Max. 90 % (non-condensing)*
Connector	*PCIe: PCIe card edge connector* *CAN: All except C.2045.68: 1x 9-pin DSUB per CAN channel, pin contacts* *C.2045.68 only: 1x 37-pin DSUB (4 CAN channels), pin contacts*
Weight	*CAN-PCIe/402-2-FD: 60 g*

Order Information:		
Hardware		*Order No.*
CAN-PCIe/402-1-FD	*1x CAN FD (CAN1 only), via DSUB9*	*C.2045.62*
CAN-PCIe/402-2-FD	*2x CAN FD (CAN1, CAN2) via DSUB9*	*C.2045.64*
CAN-PCIe/402-B4-FD/1Slot	*4x CAN FD via DSUB37 connector*	*C.2045.68*
CAN-PCIe/402-1-LP-FD	*Low-profile format, 1x CAN FD (CAN1)*	*C.2045.92*
CAN-PCIe/402-1-LP2-FD	*Low-profile format, 1x CAN FD (CAN2)*	*C.2045.94*
Accessories		
CAN-PCI/4XX- 4-FD-1C4	*Adapter cable DSUB37 to 4x DSUB9*	*C.2045.18*
Software Support [1]		
CAN layer 2 drivers for Windows/Linux are included in delivery free of charge. Additional CAN layer 2 object licences including CD-ROM:		
CAN-DRV-LCD QNX	*Object Licence for QNX6, QNX7*	*C.1101.32*
CAN-DRV-LCD RTX	*Object Licence for RTX64*	*C.1101.35*
Higher CAN layer protocols including CD-ROM for Classical CAN Application:		
CANopen-LCD Windows/Linux, RTX or QNX		*C.1101.xx*
J1939 stack for Windows, Linux		*C.1130.xx*
ARINC 825-LCD Windows/Linux, RTX or QNX		*C.1140.xx*

1 For detailed information about driver availability for your operating system please contact our sales team.

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CAN-PCIe/402-FD

Driven by esdACC-FD (Advanced CAN Core)

Basic Product Features:

- *CAN ISO 11898-1:2015 protocol compatibility*
- *Tested and certified acc. to ISO CAN Conformance Tests "ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan"*
- *11-bit and 29-bit CAN IDs*
- *Supported bit rates: From 10 kbit/s up to 8 Mbit/s*
- *Receive buffer (64 CAN messages)*
- *Complete access to CAN error counters*
- *Programmable error warning limit*
- *Error code capture register*
- *Error interrupt for each CAN bus error*
- *Arbitration lost interrupt with detailed bit position*
- *Listen only mode (no acknowledge, no active error flags)*
- *Automatic bit rate detection (hardware supported bit rate detection)*
- *Self-reception mode (reception of 'own' messages)*
- *Busload measurement*

Superior esdACC Features [1]:

- *Operating system independently programmable via esd's NTCAN-API*
- *32-bit register interface optimized for CAN needs*
  - *Easy to program*
  - *Transmission and reception of CAN frames with a minimum of register accesses*
- *RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 12.5 ns)*
  - *Timestamping complies with the CiA 603 specification*
  - *On hardware with IRIG-B interfaces IRIG-B time is used for timestamping*
- *TX FIFO (16 CAN frames deep)*
  - *Providing the means to generate 100% busload even with non-real-time operating systems*
  - *Providing the means for real back-to-back transmission*
- *Timestamped Tx FIFO (16 CAN frames deep)*
  - *High priority*
  - *64-bit timestamp*
  - *Bit time accuracy for CAN transmission*
- *Frame accurate abortion of transmissions with minimum delay*
  - *e.g. for driver timeouts*
  - *ISO11898-1:2015 conform*
  - *Aborted frames in FIFO won't be blocked by low priority TX*

Superior esdACC Features (continued) [1]:

- *Hardware timer to provide accurate software timeouts beyond operating system accuracy*
- *Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)*
- *Optional different sources for timestamps (e.g. IRIG-B)*
- *Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content*
- *The esdACC IP core has been verified on Xilinx® Spartan® and Intel® Cyclone® FPGAs.*

[1] Availability of the Superior esdACC Features depends on the operating system. Please contact our sales team for further information.

For further information on the esdACC IP Core please contact our sales team.

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