XMC-CPU/Zulu

XMC UltraScale+™ Zynq® MPSoC Board with integrated FPGA

Hardware Manual

to Product V.2031.01

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Notes

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This manual contains important information and instructions on safe and efficient handling of the XMC-CPU/Zulu. Carefully read this manual before commencing any work and follow the instructions.
The manual is a product component, please retain it for future use.

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Document History

The changes in the document listed below affect changes in the hardware as well as changes in the description of the facts, only.

Rev.	Chapter	Changes versus previous version	Date
1.0	-	First English manual	2021-03-09
1.1		Technical Information added	2022-06-23

Technical details are subject to change without further notice.

Classification of Warning Messages and Safety Instructions

This manual contains noticeable descriptions, warning messages and safety instructions, which you must follow to avoid personal injuries or death and property damage.

This is the safety alert symbol.
It is used to alert you to potential personal injury hazards. Obey all safety messages and instructions that follow this symbol to avoid possible injury or death.

DANGER, WARNING, CAUTION

Depending on the hazard level the signal words DANGER, WARNING or CAUTION are used to highlight safety instructions and warning messages. These messages may also include a warning relating to property damage.

DANGER
Danger statements indicate a hazardous situation which, if not avoided, will result in death or serious injury.

WARNING.
Warning statements indicate a hazardous situation that, if not avoided, could result in death or serious injury.

CAUTION
Caution statements indicate a hazardous situation that, if not avoided, could result in minor or moderate injury.

NOTICE

Notice statements are used to notify people on hazards that could result in things other than personal injury, like property damage.

NOTICE
This NOTICE statement indicates that the device contains components sensitive to electrostatic discharge.

NOTICE
This NOTICE statement contains the general mandatory sign and gives information that must be heeded and complied with for a safe use.

INFORMATION

INFORMATION
Notes to point out something important or useful.

Safety Instructions

- When working with the XMC-CPU/Zulu follow the instructions below and read the manual carefully to protect yourself from injury and the XMC-CPU/Zulu from damage.
- The device is a built-in component. It is essential to ensure that the device is mounted in a way that cannot lead to endangering or injury of persons or damage to objects.
- Do not use damaged or defective cables to connect the XMC-CPU/Zulu ".
- In case of damages to the device, which might affect safety, appropriate and immediate measures must be taken, that exclude an endangerment of persons and domestic animals and property.
- Current circuits which are connected to the device have to be sufficiently protected against hazardous voltage (SELV according to EN 60950-1).
- The XMC-CPU/Zulu may only be driven by power supply current circuits, that are contact protected. A power supply, that provides a safety extra-low voltage (SELV) according to EN 60950-1, complies with these conditions.

- The device has to be securely installed in the control cabinet before commissioning.
- Protect the XMC-CPU/Zulu from dust, moisture and steam.
- Protect the XMC-CPU/Zulu from shocks and vibrations.
- The XMC-CPU/Zulu may become warm during normal use. Always allow adequate ventilation around the XMC-CPU/Zulu and use care when handling.
- Do not operate the XMC-CPU/Zulu adjacent to heat sources and do not expose it to unnecessary thermal radiation. Ensure an ambient temperature as specified in the technical data.

DANGER

Hazardous Voltage - Risk of electric shock due to unintentional contact with uninsulated live parts with high voltages inside of the system into which the XMC-CPU/Zulu is to be integrated.

→ All current circuits which are connected to the device have to be sufficiently protected against hazardous voltage (SELV according to EN 60950-1) before you start with the installation.

→ Ensure the absence of voltage before starting any electrical work

NOTICE

Electrostatic discharges may cause damage to electronic components.

→ To avoid this, discharge the static electricity from your body before you touch the XMC-CPU/Zulu.

→ Furthermore, you should prevent your clothes from touching the XMC-CPU/Zulu, because your clothes might be electrostatically charged as well.

Qualified Personnel

This documentation is directed exclusively towards personnel qualified in control and automation engineering. The installation and commissioning of the product may only be carried out by qualified personnel, which is authorized to put devices, systems, and electric circuits into operation according to the applicable national standards of safety engineering.

Conformity

The XMC-CPU/Zulu is an industrial product and meets the demands of the EU regulations and EMC standards printed in the conformity declaration at the end of this manual.

Warning: In a residential, commercial or light industrial environment the XMC-CPU/Zulu may cause radio interferences in which case the user may be required to take adequate measures.

The XMC-CPU/Zulu is a sub-assembly intended for incorporation into an. The manufacturer of the final system must decide whether additional EMC or EMI protection requirements are necessary.

Data Safety

This device is equipped with an Ethernet or other interface which is suitable to establish a connection to data networks. Depending on the software used on the device, these interfaces may allow attackers to compromise normal function, get illegal access or cause damage.
esd does not take responsibility for any damage caused by the device if operated at any networks. It is the responsibility of the device's user to take care that necessary safety precautions for the device's network interface are in place.

Intended Use

The intended use of the XMC-CPU/Zulu is the operation as XMC Zynq MPSoC device with FPGA.
The guarantee given by esd does not cover damages which result from improper use, usage not in accordance with regulations or disregard of safety instructions and warnings.

- The XMC-CPU/Zulu is intended for installation on a base board according to Vita 42.3 standard.
- The operation of the XMC-CPU/Zulu in hazardous areas, or areas exposed to potentially explosive materials is not permitted.
- The operation of the XMC-CPU/Zulu for medical purposes is prohibited.

Service Note

The XMC-CPU/Zulu does not contain any parts that require maintenance by the user. The XMC-CPU/Zulu does not require any manual configuration of the hardware. Unauthorized intervention in the device voids warranty claims

Disposal

Products marked with a crossed-out dustbin must not be disposed of with household waste. Devices which have become defective in the long run must be disposed in an appropriate way or must be returned to the manufacturer for proper disposal. Please, contribute to environmental protection.

Typographical Conventions

Throughout this manual the following typographical conventions are used to distinguish technical terms.

Convention	Example
File and path names	**`/dev/null`** or **`<stdio.h>`**
Function names	***open()***
Programming constants	`NULL`
Programming data types	`uint32_t`
Variable names	*Count*

Number Representation

All numbers in this document are base 10 unless designated otherwise. Hexadecimal numbers have a prefix of 0x, and binary numbers have a prefix of 0b. For example, 42 is represented as 0x2A in hexadecimal and 0b101010 in binary.

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1 Overview

1.1 Description of XMC-CPU/Zulu

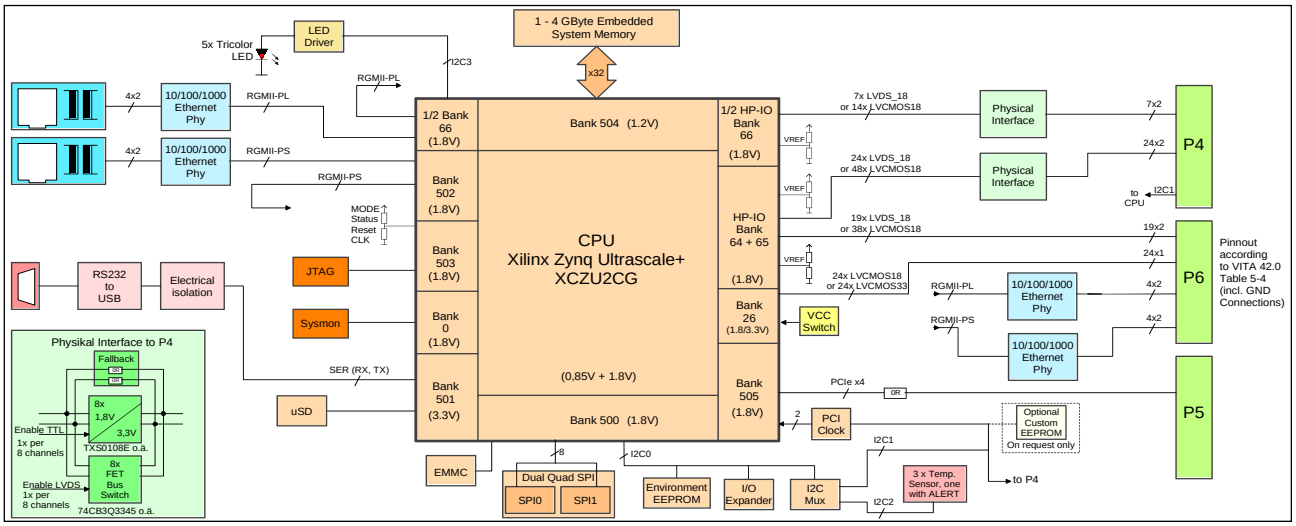


Figure 1: Block circuit diagram

64-Bit XMC ARM® Host CPU
The XMC-CPU/Zulu in XMC form factor comes with a XILINX® Zynq® UltraScale+™ CG multiprocessor system-on-chip with 1.3 GHz core frequency.
The local memory bus has a bus width of 32 bits and an overall capacity of 1 Gbyte.
64 Mbyte SPI Flash for boot loader and 128 Kbit I²C EEPROM for U-Boot environment.
XMC-CPU/Zulu features a 16-Gbyte eMMC™ memory which is used for operating system, file system and application software.

The XMC interface comes with quad-lane PCIe® bus and is designed according to VITA™ 42.3.

Two Gigabit Ethernet interfaces are accessible via the front panel of the XMC-CPU/Zulu. This gives an excellent base for EtherCAT® applications.
Two additional rear IO Ethernet interfaces are accessible via the XMC connector P6. The rear IO Ethernet interfaces come without electrical isolation.
Two of the GB Ethernet interfaces (one front, one rear) are routed through the FPGA. Therefore, special Ethernet IP-cores can be implemented.

A serial interface, designed as terminal interface, is accessible via an USB Mini type-B connector on the front.

The Flash memory carries the standard boot program “Das U-Boot” and enables the XMC-CPU/Zulu to boot various operating systems from on-board Flash, network or eMMC.
Board support packages are available for Linux® and VxWorks®. The BSPs include an example source code for the FPGA. Programming of the FPGA is done via XILINX Toolchain.

The esd EtherCAT Master Stack is available for various operating systems.

Customized options are available for customized series production in reasonable quantities.
Please contact our sales team for detailed information.
For example:

- CAN
  esd offers standard PIM modules for CAN signals.
  Furthermore, a CAN IP-core (CAN esdACC), which is configurable (number of CAN nodes, routing FPGA ↔ P4), is available for the on-board FPGA on request.

- IRIG-B
  An IRIG-B IP Core by esd electronics can be implemented in the FPGA.
  The physical interface of IRIG-B has to be provided externally via a PIM module.
  An esd PIM module is available on request.

- Other CPU Types
  Furthermore, other CPU-types (ZU2EG, ZU3CG and ZU3EG) are applicable.

- Extended Temperature Range
  The temperature range can be extended to -40 °C up to 75 °C.

- PMC
  PMC according to IEEE Std. 1386-2001 instead of XMC interface via connectors P1 and P2.
  The PCI bus conforms to PCI Local Bus Specification 3.0, 32-bit 33/66 MHz, 3.3 V (5 V tolerant), PCI bus master capability. The PMC interface supports 32-bit / 66 MHz PCI bus according to PCI Local Bus Specification 3.0.

- Ethernet
  The rear IO Ethernet signals are connected via P6. To connect standard Ethernet cabling an esd PIM module is available on request. The PIM module comes with an RJ45 connector and the Ethernet transformers on-board.

- RTC
  An additional RTC can be equipped.
  A backup battery can be connected via P4 and P6.

- Software
  Please contact our Sales-Team for board support packages for other real-time operating systems (e.g. QNX).

1.2 Glossary

Abbreviations

Abbreviation	Term
API	Application Programming Interface
CAN	Controller Area Network
CPU	Central Processing Unit
CiA	CAN in Automation
FPGA	Field Programmable Gate Array
FSBL	First Stage Bootloader
HW	Hardware
I/O	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
n.a.	not applicable
OS	Operating System
PS	Processing System (APUs + Memory + Ethernet etc.)
PL	Programmable Logic (FPGA)
RTC	Real Time Clock
SDK	Software Development Kit
VIVADO	Xilinx development tool for the programming of FPGAs

2 PCB View with Connectors

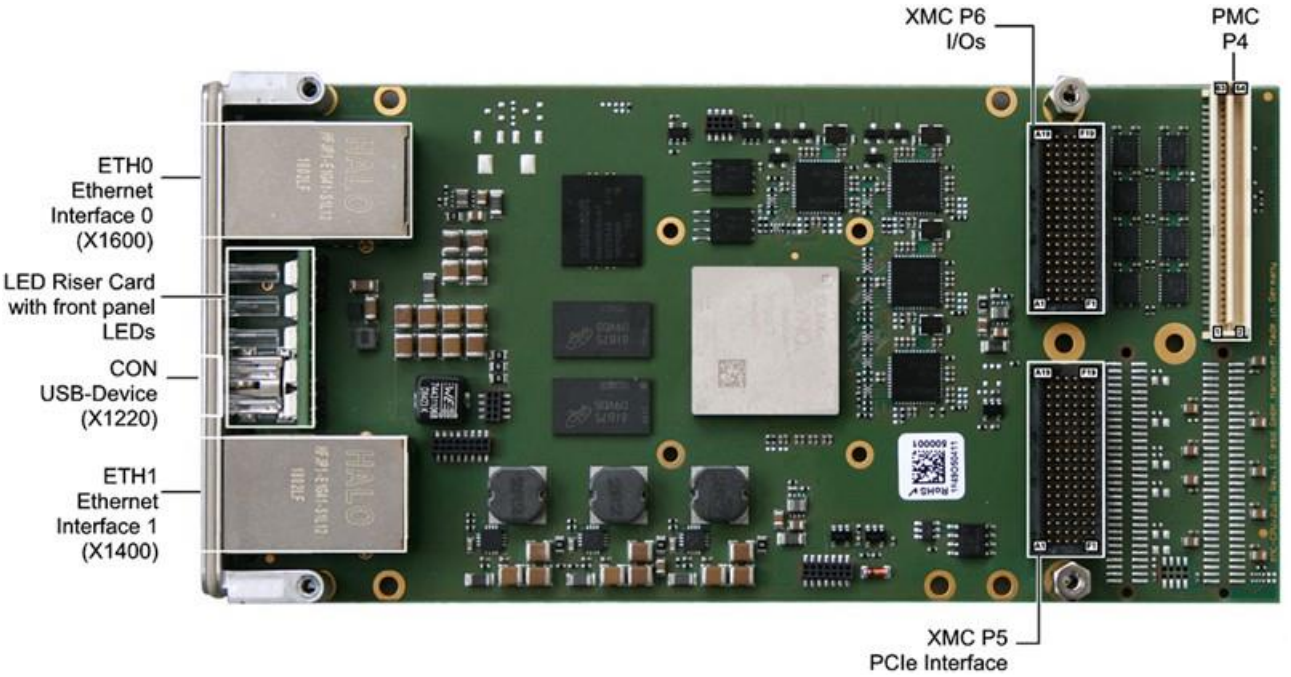


Figure 2: PCB top view

The Debug interface (X800) must be connected from the bottom side of the XMC-CPU/Zulu, see Figure 3.

PCB Bottom Layer

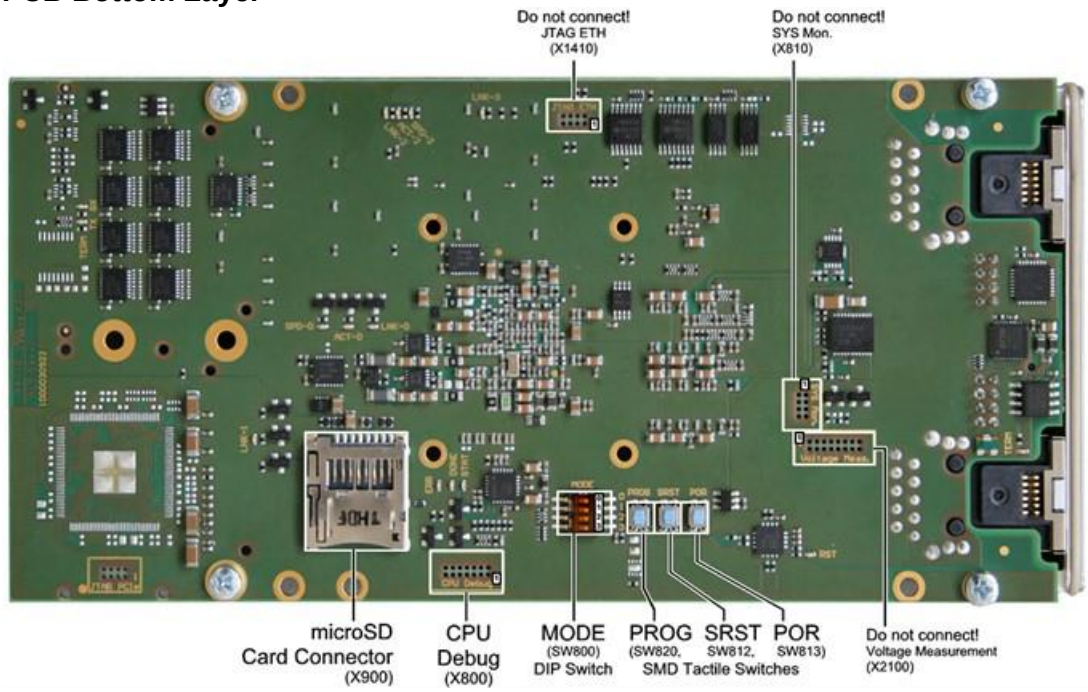


Figure 3: PCB bottom view

NOTICE
Read chapter “Hardware Installation” on page 19, before you start with the installation of the hardware!

See also from page 29 for signal assignment of the CAN connectors.
For a description of the DIP switch and the SMD tactile switches see page 17.

The LEDs are described in chapter “LEDs ” page 14.

3 LEDs

3.1 Position of the LEDs

3.1.1 Position

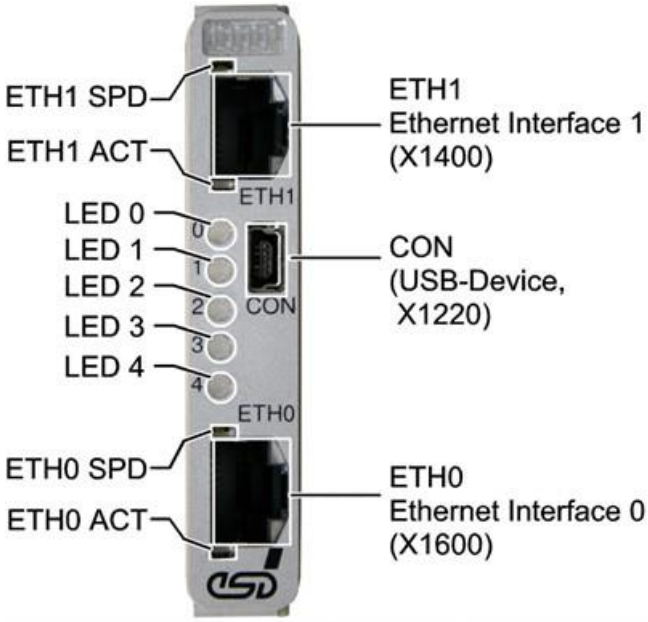


Figure 4: Connectors and LEDs

3.1.2 Indication of Ethernet LEDs ETH0, ETH1

The Activity and Link/Speed LEDs are integrated in the RJ45 sockets of ETH0 and ETH1 and display the status of the corresponding ETH channel.

LED	Colour	Function	Indicator State	Description
SPD	yellow	Speed	ON	Ethernet bit rate: 1000 Mbit/s
ACT	green	Activity	flashing	Ethernet activity (reception and transmission of Ethernet data)

Table 1: Description of LEDs

3.1.3 Indication of the Tricolour LEDs 0-4

Five tricolour LEDs are equipped in the front panel.

LED	Colour	Description
LEDX	green	User-defined via I²C bus and driver
	red	
	blue	

(X = 0-4)

Table 2: Description of LEDs 0-4

3.2 LEDs on PCB

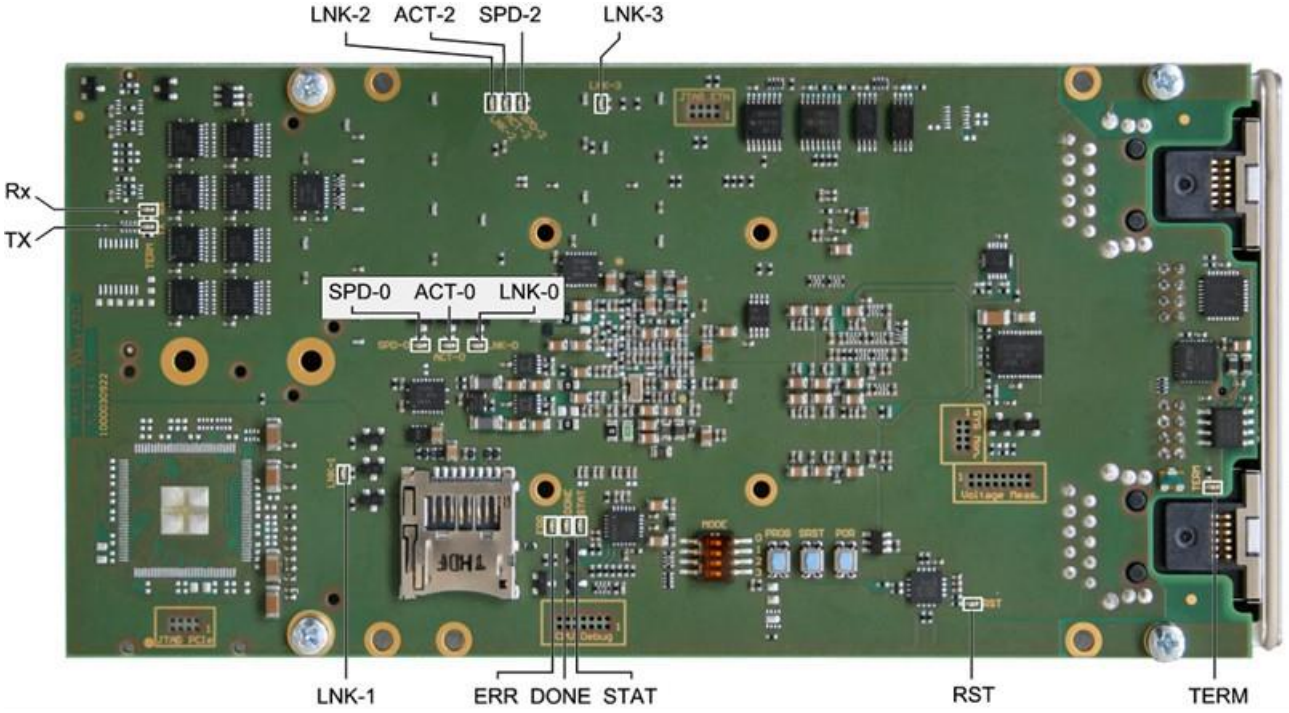


Figure 5: Connectors and LEDs

3.2.1 Ethernet LEDs

The 8 green LEDs (Speed, Activity and Link) are equipped on the bottom side of the XMC-CPU/Zulu see Figure 5.

Zynq Section	LED Name on PCB	Function	Display	Meaning LED on	LED name in schematic diagram
PL-GEM (U600 M) routed to **PS-GEM0**	-	Speed	-	integrated in RJ45 socket in the front panel, see chapter 3.1.2, page 14	in X1600
	-	Activity	-		in X1600
	LNK-3	Link	on	Ethernet link established	LED1622
PL-GEM (U600L) routed to **PS-GEM1**	**SPD-2**	Speed	on	Ethernet bit rate: 1000 Mbit/s	LED1521
	ACT-2	Activity	flashing	Ethernet activity - (reception and transmission of Ethernet data)	LED1520
	LNK-2	Link	on	Ethernet link established	LED1522
PS-GEM2 (U600H)	**SPD-0**	Speed	on	Ethernet bit rate: 1000 Mbit/s	LED1321
	ACT-0	Activity	flashing	Ethernet activity- (reception and transmission of Ethernet data)	LED1320
	LNK-0	Link	on	Ethernet link established	LED1322
PS-GEM3 (U600F)	**-**	Speed	-	integrated in RJ45 socket in the front panel, see chapter3.1.2, page 14	in X1400
	-	Activity	-		in X1400
	LNK-1	Link	on	Ethernet link established	LED1422

Table 3: Ethernet LEDs on the PCB

3.2.2 Other LEDs

The LEDs are equipped on the rear side of the XMC-CPU/Zulu, see Figure 5.

	LED	Colour	Function	Display	Description (LED on)	LED name in schematic diagram
CON port LEDs	**TX**	green	SER0_Tx	flashing	Transmitting data of serial interface via USB port CON	LED410
	RX	green	SER0_RX	flashing	Receiving data of serial interface via USB port CON	LED411
	TERM	green	Terminal	flashing	Traffic on serial interface via USB port CON (TERM)	LED1222
FPGA LEDs	**DONE**	green	Done	on	PL configuration done	LED820
	ERR	red	Err Out	on	Accidental power loss, hardware error or PMU failure.	LED821
	STAT	green	ERR_Stat	on	Platform Management Unit (PMU) dependent information	LED822
System	**RST**	red	Reset	on	Card reset active	LED810

Table 4: LEDs CON, Activity and USB PWR

4 Hardware Configuration

4.1 Coding Switch and Reset Buttons

The DIP-switch MODE and the 3 SMD tactile switches PROG, SRST and POR are equipped on the bottom layer of the XMC-CPU/Zulu. See Figure 3 on page 12 for the position on the PCB.

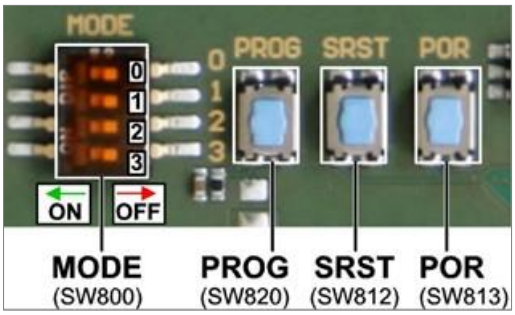


Figure 6: Position of the switches (detail)

4.1.1 Mode

The DIP-switch MODE (PS_MODE) comes with 4 Mode pins. With the DIP-switch the boot mode can be selected. Depending on the setting of the switches the BootROM boots the system from Quad-SPI (24b or 32b), SD or eMMC external boot devices.

Coding Switch	Pin	Description		Default on delivery
MODE (SW800)	0	PS_MODE0	The boot mode can be selected according to table 11-1 of the Technical Reference Manual of the Zynq UltraScale+ Device [1]	0
	1	PS_MODE1		1
	2	PS_MODE2		0
	3	PS_MODE3		0

Table 5: MODE switch

The PS_MODE switches (0-3) can be set to ON (logical value = 0) or OFF (logical value = 1). The values of all switches in the package are interpreted as one number, as read from switch 3 to 0. The following table shows the positions of the switches that must be configured for the different boot modes.

Boot Mode	Mode Pins [3:0]	Switch Position of Mode Pin				Description
		3	2	1	0	
Quad-SPI (24b)	0001	ON	ON	ON	OFF	24-bit addressing
Quad-SPI (32b)	**0010**	**ON**	**ON**	**OFF**	**ON**	**32-bit addressing** (Default on delivery)
SD0 (2.0)	0101	ON	OFF	ON	OFF	SD 2.0
eMMC (1.8V)	0110	ON	OFF	OFF	ON	eMMC version 4.5 at 1.8V

Table 6: MODE switch configuration

Please note, that the numbering of the mode pins is indicated on the PCB as shown in Figure 6! Ignore the numbers on the DIP switch housing.

4.1.2 PROG, SRST, POR

The XMC-CPU/Zulu comes with the 3 reset buttons (SMD tactile switches): PROG, SRST and POR, see Figure 6, page 17. For further information about the reset signals see Technical Reference Manual of the Zynq UltraScale+ Device [1].

Reset Button	Pin	Direction	Description
PROG (SW820)	PS_PROG_B	I/O	PL configuration reset signal
SRST (SW812)	PS_SRST_B	Input	System reset commonly used during debug
POR (SW813)	PS_POR_B	Input	Power-on reset signal

Table 7: Reset signals

5 Hardware Installation

NOTICE
Read the safety instructions at the beginning of this document carefully before you start with the hardware installation!

WARNING
Hazardous Voltage - Risk of electric shock due to unintentional contact with uninsulated live parts with high voltages inside of the system into which the XMC-CPU/Zulu is to be integrated.

→ Disconnect all hazardous voltages (mains voltage) before opening the system. Never carry out work while power supply voltage is switched on!
→ Ensure the absence of voltage before starting any electrical work.

NOTICE
Electrostatic discharges may cause damage to electronic components.

→ To avoid this, please discharge the static electricity from your body *before* you touch the XMC-CPU/Zulu.
→ Furthermore, you should prevent your clothes from touching the XMC-CPU/Zulu, because your clothes might be electrostatically charged as well.

Procedure:

1. Switch off your system and all connected peripheral devices (monitor, printer, etc.).
2. Discharge your body as described above.
3. Disconnect the system from the mains.
   Make sure that no risk arises from the system into which the XMC-CPU/Zulu shall be inserted.

   WARNING
   Hazardous Voltage
   Risk of electric shock due to unintentional contact with uninsulated live parts with high voltages.

   → Disconnect all hazardous voltages (mains voltage) before opening the system.
   → If the system does not have a flexible mains cable, but is directly connected to mains, disconnect the power supply via the safety fuse and make sure that the fuse cannot switch on again unintentionally (e.g. with caution label).
   → Ensure the absence of voltage before starting any electrical work.
   → Cover or block off adjacent live parts.

4. Open the case if necessary.
5. For sufficient EMC shielding the XMC-CPU/Zulu shall make contact to the system's enclosure nearly completely around its front panel. For this purpose, a conductive O-ring is contained in the product package of the XMC-CPU/Zulu module. Mount the conductive O-ring on the front panel of the XMC-CPU/Zulu. Additionally, or instead of it use shielding material as for example conductive shielding gasket.
6. Make sure that the XMC-CPU/Zulu is configured according to your needs:
   - For the configuration of the hardware see chapter “Coding Switch and Reset Buttons” on page 17.

7. Remove your carrier board (if already installed) and plug the XMC-CPU/Zulu carefully on the carrier board. Pay attention that the XMC-CPU/Zulu is correctly installed on the carrier board.

NOTICE
Please note that the number of mating cycles of the XMC connectors P5 and P6 is only 10! Do not uninstall the XMC-CPU/Zulu from the carrier board if it is not absolutely necessary!

Fix the XMC-CPU/Zulu with the screws on the carrier board. Use the four M 2.5 x 5 mm screws which are contained in the product package of the module.

8. Install the carrier board in your system.
9. Connect the Ethernet and the CON interface via the connectors in the front panel of the XMC-CPU/Zulu.
10. Close the system's case again (if applicable).
11. Connect the system to mains again (mains connector or safety fuse).
12. Switch on the system and the peripheral devices.
13. End of hardware installation.
14. Set the interface properties in your operating system. Refer to the documentation of the operating system.

6 Technical Data

6.1 General Technical Data

Power supply voltage	Nominal voltage:	3.3 V / $I_{3.3V\_MAX}$ = 640 mA, $I_{3.3V\_TYPICAL}$ = 610 mA VPWR: 5V / I_{5V_MAX} = 830 mA, $I_{5V\_TYPICAL}$ = 720 mA or 12V / I_{12V_MAX} = 400 mA, $I_{12V\_TYPICAL}$ = 340 mA Absolute maximum power: $P_{3.3V+5V\_MAX}$ = 10 W
Power consumption	Typical: < 10 W (Linux Idle) Maximum: 10 W (Linux Memtest)	
Temperature range	Operation: 0 °C ... + 55 °C ambient temperature Storage: -40 °C ... + 85 °C Transport: -40 °C ... + 85 °C	
Humidity	Max. 90%, non-condensing	
Connector	ETH0 ETH1	RJ45 socket (X1600, mating cycles: 1000) - Ethernet Port 0 RJ45 socket (X1400, mating cycles: 1000) - Ethernet Port 1
	CON	Mini USB socket type-B (X1220, MUSB-05-S-B-SM-A, Mating cycles: 1500) - Console (USB-Device)
	PMC P4 XMC P5 XMC P6	64-pin PMC connector (P4, mating cycles: 100) - PMC IO XMC connector (Samtec ASP-103614-04, mating cycles: 10) - PCI Express interface, XMC connector (Samtec ASP-103614-04, mating cycles: 10) - e.g.: 73 LVTTL or 34 LVDS I/Os
	Only for test- and programming purposes:	
	CPU Debug	Samtec: CLM107-02-F-D-BE (pass-thru micro socket, X800), - JTAG interface CPU
	Connectors for factory use only:	
	SYS Mon.	Samtec: CLM104-02-F-D-BE (pass-thru micro socket, X810), - SYSMON
	JTAG ETH	Samtec: CLM104-02-F-D-BE (pass-thru micro socket, X1410), - JTAG interface Ethernet
	Voltage Meas.	Samtec: CLM108-02-F-D-BE (pass-thru micro socket, X2100), - Voltage measurement
Form factor / Dimensions	149 mm x 74 mm x 10 mm (without front panel)	
Weight	Ca. 120 g (without heat sink)	

Table 8: General Data of the module

6.2 CPU Kernel

Architecture	Dual Core A53 Application Processor Unit (APU) + Dual Core Real-time Processor Unit.
CPU	XILINX Zynq UltraScale+ CG XCZU2CG-1SFVA625E – 2x APU, 2x RPU
Clock rate	1.3 GHz APU, 533 MHz RPU
Programmable Logics	Internal FPGA resources: 103K System Logic Cells, 94K CLB Flip Flops, 47K CLB LUTs
RAM	Organisation: 2 devices each 16 bit, no ECC Series: 2Gbyte – 2x MT40A512M16
Flash memory (NOR)	Organisation: 2 devices with Quad SPI Interface (Dual Quad SPI) 64Mbyte – 2x MT25QU256ABA1EW7-0SIT 100 000 read / write cycles, > 20 years data retention
Flash memory (NAND)	16 Gbyte eMMC memory e.g.: Swissbit (SFEM4096B1EA1TO-I-GE-111-E02)
EEPROM	1 x 128 Kbit for U-Boot Environment Via I²C in Fast (400kHz) Mode 1 000 000 read / write cycles, >20 years data retention

Table 9: CPU Kernel

6.3 Ethernet Interface PS

Number of Ethernet interfaces	2
Standard	IEEE 802.3, 10BASE-T, 100BASE-TX, 1000BASE-T
Bit rate	10/100/1000 Mbit/s
Controller	Integrated in the PS (Processing System) section of the CPU
Connection	Twisted Pair (compatible with IEEE 802.3), 1000BASE-T,
Electrical isolation	1x via transformer integrated in the RJ45 socket Electrical strength 1500V AC / 60sec 1 x without electrical isolation
Connector	1x RJ45 socket in the front panel with integrated LEDs (Link- and Activity) and integrated transformer 1x via P6
Topology	The interface PS-GEM3 of the controller integrated in the CPU is connected to the front panel as ETH1, interface PS-GEM2 is connected to connector P6. A common MDIO interface is used for all interfaces (PS and PL).
PTP	It is possible to synchronise the device time by means of the IEEE1588 conformant PTP protocol via this Ethernet interface.

Table 10: Data of the Ethernet interface PS

6.4 Ethernet Interface PL

Number of Ethernet interfaces	2
Standard	IEEE 802.3, 10BASE-T, 100BASE-TX, 1000BASE-T
Bit rate	10/100/1000 Mbit/s
Controller	Integrated in the PS section and routed via the PL (Programmable Logic) section of the CPU or embedded as IP core in the PL section of the CPU
Connection	Twisted Pair (compatible with IEEE 802.3), 1000BASE-T,
Electrical isolation	1x via transformer integrated in the RJ45 socket Electrical strength 1500V AC / 60sec 1 x without electrical isolation
Connector	1x RJ45 socket in the front panel with integrated LEDs (Link- and Activity) and integrated transformer 1x via P6
Topology	The CPU integrated controllers are used instead of using the IP core as controller, thus the interface PS-GEM0 is connected to the front panel as ETH0, interface PS-GEM1 is connected to connector P6. A common MDIO interface is used for all interfaces (PS and PL).
PTP	It is possible to synchronise the device time by means of the IEEE1588 conformant PTP protocol via this Ethernet interface.

Table 11: Data of the Ethernet interface PL

6.5 USB Console Port (CON)

Number	1 asynchronous serial interface, used as terminal interface
Controller	Integrated in CPU
Bit rate	Value range: 9600 Baud ... 115200 Baud Default setting: 115200 Baud, 8 Bit, No Parity 1 Stop-Bit
Physical Interface	UART serial console transformed to USB 1.1 via USB to serial converter
Software	Standard operating-system driver
Connector	MiniUSB Type-B

Table 12: Data of the USB console port

6.6 PCIe Interfaces

Number	1
Controller	Integrated in the PS section of the CPU
Standard	VITA 42.0 Notice: The CPU can support PCIe 2.0. If the usage of PCIe 2.0 via the VITA 42 connectors should cause problems, it is possible to limit the usage to PCIe 1.1 via software.
Lanes	4
Mode	Endpoint or Root Complex (defined by the base board via XMC pin DP19+ on XMC_J15)
Software support	As Root Complex: Standard operating system drivers As Endpoint: Access to a shared memory section
Connector	P5

Table 13: Data of the PCIe interface

6.7 Digital Inputs/Outputs P4

Number	Maximum 62, see chapter “PMC P4 I/O Connector” page 31 for assignment
IO Configuration	Single ended or differential inputs or outputs, depending on FPGA pin configuration. Routed as differential pair in the layout
Physical interface	1.8V to 3.3V level shifters or FET switches for LVDS signals can be alternatively enabled via FPGA by groups of 8 pins. Connections are visible on page 31. On request only: 0 Ohm resistors as fallback,
Input switching threshold	3,3V LVTTL, not 5V tolerant or 1,8V LVDS according to XILINX data sheet
Bandwidth	3,3V LVTTL: max. 60 Mbps 1,8 LVDS: max. 500MHz bandwidth
Electrical isolation	None
Protective circuit	None
Connector	P4

Table 14: Data of the Digital I/Os on P4

6.8 Digital Inputs/Outputs P6

Number	Maximum 62, see chapter “XMC – P6 I/O Connector” page 34 for assignment
IO Configuration	Single ended or differential inputs or outputs, depending on FPGA pin configuration. Routed as differential pair in the layout
Physical interface	FPGA directly connected to P6
Input switching threshold	1.8V LVTTL, not tolerant for 2.5V / 3.3V or 5V or 1.8V LVDS according to XILINX data sheet
Bandwidth	According to XILINX data sheet
Electrical isolation	None
Protective circuit	None
Connector	P6

Table 15: Data of the Digital I/Os on P6

6.9 Control Elements

Buttons	3 SMD tactile switches for the signals SRST, PROG and POR (Power On Reset) are equipped on the bottom layer of the XMC-CPU/Zulu (see Figure 6 page 17).
Switch	4-bit DIP-switch MODE for the configuration of the boot modes. (Together with the SD-card slot for initial system start-up). The DIP switch is equipped on the bottom layer of the XMC-CPU/Zulu see Figure 6 page 17).

Table 16: Data of the control elements and display elements

6.10 Health

Voltage	Internal voltages of the PS and PL sections via the CPU internal SYSMON Unit (see XILINX data sheet)
Temperature	3 CPU internal sensors of the SYSMON unit (see XILINX data sheet) + 3 external I²C temperature sensors, one with alert output ports. The 3 external I²C sensors are connected to the I²C bus 2: One TMP100 each at I²C address 0x4a and 0x4b One ADT7461 at address 0x4c. This has one internal temperature sensor and a connection to the CPU diode for CPU-DIE temperature measurement.
XMC-IPMI support	Not supported
Digital IO extension	For sideband signals of the PMC/XMC bus as e.g.: Root, Monarch, Wake, Reset, ... Connected via an I²C IO expander respectively direct to the FPGA Pins
Power Management	Voltage regulator and clock distribution component are connected to the CPU via I²C. It is possible to request or set various characteristic values
Board Type	Board revision and variant can be requested via FPGA IO pins and external resistors

Table 17: Health unit

6.11 Mass Storage

Number	1
Standard	eMMC specification 4.51
Topology	Directly connected to the CPU
Controller	Integrated in the PS section of the CPU
Capacity	16 Gbyte maximum capacity
Data rate	HS200 mode (theoretically 1660 Mbyte/s)

Table 18: Data of the mass storage unit

6.12 MicroSD Card Slot

Number	1
Standard	Compatible with the SD Host Controller Specification revision 3.0 (SDHC)
Topology	Directly connected to the CPU
Controller	Integrated into the PS section of the CPU
Data rate	SDR104 mode (theoretically 800Mbyte/s)
Supported media	The usability of individual media (manufacturer, type, size) depends on the technology used and cannot be granted.
Functionality	This slot is intended for the initial start-up only (Bare Metal bring up)

Table 19: Data of the MicroSD card slot

6.13 Front Panel LEDs

Device	Texas TLC59116
Connection	Via I²C to PL: I²C SCL on pin G6, I²C SDA on Pin H6, Reset on Pin D8
I²C address	0x60
LED colour	Each tricolour LED has its separate three inputs from the TCL59116. The first connection is wired to the green LED, the second one to the red LED and the third to the blue LED.

Table 20: Front panel LEDs

6.14 PCI Clock Generator

Device	IDT 5P49V5935B
Connection	Control via I²C 1 Clock output 1...3 can be used for PCIe Clock input to CPU PS if operating in ROOT Complex mode. Output 4 is connected to PL (E6 CLK_P, E5 CLK_N) and can be used for user application.
I²C address	0x6A
Configuration	Please contact our support team (support@esd.eu) if you want to use the external clock feature.

Table 21: PCI Clock generator

6.15 Optional Interfaces

6.15.1 CAN Interfaces

Number of CAN interfaces	2
Topology	Parallel connection of RX and TX signals to the PS pins and to the PL pins.
CAN controller	Acc. to ISO 11898-1 Configurable per software from PS or as esdACC IP-core integrated in the FPGA section
CAN protocol	According to ISO 11898-1
Physical Layer	External
Electrical isolation	None / If required the CAN interfaces have to be electrically isolated externally
Bus termination	A terminating resistor has to be set externally, if required
Connector	Via P4

Table 22: Data of the optional CAN interfaces

6.15.2 PMC Interface

Number	1
Controller	Pericom PI7C9X111SLBFDE PCIe to PCI Bridge
Standard	IEEE1386 (PCI 3.0)
Version	32 Bit, 33/66MHz, 3.3V, 5V tolerant
Mode	Monarch or Non-Monarch (defined by the base board via pin)
Software support	As Monarch: Standard operating system driver As Non-Monarch: Access to a Shared Memory section
Connector	P1 and P2

Table 23: Data of the optional PMC interface

7 Connector Assignments

7.1 PMC/XMC Connectors

7.1.1 PMC P1 Connector

Pin	Signal	Signal	Pin
1	TCK	-12V	2
3	GND	INTA#	4
5	INTB#	INTC#	6
7	GND (PRESENT#)	+5V	8
9	INTD#	n.c. (reserved)	10
11	GND	n.c. (reserved)	12
13	PCI-CLK	GND	14
15	GND	GNT#	16
17	REQ#	+5V	18
19	VIO	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	GND	24
25	GND	C/BE3#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	VIO	AD[17]	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	DEVSEL#	+5V	38
39	GND	n.c. (LOCK#)	40
41	n.c. (SDONE#)	n.c. (SBO)	42
43	PAR	GND	44
45	VIO	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	GND	C/BE0#	52
53	AD[06]	AD[05]	54
55	AD[04]	GND	56
57	VIO	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	GND	n.c. (REQ64#)	64

7.1.2 PMC P2 Connector

Pin	Signal	Signal	Pin
1	+12V	TRST#	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	n.c. (reserved)	8
9	n.c. (reserved)	n.c. (reserved)	10
11	MODE2#	+3.3V	12
13	PCI-RST#	MODE3#	14
15	+3.3V	MODE4#	16
17	n.c. (PME#)	GND	18
19	AD[30]	AD[29]	20
21	GND	AD[26]	22
23	AD[24]	+3.3V	24
25	IDSEL	AD[23]	26
27	+3.3V	AD[20]	28
29	AD[18]	GND	30
31	AD[16]	C/BE2#	32
33	GND	IDSELB	34
35	TRDY#	+3.3V	36
37	GND	STOP#	38
39	PERR#	GND	40
41	+3.3V	SERR#	42
43	C/BE1#	GND	44
45	AD[14]	AD[13]	46
47	M66EN	AD[10]	48
49	AD[08]	+3.3V	50
51	AD[07]	n.c. (REQB#)	52
53	+3.3V	GNTB#	54
55	n.c. (reserved)	GND	56
57	n.c. (reserved)	EREADY	58
59	GND	RESETOUT#	60
61	n.c. (ACK64#)	+3.3V	62
63	GND	MONARCH#	64

7.1.3 PMC P4 I/O Connector

Pin	Signal Name	Notes	Alternative Signal Name	Differential Pair (XILINX Name)	Notes
1	FPGA-IO<0>	IO, T/L0		IO_L20N_T3L_N3_AD1N_66	
2	FPGA-IO<1>	IO, T/L0		IO_L23N_T3U_N9_66	
3	FPGA-IO<2>	IO, T/L0		IO_L20P_T3L_N2_AD1P_66	
4	FPGA-IO<3>	IO, T/L0		IO_L23P_T3U_N8_66	
5	FPGA-IO<4>	IO, T/L0		IO_L21N_T3L_N5_AD8N_66	
6	FPGA-IO<5>	IO, T/L0		IO_L24N_T3U_N11_PERSTN0_65	
7	FPGA-IO<6>	IO, T/L0		IO_L21P_T3L_N4_AD8P_66	
8	FPGA-IO<7>	IO, T/L1		IO_L24P_T3U_N10_PERSTN1_I2C_S	
9	FPGA-IO<8>	IO, T/L1		IO_L21N_T3L_N5_AD8N_65	
10	FPGA-IO<9>	IO, T/L1		IO_L19N_T3L_N1_DBC_AD9N_65	
11	FPGA-IO<10>	IO, T/L1		IO_L21P_T3L_N4_AD8P_65	
12	FPGA-IO<11>	IO, T/L1		IO_L19P_T3L_N0_DBC_AD9P_65	
13	FPGA-IO<12>	IO, T/L1		IO_L12N_T1U_N11_GC_65	CLK Input
14	FPGA-IO<13>	IO, T/L1		IO_L22N_T3U_N7_DBC_AD0N_65	
15	FPGA-IO<14>	IO, T/L1		IO_L12P_T1U_N10_GC_65	CLK Input
16	FPGA-IO<15>	IO, T/L1		IO_L22P_T3U_N6_DBC_AD0P_65	
17	FPGA-IO<16>	IO, T/L2		IO_L22N_T3U_N7_DBC_AD0N_66	
18	FPGA-IO<17>	IO, T/L2		IO_L15N_T2L_N5_AD11N_66	
19	FPGA-IO<18>	IO, T/L2		IO_L22P_T3U_N6_DBC_AD0P_66	
20	FPGA-IO<19>	IO, T/L2		IO_L15P_T2L_N4_AD11P_66	
21	FPGA-IO<20>	IO, T/L2		IO_L24N_T3U_N11_66	
22	FPGA-IO<21>	IO, T/L2		IO_L10N_T1U_N7_QBC_AD4N_65	
23	FPGA-IO<22>	IO, T/L2		IO_L24P_T3U_N10_66	
24	FPGA-IO<23>	IO, T/L2		IO_L10P_T1U_N6_QBC_AD4P_65	
25	FPGA-IO<24>	IO, T/L3		IO_L19N_T3L_N1_DBC_AD9N_66	
26	FPGA-IO<25>	IO, T/L3		IO_L14N_T2L_N3_GC_65	CLK Input
27	FPGA-IO<26>	IO, T/L3		IO_L19P_T3L_N0_DBC_AD9P_66	
28	FPGA-IO<27>	IO, T/L3		IO_L14P_T2L_N2_GC_65	CLK Input
29	FPGA-IO<28>	IO, T/L3		IO_L11N_T1U_N9_GC_65	CLK Input
30	FPGA-IO<29>	IO, T/L3		IO_L13N_T2L_N1_GC_QBC_65	CLK Input
31	FPGA-IO<30>	IO, T/L3		IO_L11P_T1U_N8_GC_65	CLK Input
32	FPGA-IO<31>	IO, T/L3		IO_L13P_T2L_N0_GC_QBC_65	CLK Input

Notes:

1) Signals in the column "Notes" T/Lx refer to PL Outputs to enable TTL an LVDS switches. Please check the supplied sample FPGA for pin assignment.

Pin	Signal Name	Notes	Alternative Signal Name	Notes	Differential Pair (XILINX Name)	Notes
33	FPGA-IO<32>	IO, T/L4			IO_L6N_T0U_N11_AD6N_64	
34	FPGA-IO<33>	IO, T/L4	CAN0_TX	3.3V, O	IO_L17N_T2U_N9_AD10N_65	
35	FPGA-IO<34>	IO, T/L4			IO_L6P_T0U_N10_AD6P_64	
36	FPGA-IO<35>	IO, T/L4	CAN0_RX	5V, I	IO_L17P_T2U_N8_AD10P_65	
37	FPGA-IO<36>	IO, T/L4			IO_L12N_T1U_N11_GC_64	CLK Input
38	FPGA-IO<37>	IO, T/L4	CAN1_TX	3.3V, O	IO_L4N_T0U_N7_DBC_AD7N_64	
39	FPGA-IO<38>	IO, T/L4			IO_L12P_T1U_N10_GC_64	CLK Input
40	FPGA-IO<39>	IO, T/L5	CAN1_RX	5V, I	IO_L4P_T0U_N6_DBC_AD7P_64	
41	FPGA-IO<40>	IO, T/L5			IO_L9N_T1L_N5_AD12N_64	
42	FPGA-IO<41>	IO, T/L5	GND (when using CAN 0 or 1)	GND	IO_L11N_T1U_N9_GC_64	CLK Input
43	FPGA-IO<42>	IO, T/L5	GND (when using CAN 0 or 1)	GND	IO_L9P_T1L_N4_AD12P_64	
44	FPGA-IO<43>	IO, T/L5	TxS-0	RS232, O	IO_L11P_T1U_N8_GC_64	CLK Input
45	FPGA-IO<44>	IO, T/L5			IO_L7N_T1L_N1_QBC_AD13N_65	
46	FPGA-IO<45>	IO, T/L5	RxS-1	RS232, I	IO_L22N_T3U_N7_DBC_AD0N_64	
47	FPGA-IO<46>	IO, T/L5			IO_L7P_T1L_N0_QBC_AD13P_65	
48	FPGA-IO<47>	IO, T/L6	TxS-1	RS232, O	IO_L22P_T3U_N6_DBC_AD0P_64	
49	FPGA-IO<48>	IO, T/L6			IO_L16N_T2U_N7_QBC_AD3N_64	
50	FPGA-IO<49>	IO, T/L6	RxS-0	RS232, I	IO_L13N_T2L_N1_GC_QBC_64	CLK Input
51	FPGA-IO<50>	IO, T/L6			IO_L16P_T2U_N6_QBC_AD3P_64	
52	FPGA-IO<51>	IO, T/L6	GND (when using SER 1)	GND	IO_L13P_T2L_N0_GC_QBC_64	CLK Input
53	FPGA-IO<52>	IO, T/L6	CLOCK_IN	5V, I	IO_L14N_T2L_N3_GC_64	CLK Input
54	FPGA-IO<53>	IO, T/L6		3.3V, O	IO_L1N_T0L_N1_DBC_64	
55	FPGA-IO<54>	IO, T/L6	RESET_IN	5V, I	IO_L14P_T2L_N2_GC_64	CLK Input
56	FPGA-IO<55>	IO, T/L6		3.3V, O	IO_L1P_T0L_N0_DBC_64	
57	FPGA-IO<56>	IO, T/L7	IRIG-B_R_IN	5V, I	IO_L24N_T3U_N11_64	
58	FPGA-IO<57>	IO, T/L7		3.3V, O	IO_L15N_T2L_N5_AD11N_64	
59	FPGA-IO<58>	IO, T/L7			IO_L24P_T3U_N10_64	
60	FPGA-IO<59>	IO, T/L7		3.3V, O	IO_L15P_T2L_N4_AD11P_64	
61	FPGA-IO<60>	IO, T/L7			IO_L18N_T2U_N11_AD2N_64	
62	FPGA-IO<62>	IO, T/L7		3.3V, O	IO_L18P_T2U_N10_AD2P_64	
63	IIC-SDA	IO,I2C1 SDA	FPGA-IO<61>, T/L7		IO_L7N_T1L_N1_QBC_AD13N_64	
64	IIC-SCL	O, I2C1 SCL	FPGA-IO<63>, T/L7		IO_L7P_T1L_N0_QBC_AD13P_64	

Notes:

1) Signals in the column "Alternative Signal Name" are assembly options, which can be enabled via 0Ω resistors.
2) The functional assignment of the signals to the pins of the connector (LVDS_P, LVDS_N, CLK Inputs) equal the assignment of the XMC-CPU/2041 unit.

7.1.4 XMC - P5

Signal / PIN Row A		Signal / PIN Row B		Signal / PIN Row C		Signal / PIN Row D		Signal / PIN Row E		Signal / PIN Row F	
PCIe_Tx_L0p	1	PCIe_Tx_L0n	1	3.3V	1	PCIe_Tx_L1p	1	PCIe_Tx_L1n	1	unused	1
GND	2	GND	2	unused (JTAG_TRST#)	2	GND	2	GND	2	PCIe_RST_IN#	2
PCIe_Tx_L2p	3	PCIe_Tx_L2n	3	3.3V	3	PCIe_Tx_L3p	3	PCIe_Tx_L3n	3	unused	3
GND	4	GND	4	unused (JTAG_TCK)	4	GND	4	GND	4	unused	4
unused	5	unused	5	3.3V	5	unused	5	unused	5	unused	5
GND	6	GND	6	unused (JTAG_TMS)	6	GND	6	GND	6	unused	6
unused	7	unused	7	3.3V	7	unused	7	unused	7	unused	7
GND	8	GND	8	unused (JTAG_TDI)	8	GND	8	GND	8	unused	8
unused	9	unused	9	unused	9	unused	9	unused	9	unused	9
GND	10	GND	10	unused (JTAG_TDO)	10	GND	10	GND	10	unused (EEPROM_GA0)	10
PCIe_Rx_L0p	11	PCIe_Rx_L0n	11	Unused (FPGA-)BIST#	11	PCIe_Rx_L1p	11	PCIe_Rx_L1n	11	unused	11
GND	12	GND	12	unused (EEPROM_GA1)	12	GND	12	GND	12	GND	12
PCIe_Rx_L2p	13	PCIe_Rx_L2n	13	unused	13	PCIe_Rx_L3p	13	PCIe_Rx_L3n	13	unused	13
GND	14	GND	14	unused (EEPROM_GA2)	14	GND	14	GND	14	unused (EEPROM_SDA)	14
unused	15	unused	15	unused	15	unused	15	unused	15	unused	15
GND	16	GND	16	unused (EEPROM_WE)	16	GND	16	GND	16	unused (EEPROM_SCL)	16
unused	17	unused	17	unused	17	unused	17	unused	17	unused	17
GND	18	GND	18	unused	18	GND	18	GND	18	unused	18
REFCLK_0p	19	REFCLK_0n	19	unused	19	WAKE#	19	ROOT#	19	unused	19

The pin PCIe_RST_IN# is connected to the CPU POR# signal so that a reset on the PCI also rests the XMC-CPU/Zulu.

7.1.5 XMC – P6 I/O Connector

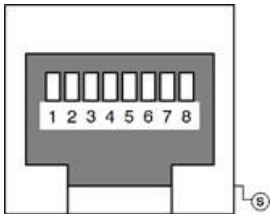
Signal / PIN Row A		Signal / PIN Row B		Signal / PIN Row C		Signal / PIN Row D		Signal / PIN Row E		Signal / PIN Row F	
ETH1-MDIO0_P	1	ETH1-MDIO0_N	1	ETH1-MDIO1_N	1	ETH1-MDIO2_P	1	ETH1-MDIO2_N	1	ETH1-MDIO3_N	1
GND	2	GND	2	ETH1-MDIO1_P	2	GND	2	GND	2	ETH1-MDIO3_P	2
ETH3-MDIO0_P	3	ETH3-MDIO0_N	3	ETH3-MDIO1_N	3	ETH3-MDIO2_P	3	ETH3-MDIO2_N	3	ETH3-MDIO3_N	3
GND	4	GND	4	ETH3-MDIO1_P	4	GND	4	GND	4	ETH3-MDIO3_P	4
FPGA-IO<102> IO_L3P_AD9P_26	5	FPGA-IO<100> IO_L3N_AD9N_26	5	FPGA-IO<132> IO_L9N_AD3N_26	5	FPGA-IO<103> IO_L2P_AD10P_26	5	FPGA-IO<101> IO_L2N_AD10N_26	5	FPGA-IO<133> IO_L12N_AD0N_26	5
GND	6	GND	6	FPGA-IO<134> IO_L9P_AD3P_26	6	GND	6	GND	6	FPGA-IO<135> IO_L12P_AD0P_26	6
FPGA-IO<106> IO_L4P_AD8P_26	7	FPGA-IO<104> IO_L4N_AD8N_26	7	FPGA-IO<136> IO_L11N_AD1N_26	7	FPGA-IO<107> IO_L5P_HDGC_AD7P_26	7	FPGA-IO<105> IO_L5N_HDGC_AD7N_26	7	FPGA-IO<137> IO_L10N_AD2N_26	7
GND	8	GND	8	FPGA-IO<138> IO_L11P_AD1P_26	8	GND	8	GND	8	FPGA-IO<139> IO_L10P_AD2P_26	8
FPGA-IO<110> IO_L6P_HDGC_AD6P_26	9	FPGA-IO<108> IO_L6N_HDGC_AD6N_26	9	FPGA-IO<140> IO_L7N_HDGC_AD5N_26	9	FPGA-IO<111> IO_L1P_AD11P_26	9	FPGA-IO<109> IO_L1N_AD11N_26	9	FPGA-IO<141> IO_L8N_HDGC_AD4N_26	9
GND	10	GND	10	FPGA-IO<142> IO_L7P_HDGC_AD5P_26	10	GND	10	GND	10	FPGA-IO<143> IO_L8P_HDGC_AD4P_26	10
FPGA-IO<114> IO_L15P_T2L_N4_AD11P_65	11	FPGA-IO<112> IO_L15N_T2L_N5_AD11N_65	11	FPGA-IO<144> IO_L9N_T1L_N5_AD12N_65	11	FPGA-IO<115> IO_L23P_T3U_N8_I2C_SCLK_65	11	FPGA-IO<113> IO_L23N_T3U_N9_65	11	FPGA-IO<145> IO_L8N_T1L_N3_AD5N_65	11
GND	12	GND	12	FPGA-IO<146> IO_L9P_T1L_N4_AD12P_65	12	GND	12	GND	12	FPGA-IO<147> IO_L8P_T1L_N2_AD5P_65	12
FPGA-IO<118> IO_L16P_T2U_N6_QBC_AD3P_65	13	FPGA-IO<116> IO_L16N_T2U_N7_QBC_AD3N_65	13	FPGA-IO<148> IO_L5N_T0U_N9_AD14N_65	13	FPGA-IO<119> IO_L18P_T2U_N10_AD2P_65	13	FPGA-IO<117> IO_L18N_T2U_N11_AD2N_65	13	FPGA-IO<149> IO_L6N_T0U_N11_AD6N_65	13
GND	14	GND	14	FPGA-IO<150> IO_L5P_T0U_N8_AD14P_65	14	GND	14	GND	14	FPGA-IO<151> IO_L6P_T0U_N10_AD6P_65	14
FPGA-IO<122> IO_L3P_T0L_N4_AD15P_65	15	FPGA-IO<120> IO_L3N_T0L_N5_AD15N_65	15	FPGA-IO<152> IO_L4N_T0U_N7_DBC_AD7N_65	15	FPGA-IO<123> IO_L2P_T0L_N2_65	15	FPGA-IO<121> IO_L2N_T0L_N3_65	15	FPGA-IO<153> IO_L20N_T3L_N3_AD1N_65	15
GND	16	GND	16	FPGA-IO<154> IO_L4P_T0U_N6_DBC_AD7P_SMBALE	16	GND	16	GND	16	FPGA-IO<155> IO_L20P_T3L_N2_AD1P_65	16
FPGA-IO<126> IO_L20P_T3L_N2_AD1P_64	17	FPGA-IO<124> IO_L20N_T3L_N3_AD1N_64	17	FPGA-IO<156> IO_L1N_T0L_N1_DBC_65	17	FPGA-IO<127> IO_L19P_T3L_N0_DBC_AD9P_64	17	FPGA-IO<125> IO_L19N_T3L_N1_DBC_AD9N_64	17	FPGA-IO<157> IO_L5N_T0U_N9_AD14N_64	17
GND	18	GND	18	FPGA-IO<158> IO_L1P_T0L_N0_DBC_65	18	GND	18	GND	18	FPGA-IO<159> IO_L5P_T0U_N8_AD14P_64	18
FPGA-IO<130> IO_L23P_T3U_N8_64	19	FPGA-IO<128> IO_L23N_T3U_N9_64	19	FPGA-IO<160> IO_L17N_T2U_N9_AD10N_64	19	FPGA-IO<131> IO_L21P_T3L_N4_AD8P_64	19	FPGA-IO<129> IO_L21N_T3L_N5_AD8N_64	19	FPGA-IO<161> IO_L17P_T2U_N8_AD10P_64	19

The signals marked with grey background can only be configured as pseudo differential inputs or single ended LVCMOS I/Os.
During runtime the I/O voltage of Bank 26 can be switched between 1.8V and 3.3V via an FPGA I/O pin. Per default the voltage is 1.8V.

7.2 Ethernet ETH0, ETH1

Device connector: RJ45 socket, 8-pin

Pin Position:



Pin Assignment:

Pin	Signal	
1	MDI0+	(TP0+)
2	MDI0-	(TP0-)
3	MDI1+	(TP1+)
4	MDI2+	(TP2+)
5	MDI2-	(TP2-)
6	MDI1-	(TP1-)
7	MDI3+	(TP3+)
8	MDI3-	(TP3-)

S	Shield

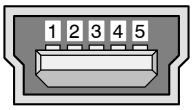
Signal Description:

MDIx+/- ...	Ethernet data lines (x = 0, 1)
Shield...	case shield, connected with the front panel of the XMC-CPU/Zulu

NOTICE
Cables of category CAT 5e or higher must be used to grant the function in networks with up to 1000 Mbits/s.
esd grants the EC conformity of the product if the wiring is carried out with shielded twisted pair cables of class SF/UTP or higher.

7.3 USB Console Port – CON (X1220)

Device connector: 5-pin mini USB socket, standard type B

Pin Position:	Pin Assignment:	
	**Pin**	**CON (X1220)**
	1	V_{BUS} (Input)
	2	D-
	3	D+
	4	-
	5	GND

Signal Description

VBUS...	+5 V power supply voltage
D+, D-...	USB signal lines Data+, Data-
-...	not connected
GND...	Reference potential

7.4 Adapters

esd offers the XMC-CPU-ADAPTER-FPGA and XMC-JTAG-Adapter as accessory, see “Order Information” on page 46.

The adapters must be connected from the bottom side of the XMC-CPU/Zulu.

7.4.1 XMC-CPU-ADAPTER-FPGA

The XMC-CPU-ADAPTER-FPGA (esd order No.: V.2029.03) is an interface to connect the Tool XILINX ChipScope to the XMC-CPU/Zulu connector X1410.

NOTICE
The connector X400 is for factory test only, do not connect!
The adapter can be used by esd to connect X400 to a JTAG chain of the Health Controller and PCIe-to-PCI bridge.

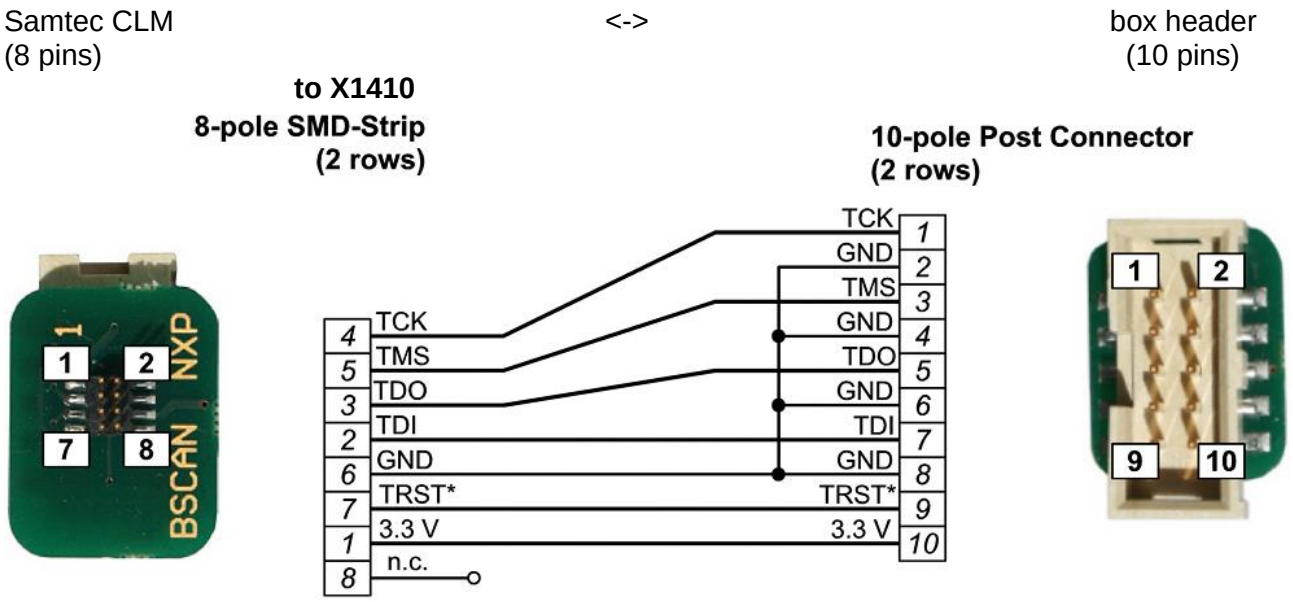


Figure 7: XMC-CPU-ADAPTER-FPGA

NOTICE
The 8-pole SMD strip has no inverse-polarity protection! Property damage may result due to incorrect adapter connection.
Ensure that the connector is inserted in the correct position. See Figure 3 on page 12 for the position of the X1410 connector pins.

7.4.2 XMC-JTAG-Adapter

The XMC-JTAG-Adapter (esd order No.: V.2031.04) is an adapter cable to connect the JTAG-Interface onboard with the programmer (XMC-CPU/Zulu-Testadapter, esd order No.: V.2031.05).
The adapter comes with a header on one side and a socket strip on the other side.
The header can be connected to the CPU/Debug connector (X800 on the PCB bottom side of XMC-CPU/Zulu). The socket strip can be connected to the XMC-CPU/Zulu-Testadapter.
The -JTAG-Adapter comes with a 14-pos. socket strip and a 14-pos. header.

Socket strip and **Header:**

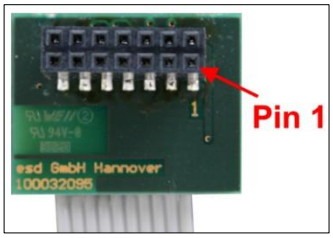


Figure 8: Socket strip

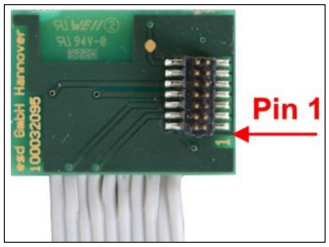


Figure 9: Header

Figure 10: XMC-JTAG-Adapter

NOTICE
The 14-pole SMD strips have no inverse-polarity protection! Property damage may result due to incorrect adapter connection! The header has to be plugged-in on the PCB bottom side of XMC-CPU/Zulu
Ensure that the header is plugged-in in the correct position. See Figure 11 on page 39 for the position of the X800 connector pins.

Connecting the XMC-CPU/Zulu-Testadapter to the XMC-CPU/Zulu via XMC-JTAG-Adapter

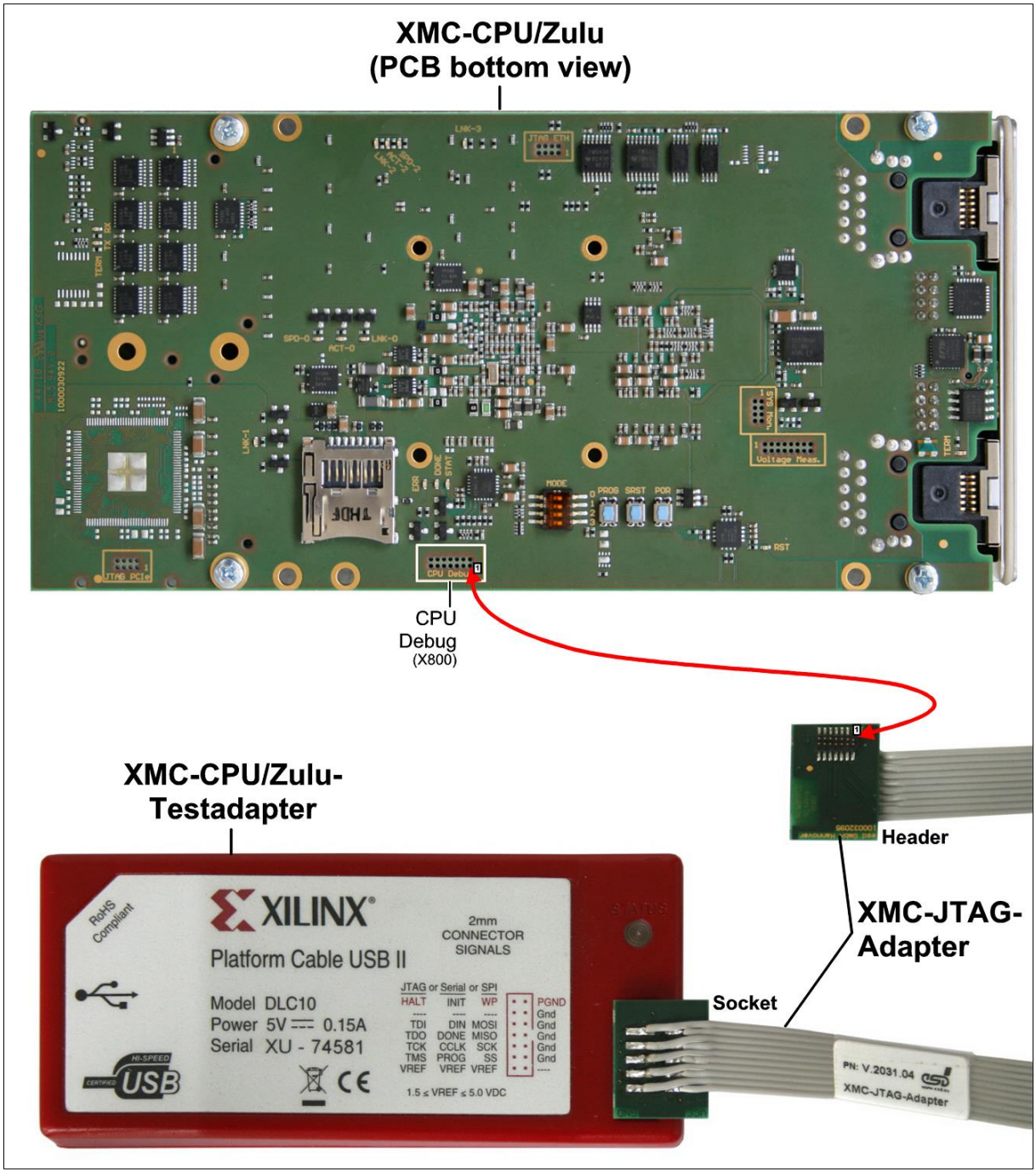


Figure 11: Connecting diagram of the XMC-JTAG-Adapter

8 Software

8.1 Introduction

The firmware of the XMC-CPU/Zulu is based on a Peta Linux distribution and a BSP. Linux is developed on the base of the Xilinx Peta Linux version v2018.2.

The on-board NOR-flash memory carries the standard boot program “Das U-Boot” and enables the XMC-CPU/Zulu to boot various operating systems from the boot device as defined via environment variables.

An alternative boot device can be selected via the MODE switch as described on page 17. This is a helpful feature if you want to develop your own customized firmware.

BSPs from esd are available as described in the “Order Information” on page 46.
The BSPs include an example source code for the FPGA.
Programming of the FPGAs is done via XILINX Toolchain. See www.xilinx.com for further information.

Loading of the FPGA is done during the system Start up as part of loading the BOOT.BIN image.
For the FPGA an esdACC (esd Advanced CAN Controller) implementation is available as customized option.
The esd EtherCAT Master is available for the BSPs developed by esd (see page 46).

For detailed information about the driver availability for your operating system, please contact our sales team: sales@esd.eu

8.2 Overview of Software Components

Name	Description
Peta Linux	Development environment
U-Boot	Bootloader
Linux	Operating system
VHDL-Code	Example FPGA implementation

8.3 Licenses

The complete local firmware is stored in the internal flash and can be updated as required.

8.3.1 Bootloader

Bootloader	“Das U-Boot”
Author / license holder	Denx software engineering
License information	GNU GPLv2+ This product uses the open source-bootloader “Das U- Boot”. The U-Boot-source code is released under the terms of the GNU Public License (GPL). The complete text of the license is contained in the esd-document “3rd Party Licensor Notice” as part of the product documentation. esd provides the complete bootloader-source code on request. The homepage of the U-Boot project is: http://www.denx.de/wiki/U-Boot.
Update Mechanism	Via Ethernet
System Boot	U-Boot is configured in a way that the operating system can boot from different sources: 1.) SPI Flash 2.) eMMC 3.) SD-card

8.3.2 Operating System

Operating system	Peta Linux
Author / license holder	XILINX
Delivery	Download Link
Licenses	Predominantly GPL – a detailed listing of the licenses that must be observed is automatically generated by the Yocto environment.

8.3.3 VHDL-Code

Function	Example implementation for testing the periphery connected to PL.
Author / license holder	esd
Delivery	VHDL Source Code
Documentation	Description of the registers and functionalities in the VHDL source code
Licenses	The rights of use of esd electronics gmbh apply to the software modules provided by esd electronics as the author of the software. For software modules provided by third parties the license terms of these authors or copyright holders will apply.

8.4 Generating Firmware Image

Procedure for generating the firmware image:

- Vivado Tool
With the Vivado tool the configuration of the hardware (Zynq Processing System and connected components) is described, and the FPGA Image is created. The Vivado tool generates an FSBL (First Stage Bootloader) and a hardware project from this.

- Vivado Hardware Project
The hardware project generated by Vivado is used together with a Linux BSP as base for the Peta Linux. By means of Peta Linux a Yocto Linux project is created.
This is done in item "Create Peta Linux project" and "Configure project to match the hardware".

- With the Yocto Linux project the U-Boot and the required Linux components can be created.

The created development toolchain is completely archived once and is provided for download then. All further changes for the XMC-CPU/Zulu will be developed as patches for the Yocto Linux, that has been generated at the creation of the Peta Linux project.

The software only contains the necessary components for the support of the A53 cores, and not of the R5 CPUs which are also contained in the system.

A Boot-Image (BOOT.BIN) which is created with the toolchain usually contains the following components. esd electronics assumes only a limited warranty for the necessary adjustments to the components in the scope of this project.

Name	Short information	Meaning	Source	Comment
FSBL	First stage bootloader	Configuration of the Zynq	esd	Created by the Vivado Tool.
BL31	ARM trusted firmware	Security Manager	Xilinx	Image from Xilinx is taken without changes
U-Boot	Second stage bootloader	Bootloader for Linux	Xilinx / esd	An adequate U-Boot from Xilinx is used and adjusted by esd.
PMUFW	Platform Management Unit Firmware	Sleep mode and temperature-/voltage monitoring	Xilinx	Image from Xilinx is used without changes.
FPGA	Field Programmable Gate Array	Initial code for the PL	esd	Created by the Vivado Project.

After power on the modules listed above are loaded and executed. Finally, the U-Boot is started, that can boot the Linux operating system.

The U-Boot is separately maintained as branch of a Xilinx Git tree and not in the Peta Linux/Yocto project. The branch is delivered to customer by esd.

8.5 Software

8.5.1 Peta Linux

The Xilinx Peta Linux version v2018.2 is used as base for the development of Linux.
The Standard Linux is created by means of the development environment.
By means of Yocto the software adaption for the XMC-CPU/Zulu is integrated.
A combination of single modules built the firmware image.

8.5.2 U-Boot

U-Boot is based on the current version of Xilinx. For the XMC-CPU/Zulu version 2018.01 is used as base and necessary adaptions to the hardware are implemented.
A toolchain for building the U-Boot image is provided.
After powering-up the XMC-CPU/Zulu U-Boot is started and can be operated via the console CON.

Following hardware components are supported by U-Boot:

Hardware	***Description***
RS232	Used as console CON.
GPIO	Only with example FPGA image
Network	PS based interfaces are supported.
SPI	Access to SPI memory.
uSD/eMMC	Storage media can be used as s boot medium or/and file system.
HEALTH	Access on the temperature and voltage values, partly via I²C.
LED	Control of the tricolour LEDs can be done via U-Boot.
FPGA	Booting the FPGA section (PL)
Customized Option:	
RTC	RTC can be read and set.

8.5.3 Linux

Linux as operating system is used as base for a customized application.

The executable Linux system offers the possibility to modify the kernel configuration.
A standard configuration of the listed components (see Table below) of the Linux OS is created.

The operating system provides interfaces for the interaction of the application with hardware components.

The following Linux drivers are implemented:

Hardware	***Description***
RS232	Used as console CON.
GPIO	Only with example FPGA image
Network	PL and PS based interfaces are supported. Test of the standard network functionality.
SPI	Access to SPI memory.
uSD/eMMC	Storage media can be used as file system.
HEALTH	Access on the temperature and voltage values, partly via I²C.
LED	Control of the tricolour LEDs
PCIe	The XMC-CPU/Zulu normally works as PCI endpoint and supports accesses from the PCI Master to a memory range of the XMC-CPU/Zulu and Master accesses to the memory of the HOST system. A dynamic change of the Monarch / Root status is not supported. It is possible to request the Monarch / Root status of U-Boot.
Customized Options:	
CAN	esd IP-Core (esdACC)
RTC	RTC is used by Linux

8.5.4 VHDL-Code

To verify the functionality of the periphery an FPGA implementation is created that allows a rudimentary usage of the periphery that is connected to PL

9 References

[1] Zynq UltraScale™+ Device - Technical Reference Manual by Xilinx
UG1085 (v1.7) December 22, 2017

10 Declaration of Conformity

EU-KONFORMITÄTSERKLÄRUNG
EU DECLARATION OF CONFORMITY

Adresse / *Address*
esd electronics gmbh
Vahrenwalder Str. 207
30165 Hannover
Germany

esd erklärt, dass das Produkt *esd declares, that the product*	Typ, Modell, Artikel-Nr. *Type, Model, Article No.*
XMC-CPU/Zulu	**V.2031.01**
die Anforderungen der Normen *fulfills the requirements of the standards*	**EN 61000-6-2:2005,** **EN 61000-6-4:2007/A1:2011**
gemäß folgendem Prüfbericht erfüllt. *according to test certificate.*	**H-K00-0735-19**
Das Produkt entspricht damit der EU-Richtlinie „EMV" *Therefore the product conforms to the EU Directive 'EMC'*	**2014/30/EU**
Das Produkt entspricht den EU-Richtlinien „RoHS" *The product conforms to the EU Directives 'RoHS'*	**2011/65/EU, 2015/863/EU**

Diese Erklärung verliert ihre Gültigkeit, wenn das Produkt nicht den Herstellerunterlagen entsprechend eingesetzt und betrieben wird, oder das Produkt abweichend modifiziert wird.
This declaration loses its validity if the product is not used or run according to the manufacturer's documentation or if non-compliant modifications are made.

Name / *Name* T. Bielert
Funktion / *Title* QM-Beauftragter / *QM Representative*
Datum / *Date* Hannover, 2019-11-08

Rechtsgültige Unterschrift / *authorized signature*

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11 Order Information

11.1 Hardware

Type	Properties	Order No.
XMC-CPU/Zulu	XMC-CPU based on XILINX Zynq UltraScale+XCZU2CG	V.2031.01
Accessories:		
XMC-JTAG-Adapter	Adapter cable to connect the JTAG-Interface onboard with the programmer (XMC-CPU/Zulu-Testadapter).	V.2031.04
XMC-CPU/Zulu-Testadapter	Test adapter for XMC-CPU/Zulu Signal-Routing XMC-CPU/Zulu P4 <-> pin header P6-IO <-> pin header P6-Eth <-> RJ45 JTAG-Interface <-> pin header Supply: extern 3,3V; 5V; 12V (default) or PCIe (configure via solder jumper) or PCI (configure via solder jumper)	V.2031.05
Software		
Board Support Package		
XMC-CPU/Zulu-Linux BSP	Linux Board Support Package, incl. 12 moths support	V.2031.77
XMC-CPU/Zulu-Linux BSP (Bundle)	BSP Bundle including: - 1 Board-Support-Package (V.2031.77) - 12 months Hotline-Support and Linux BSP Updates (V.2031.67)	V.2031.57
Support for BSPs		
XMC-CPU/Zulu-Linux-Support	Hotline Support and Linux BSP Updates, for 12 months	V.2031.67
For detailed information about the driver availability for your special operating system, please contact our sales team.		

Table 24: Order information for XMC-CPU/Zulu

11.2 Manuals

PDF Manuals
Please download the manuals as PDF documents from our esd website https://www.esd.eu for free.

Manuals		Order No.
XMC-CPU/Zulu-ME	Hardware manual in English	V.2031.21

Table 25: Available Manuals

Printed Manuals
If you need a printout of the manual additionally, please contact our sales team (sales@esd.eu) for a quotation. Printed manuals may be ordered for a fee.