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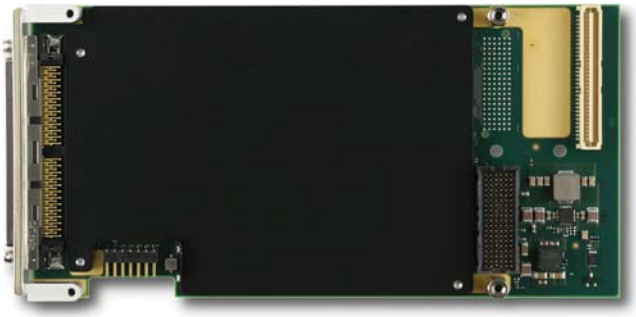
The Embedded I/O Company

TEWS TECHNOLOGIES

TXMC637 Reconfigurable FPGA with 16 x 16 bit Analog Input 8 x 16 bit Analog Output and 32 digital I/O



TXMC637-10R

TXMC637-10R without heat sink

Application Information

The TXMC637 is a standard single-width Switched Mezzanine Card (XMC) compatible module providing a user configurable FPGA (AMD Artix™ 7).

32 ADC input channels, based on four ADAS3022, can be software configured in groups to operate in single-ended or differential mode. Each of the 32 channels has a resolution of 16bit and can work with up to 1 MSPS. The programmable gain amplifier is software configurable and allows a full-scale input voltage range of up to +/-10.24V.

The TXMC637 DAC output channels are based on the Dual 16bit AD5547 DAC. Each DAC output is designed as a configurable single-ended bipolar analog output. Output voltage is configurable as ±10.0V, ±5.0V or ±2.5V.

32 ESD-protected TTL lines provide a flexible digital interface. All I/O lines are individually programmable either as input or output. Input I/O lines are tri-stated and could be used with the on-board pull up or as tri-stated output. Each TTL I/O line has a pull resistor sourced by a common pull source. The pull voltage level is selectable to be either +3.3V, +5V and additionally GND.

16 of these ESD-protected TTL lines can be switched to be either a TTL interface or RS422 interface. Switching is done via the User FPGA. All 8 RS422 transceivers have individual internal switchable terminations.

The User FPGA is connected to a 512 Mbytes, 16 bit wide DDR3L SDRAM. (to be used with the AMD Memory Interface Generator)

For customer specific I/O extension or inter-board communication, the TXMC637 provides 64 FPGA I/Os on P14 (directly connected). All P14 I/O lines can be configured in accordance with 7-Series SelectI/O features e.g. as 64 single ended LVCMOS25 or as 32 differential LVDS25 interface

The User FPGA is configured by a serial quad SPI flash. For full PCIe specification compliance, the AMD Tandem Configuration Feature can be required for FPGA configuration. AMD Tandem Methodologies “Tandem PROM” should be the favored Methodology. The SPI flash device is in-system programmable. An in-circuit debugging option is available via a JTAG header for (real-time) debugging of the FPGA design.

User applications for the TXMC637 with Artix™ 7 FPGA can be developed using the AMD Vivado ™ design tool.

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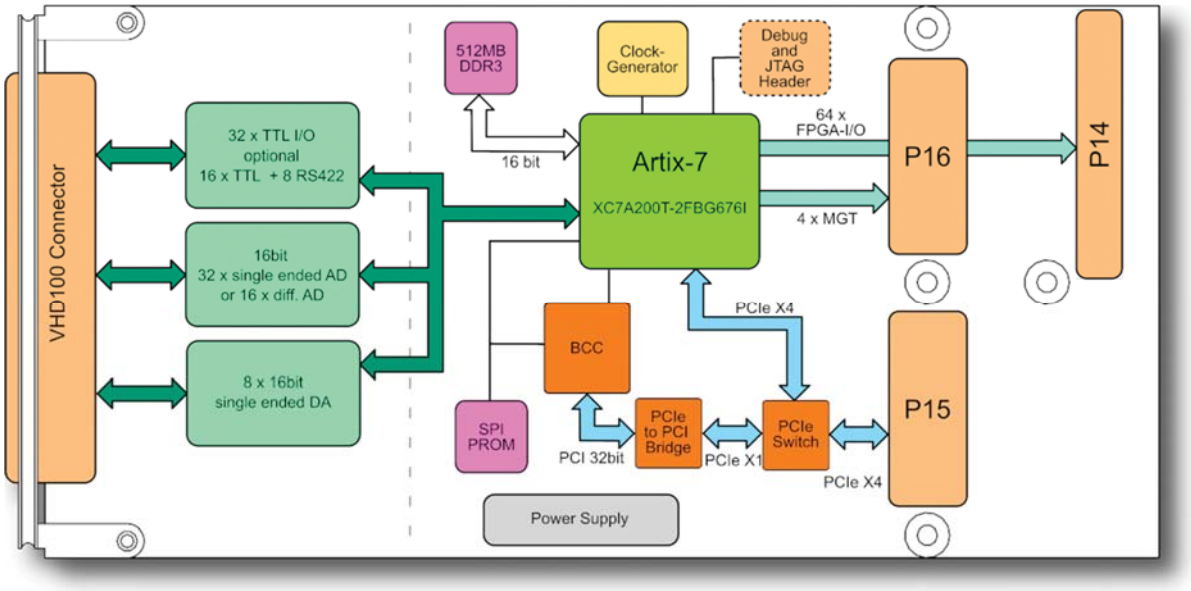
Technical Information

- Form Factor: Standard single width XMC
  - Board size: 149 mm x 74 mm
- PCI Express (Base Specification 1.1) compliant interface conforming to ANSI/VITA 42.3-2006
- IPMI resource: FRU hardware definition information stored in on-board EEPROM
- AMD Artix™ 7 FPGA (XC7A200T-2FBG676I)
- Serial Flash for FPGA Configuration
- FPGA clock options:
  - Local clock generator as source for the FPGA internal PLL
- DDR3 SDRAM bank, 256M x 16 Bit (512MB)
- Front I/O lines
  - 32 single ended or 16 diff. analog inputs
    - 16 bit resolution
    - Programmable input voltage
    - Conversation time: up to 1.1µs
    - Factory calibration
  - 8 channels single-ended analog output
    - 16 bit resolution
    - Programmable output voltage: ±10V, ±5.0 V or ±2.5 V
    - Full scale settling time: typ.1µs
    - Factory calibration
  - 32 digital TTL compatible I/O lines
    - 16 lines optional configured as differential RS422 interface
- P14/P16 Rear I/O lines
  - 64 single ended or 32 differential rear I/O lines on a rear XMC 64pin P14 connector
  - 4 FPGA Multi-Gigabit-Transceiver on a rear XMC P16 connector.
- Operating temperature -40 °C to +85 °C
- MTBF (MIL-HDBK217F/FN2 GB 20 °C): 170 000h



Block Diagram TXMC637

Order Information

RoHS Compliant

TXMC637-10R	Artix™ 7 FPGA XC7A200T-2 FBG676, 512MBDDR3	16 x Analog In, 8 x Analog Out, 32 digital Front I/O, 64 direct FPGA Rear I/O Lines and 4 MGTs Rear I/O ©

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Software

TDRV018-SW-25	Integrity Software Support
TDRV018-SW-42	VxWorks Software Support (Legacy and VxBus-Enabled Software Support)
TDRV018-SW-65	Windows Software Support
TDRV018-SW-82	Linux Software Support
TDRV018-SW-95	QNX Software Support

For other operating systems please contact TEWS.

Related Products

TA110	1.2 m cable with one VHDCI-100 male connector and two male HD50 connector for TXMC637
TA201	50 pin terminal block with 50 pin female SCSI-2 type connector

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